Advantech

AQD-D3L8GN16-MG

Datasheet

Rev. 1.1

2013-09-30

Description

AQD-D3L8GN16-MG is a DDR3 Unbuffered, non-ECC, high-speed, low power memory module that use 16 pcs of 512Mx8bits DDR3 low voltage SDRAM in FBGA package and a 2048 bits serial EEPROM on a 240-pin printed circuit board. AQD-D3L8GN16-MG is a Dual In-Line Memory Module and intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

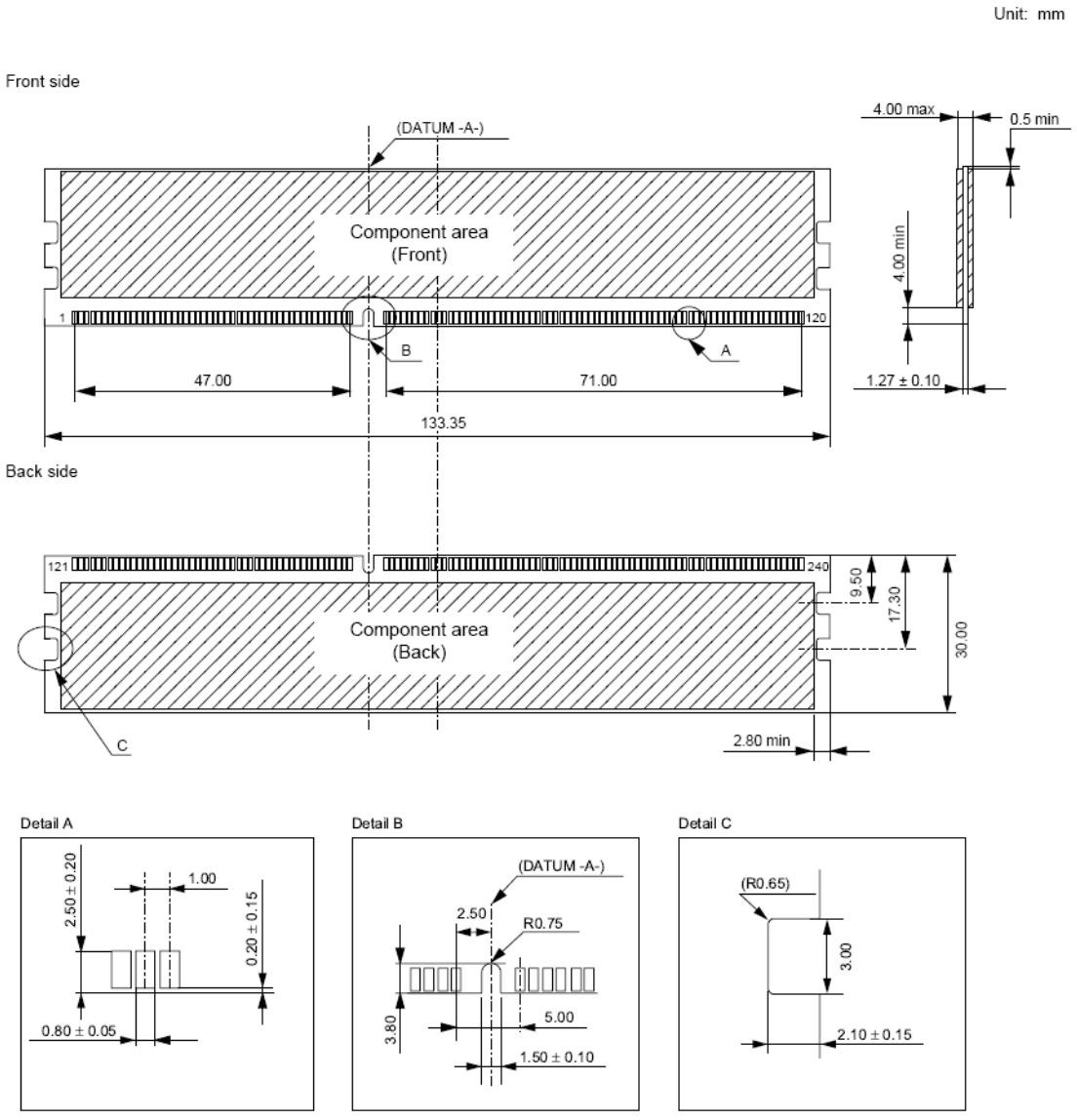
Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.283V~1.45V) Power supply
- JEDEC standard 1.5V(1.425V~1.575V) Power supply
- VDDQ=1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)
- Clock Freq: 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/S0, /S1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
$V_{REF}DQ$	I/O reference supply
$V_{REF}CA$	Command/address reference supply
$V_{DD}SPD$	SPD EEPROM power supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



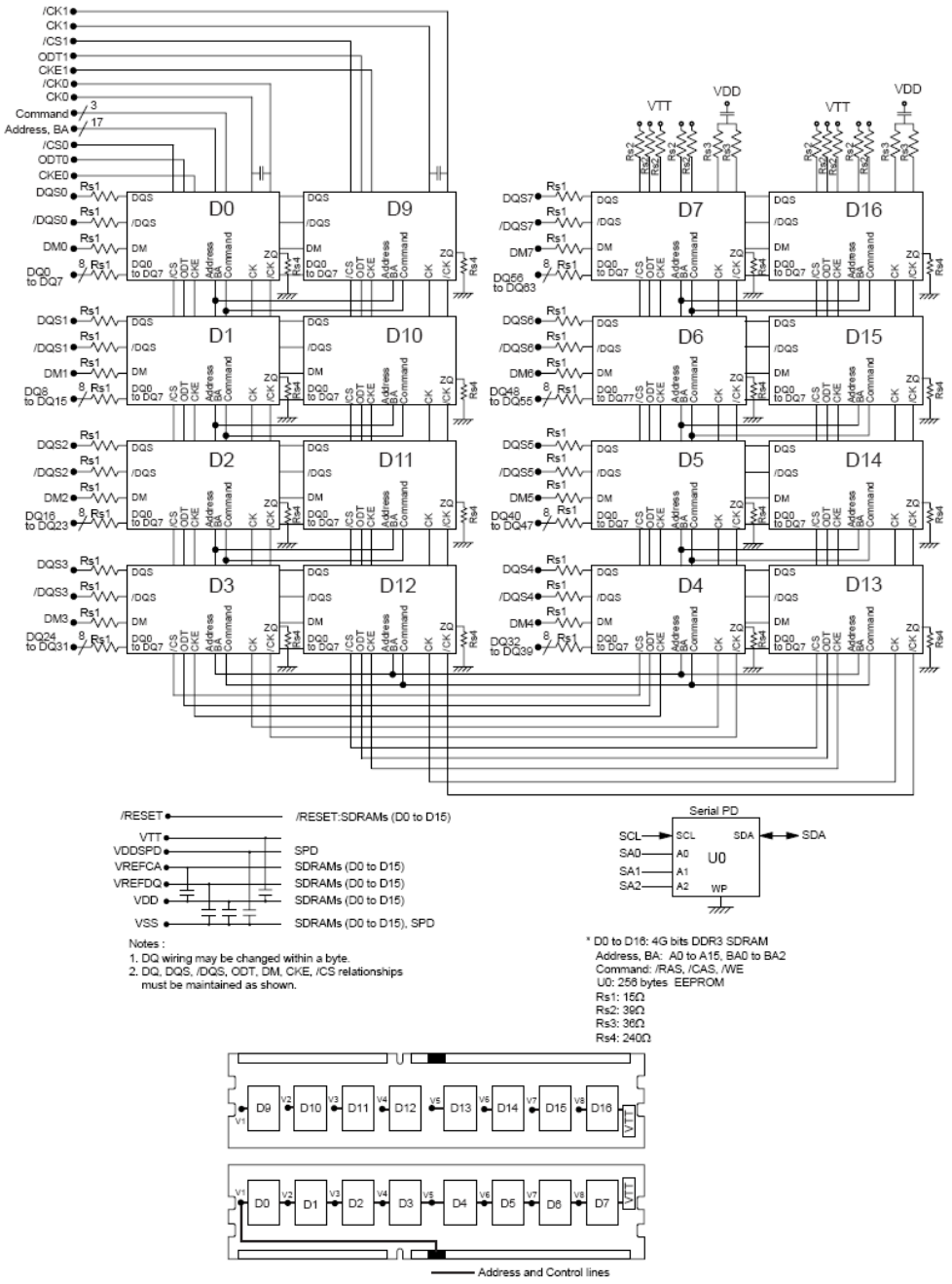
(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3	182	VDD	212	DM5
3	DQ0	33	/DQS3	63	CK1(NC)	93	/DQS5	123	DQ5	153	NC	183	VDD	213	NC
4	DQ1	34	DQS3	64	/CK1(NC)	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	NC	98	VSS	128	DQ6	158	NC	188	A0	218	DQ52
9	DQ2	39	NC	69	VDD	99	DQ48	129	DQ7	159	NC	189	VDD	219	DQ53
10	DQ3	40	NC	70	A10(AP)	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	NC	191	VDD	221	DM6
12	DQ8	42	NC	72	VDD	102	/DQS6	132	DQ13	162	NC	192	/RAS	222	NC
13	DQ9	43	NC	73	/WE	103	DQS6	133	VSS	163	VSS	193	/CS0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1	164	NC	194	VDD	224	DQ54
15	/DQS1	45	NC	75	VDD	105	DQ50	135	NC	165	NC	195	ODT0	225	DQ55
16	DQS1	46	NC	76	/CS1(NC)	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1(NC)	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	NC	78	VDD	108	DQ56	138	DQ15	168	/RESET	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	VSS	169	CKE1(NC)	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15(NC)	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14(NC)	202	VSS	232	VSS
23	VSS	53	NC	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

Note: 1. CS1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs
2. CK1,NC and CK1,NC : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated

Block Diagram
8GB, 1Gx64 Module(2 Rank x8)



Notes :
1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.

* D0 to D16: 4G bits DDR3 SDRAM
Address, BA: A0 to A15, BA0 to BA2
Command: /RAS, /CAS, /WE
U0: 256 bytes EEPROM
Rs1: 15Ω
Rs2: 39Ω
Rs3: 36Ω
Rs4: 240Ω

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.4 ~ 1.975	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4 ~ 1.975	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating Min	Rating Typ.	Rating Max	Unit	Notes
Supply voltage	VDD	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575		
Supply voltage for Output	VDDQ	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575		
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.35V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.5V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	VIH(AC)	1.35V	VREF+0.160	-	-	V	
		1.5V	VREF+0.175	-	-		
AC Input Logic Low	VIL(AC)	1.35V	-	-	VREF-0.160	V	
		1.5V	-	-	VREF-0.175		
DC Input Logic High	VIH(DC)	1.35V	VREF+0.09	-	VDD	V	
		1.5V	VREF+0.1	-	VDD		
DC Input Logic Low	VIL(DC)	1.35V	VSS	-	VREF-0.09	V	
		1.5V	VSS	-	VREF-0.1		

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)

8GB, 1Gx64 Module(2 Rank x8)

Parameter	Symbol	DDR3 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	584	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	672	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-0	288	mA
	IDD2P-1	512	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	512	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	512	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	608	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	608	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1400	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1144	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5B	1384	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	320	mA
Self refresh temperature current (SRT-enabled): MAX TC = 95°C	IDD6ET	400	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1904	mA

Note: 1. Module IDD was calculated on the specific brand DRAM(4xnm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3 1600		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	1.25	<1.5	ns
CK high-level width	tCH	0.47	0.53	tCK
CK low-level width	tCL	0.47	0.53	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK
DQ low-impedance time from CK, /CK	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	225	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS	10	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH	45		ps
DQ and DM input pulse width for each input	tDIPW	360	-	ps
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential Read postamble	tRPST	0.3	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
DQS, /DQS Write postamble	tWPST	0.3	-	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	-450	225	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	225	ps
DQS, /DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	+0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	Max (4tck, 7.5ns)	-	
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	4	-	tCK
/CAS to /CAS command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tck		nCK
Active to active command period for 1KB page size	tRRD	Max (4tck, 6ns)	-	ns

Speed		DDR3 1600		Unit
Parameter	Symbol	Min	Max	
Active to active command period for 2KB page size	tRRD	Max (4tck, 7.5ns)	-	
Four Activate Window for 1KB page size	tFAW	30	-	ns
Four Activate Window for 2KB page size products	tFAW	40	-	ns
Power-up and RESET calibration time	tZQinitl	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQcs	64	-	tCK
Exit self refresh to commands not requiring a locked DLL	tXS	Max (5tCK, tRFC+10ns)	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLL(min)	-	tCK
Internal read to precharge command delay	tRTP	Max (4tck, 7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCK(min)+1tCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	Max (3tCK, 6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	Max (3tCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
ODT turn-off	tAOF	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

AQD-D3L8GN16-MG Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of serial PD bytes written/SPD device size/CRC coverage	CRC 0-116/256/176	92
1	SPD revision	Revision 1.0	10
2	Key byte/DRAM device type	DDR3 SDRAM	0B
3	Key byte/module type	UnbDIMM	02
4	SDRAM density and banks	4Gbits, 8 banks	04
5	SDRAM addressing	16 rows, 10 columns	21
6	Module Nominal Voltage,VDD	Standard = 1.35V	02
7	Module organization	2ranks / x8 bits	09
8	Module memory bus width	64 bits	03
9	Fine timebase (FTB) dividend/divisor	5 / 2	52
10	Medium timebase (MTB) dividend	1	01
11	Medium timebase (MTB) divisor	8	08
12	SDRAM minimum cycle time (tCK (min.))	1.25ns	0A
13	Reserved	—	00
14	SDRAM /CAS latencies supported, LSB	CL=6,7,8,9,10,11	FC
15	SDRAM /CAS latencies supported, MSB	Not support over CL=12	00
16	SDRAM minimum /CAS latencies time (tAA (min.))	13.125ns	69
17	SDRAM write recovery time (tWR)	15ns	78
18	SDRAM minimum /RAS to /CAS delay (tRCD)	13.125ns	69
19	SDRAM minimum row active to row active delay (tRRD)	6ns	30
20	SDRAM minimum row precharge time (tRP)	13.125ns	69
21	SDRAM upper nibbles for tRAS and tRC	Refer to Byte22,23	11
22	SDRAM minimum active to precharge time (tRAS), LSB	35ns	18
23	SDRAM minimum active to active /auto- refresh time (tRC), LSB	48.125ns	81
24	SDRAM minimum refresh recovery time delay (tRFC), LSB	260ns	20
25	SDRAM minimum refresh recovery time delay (tRFC), MSB	260ns	08
26	SDRAM minimum internal write to read command delay (tWTR)	7.5ns	3C
27	SDRAM minimum internal read to precharge command delay (tRTP)	7.5ns	3C
28	Upper nibble for tFAW	Refer to Byte29	00
29	Minimum four activate window delay time (tFAW (min.))	30ns	F0
30	SDRAM output drivers supported	DLL-Off Mode Support/RZQ/6,7	83
31	SDRAM refresh options	PASR / ASR / Normal Temp	85
32	Module Thermal Sensor	not incorporated	00
33	SDRAM type	Standard	00
34~59	Reserved	—	00

60	Module nominal height	29 < height ≦ 30mm	0F
61	Module maximum thickness	thickness ≦ 4 mm	11
62	Reference raw card used	Raw Card B	01
63	Address mapping from edge connecter to DRAM	1 = Mirrored	01
64~116	Module specific section	—	00
117	Module ID: manufacturer's JEDEC ID code, LSB	Apacer	01
118	Module ID: manufacturer's JEDEC ID code, MSB	Apacer	7A
119	Module ID: manufacturing location		00
120	Module ID: manufacturing date	Year code (BCD)	00
121	Module ID: manufacturing date	Week code (BCD)	00
122-125	Module ID: module serial number		00
126	Cyclical redundancy code (CRC)		E5
127	Cyclical redundancy code (CRC)		DE
128	Module part number	A	41
129	Module part number	Q	51
130	Module part number	D	44
131	Module part number	–	2D
132	Module part number	D	44
133	Module part number	3	33
134	Module part number	L	4C
135	Module part number	8	38
136	Module part number	G	47
137	Module part number	N	4E
138	Module part number	1	31
139	Module part number	6	36
140	Module part number	–	2D
141	Module part number	M	4D
142	Module part number	G	47
143	Module part number		20
144	Module part number		20
145	Module part number		20
146	Module revision code		00
147	Module revision code		00
148	SDRAM manufacturer's JEDEC ID code, LSB		00
149	SDRAM manufacturer's JEDEC ID code, MSB		00
150-175	Manufacturer's specific data		00
176-255	Open for customer use		00