NTMFS4839N

Power MOSFET

30 V, 66 A, Single N−Channel, SO−8FL

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb−Free Devices

Applications

- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC−DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	15	A
		T_A = 85°C		11	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.17	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	ID	9.5	A
		T_A = 85°C		7.0	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	0.87	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	66	A
		T_C = 85°C		48	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	41.7	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	132	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	35	A
Drain to Source DV/DT			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 19 A_{pk}, L = 1.0 mH, R_G = 25 Ω			EAS	180.5	mJ
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

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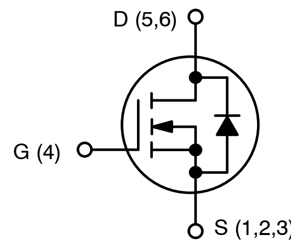
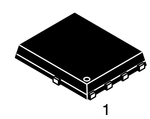
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	5.5 mΩ @ 10 V	66 A
	9.5 mΩ @ 4.5 V	

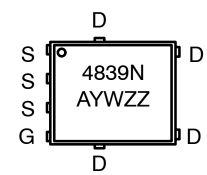


N−CHANNEL MOSFET



SO−8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



A	= Assembly Location	
Y	= Year	
W	= Work Week	
ZZ	= Lot Traceavility	

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4839NT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NTMFS4839NT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	3.0	°C/W
Junction−to−Ambient – Steady State (Note 3)	$R_{\theta JA}$	57.7	
Junction−to−Ambient – Steady State (Note)	$R_{\theta JA}$	143.4	

3. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			1	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.8		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V to 11.5 V	I_D = 30 A		4.5	5.5	mΩ
			I_D = 15 A		4.5		
		V_{GS} = 4.5 V	I_D = 30 A		8.4	9.5	
			I_D = 15 A		8.4		
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 15 A			14.7		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 12 V			1588		pF
Output Capacitance	C_{OSS}				352		
Reverse Transfer Capacitance	C_{RSS}				196		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			13	18	nC
Threshold Gate Charge	$Q_{G(TH)}$				1.6		
Gate−to−Source Charge	Q_{GS}				4.8		
Gate−to−Drain Charge	Q_{GD}				5.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V; I_D = 30 A			28		nC
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			12		ns
Rise Time	t_r				29		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				7.0		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			8.0		ns
Rise Time	t_r				21		
Turn−Off Delay Time	$t_{d(OFF)}$				24		
Fall Time	t_f				7.0		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.8		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 30 A			22.2		ns
Charge Time	t_a				12.5		
Discharge Time	t_b				9.7		
Reverse Recovery Charge	Q_{RR}				10.8		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.93		nH
Drain Inductance	L_D				0.005		nH
Gate Inductance	L_G				1.84		nH
Gate Resistance	R_G				3.3		Ω

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

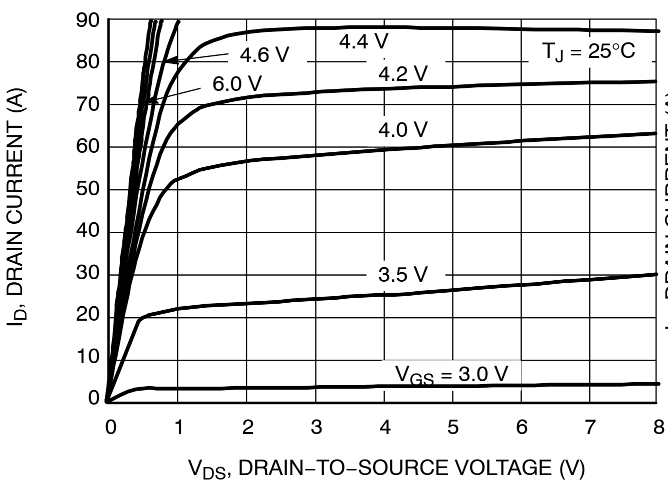


Figure 1. On−Region Characteristics

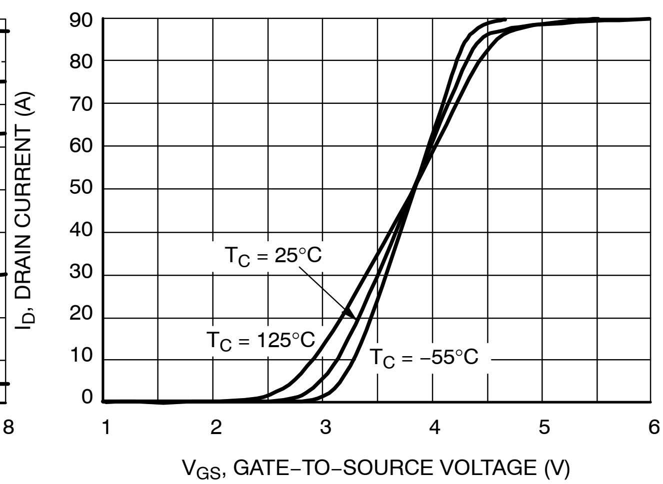


Figure 2. Transfer Characteristics

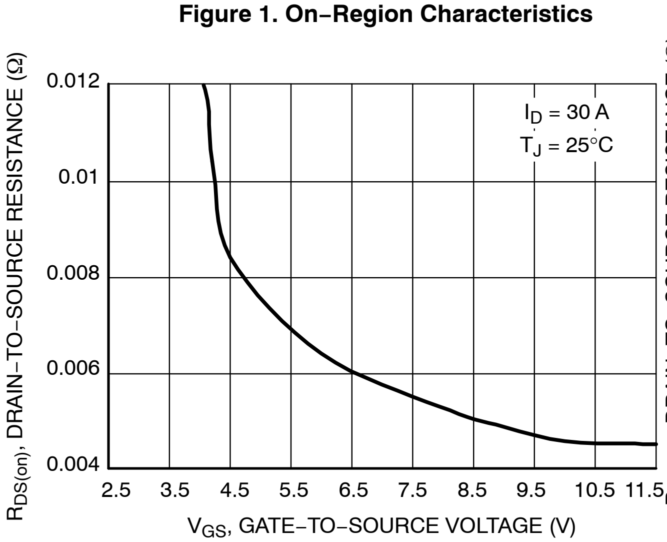


Figure 3. On−Resistance versus Gate−to−Source Voltage

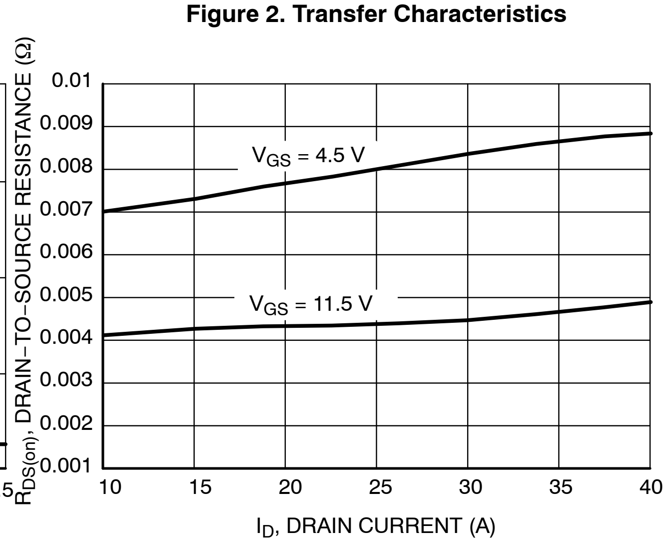


Figure 4. On−Resistance versus Drain Current and Temperature

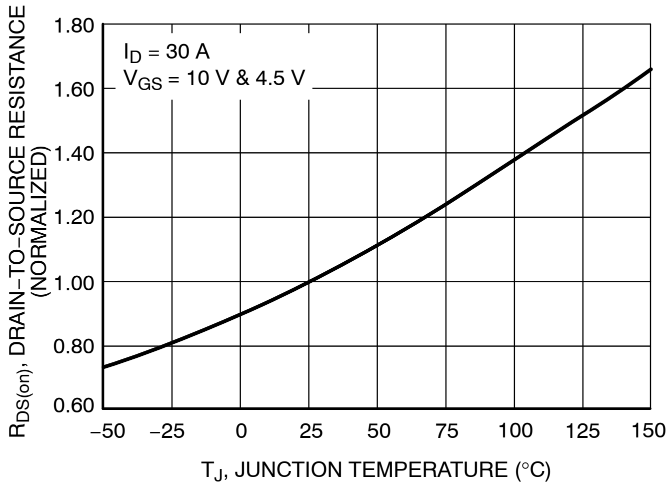


Figure 5. On−Resistance Variation with Temperature

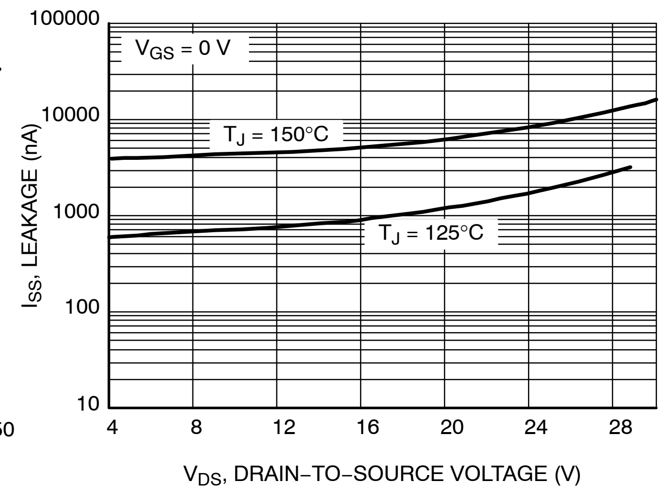


Figure 6. Drain−to−Source Leakage Current versus Voltage

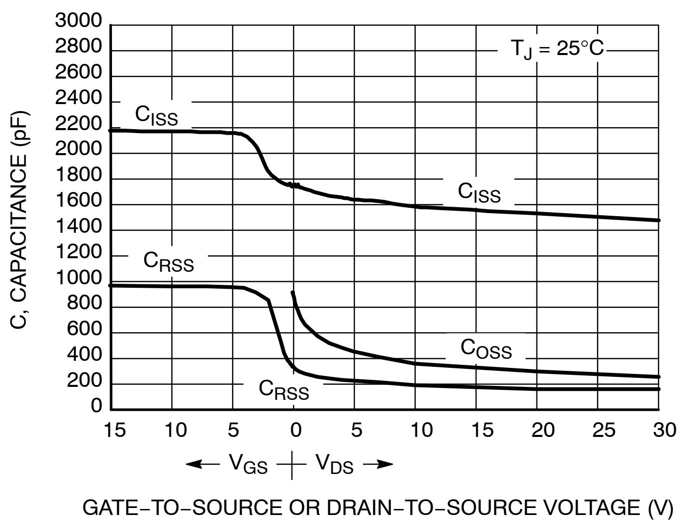


Figure 7. Capacitance Variation

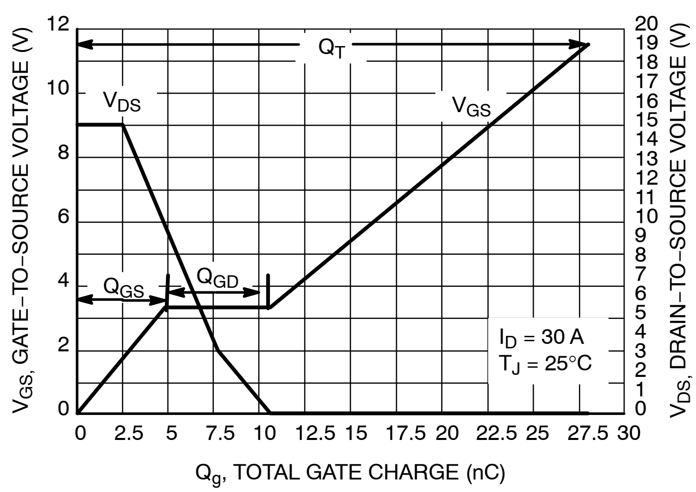


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Gate Charge

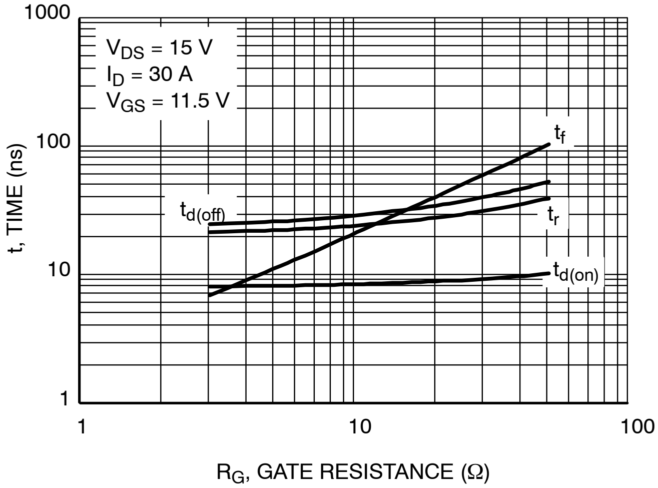


Figure 9. Resistive Switching Time Variation versus Gate Resistance

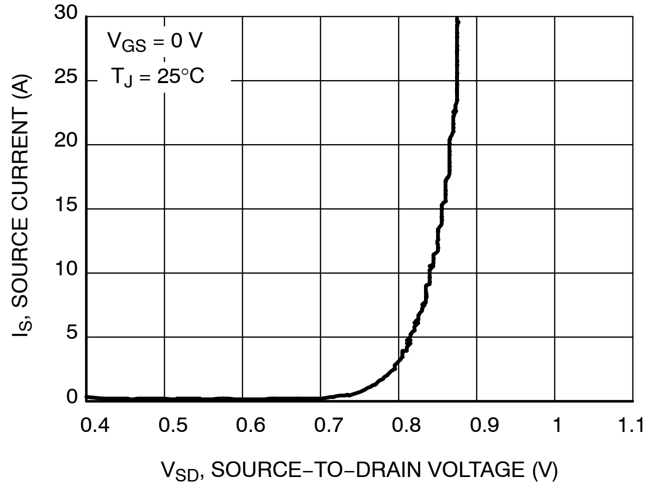


Figure 10. Diode Forward Voltage versus Current

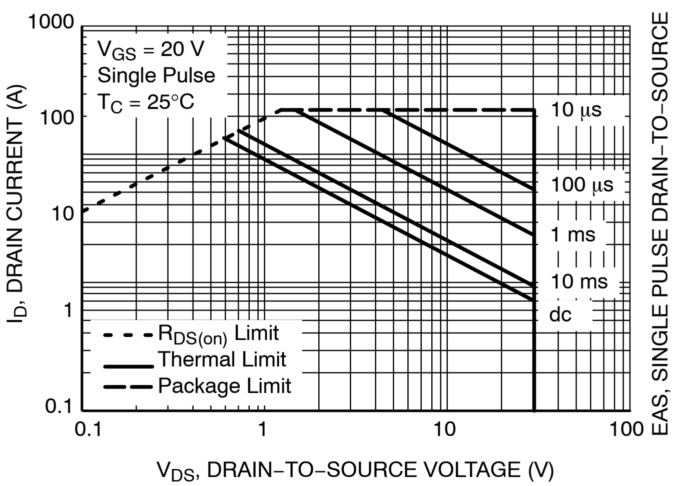


Figure 11. Maximum Rated Forward Biased Safe Operating Area

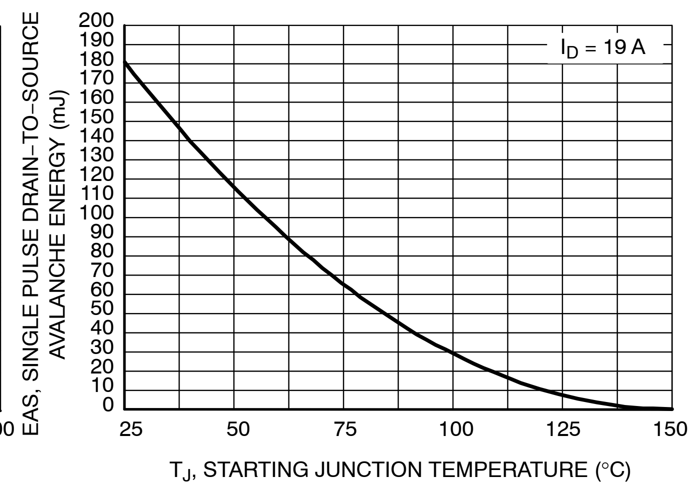
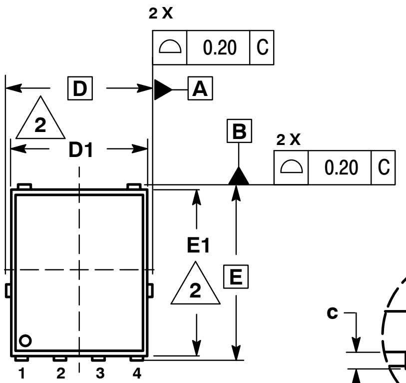


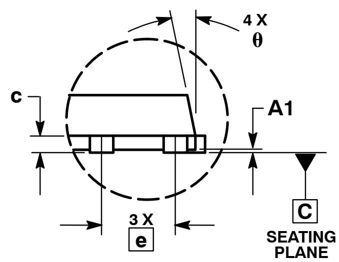
Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

PACKAGE DIMENSIONS

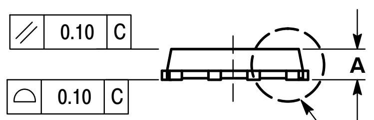
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE G



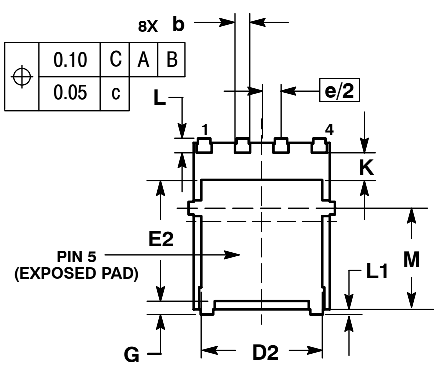
TOP VIEW



DETAIL A



SIDE VIEW DETAIL A



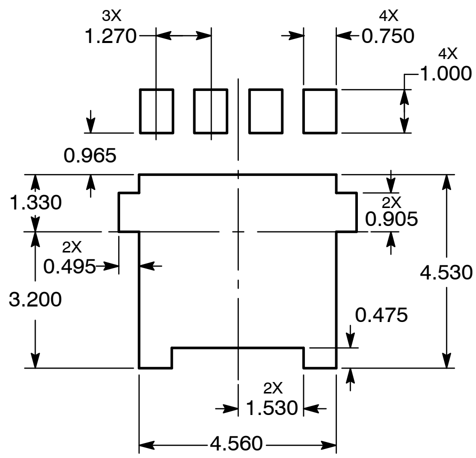
BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	−−−	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	−−−	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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