Advantech

AQD-D4U4GE24-SG

Datasheet

Rev. 1.0

2017-03-13

Description

DDR4 1.2V ECC Unbuffered DIMM is high-speed, low power memory module that use 512Mx8bits DDR4 SDRAM in FBGA package and a 4096 bits serial EEPROM on a 288-pin printed circuit board. DDR4 1.2V Unbuffered DIMM is a Dual In-Line Memory Module and is intended for mounting into 288-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

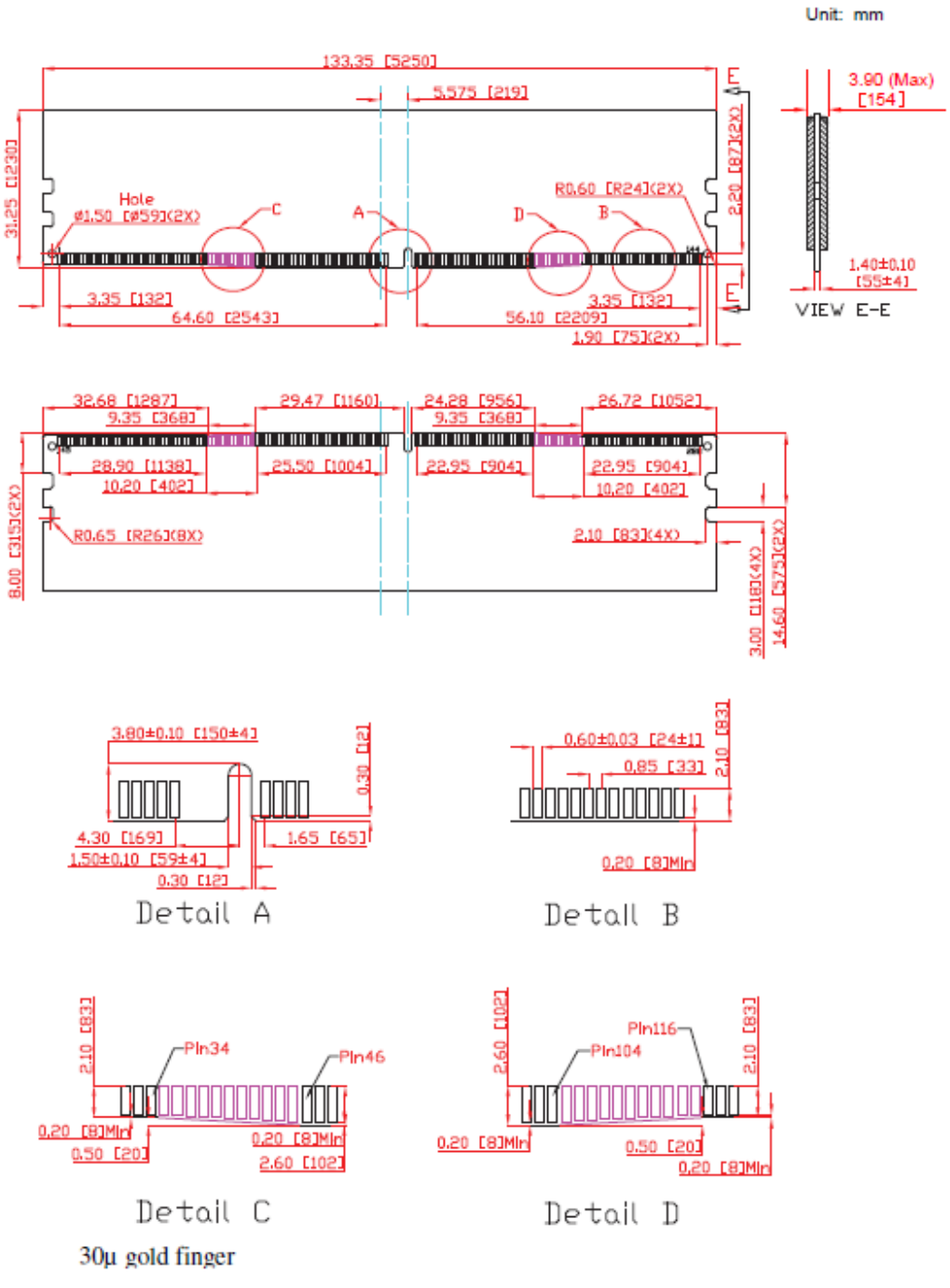
- RoHS compliant products
- JEDEC standard 1.2V (1.14V to 1.26V) Power supply
- VDDQ=1.2V (1.14V to 1.26V)
- Clock Freq: 1200MHZ for 2400Mb/s/Pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10, 11, 12, 13, 14,15,16, 17,18
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 12,16 (DDR4-2400)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset
- PCB: 30µ gold finger

Pin Identification

Symbol	Function
A0–A17	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n2	Register row address strobe input
CAS_n3	Register column address strobe input
WE_n4	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register

SA0–SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection

Dimensions (Unit: millimeter)



30µ gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Pin Assignments

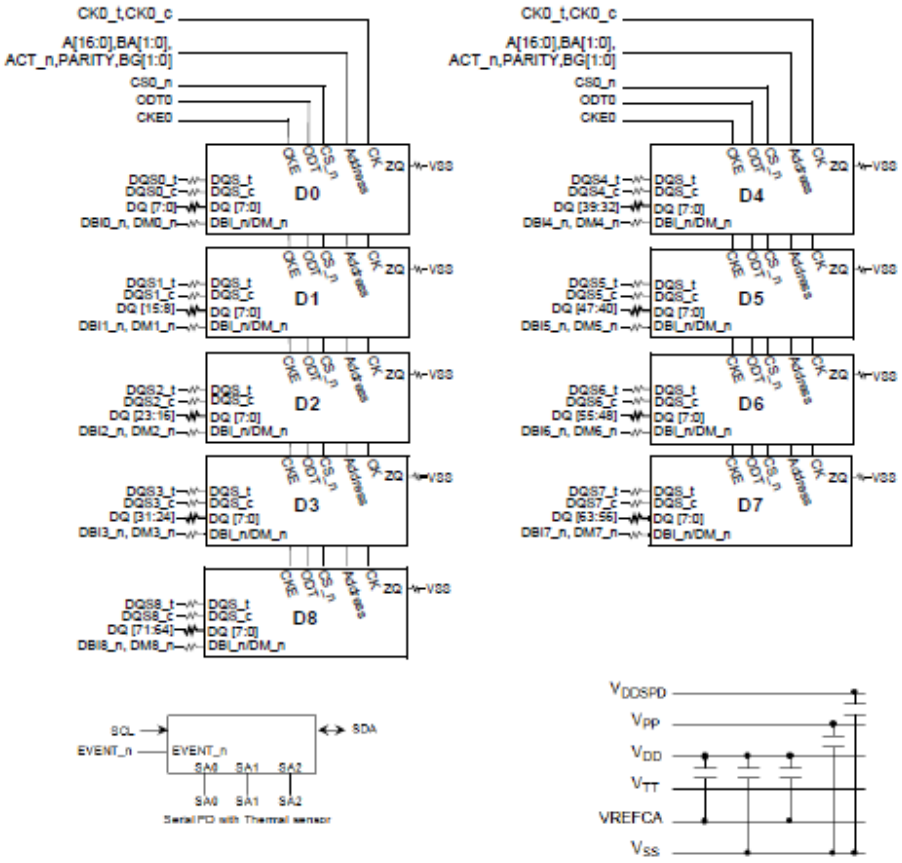
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	NC	145	NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DM3_n, DBI3_n, NC	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	NC	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DM0_n,DBI0_n, NC	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	NC	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	DM6_n, DBI6_n, NC	265	VSS
9	VSS	153	DQS0_t	47	CB4, NC	191	VSS	84	CS0_n	228	WE_n/A14	122	NC	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5, NC	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0, NC	193	VSS	86	CAS_n/A15	230	NC	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1, NC	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DM8_n, DBI8_n, NC	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	NC	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6, NC	198	VSS	91	ODT1	235	NC	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7, NC	92	VDD	236	VDD	130	DQ56	274	VSS
18	DM1_n, DBI1_n, NC	162	VSS	56	CB2, NC	200	VSS	93	NC	237	NC	131	VSS	275	DQ57
19	NC	163	DQS1_c	57	VSS	201	CB3, NC	94	VSS	238	SA2	132	DM7_n, DBI7_n, NC	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	NC	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63

24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DM4_n, DBI4_n, NC	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	NC	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12/BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DM2_n, DBI2_n, NC	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	NC	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DM5_n, DBI5_n, NC	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	NC	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

NOTE :

1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Block Diagram
4GB, 512Mx72 Module(1 Rank x8)



Note 1: CK1_t, CK1_c terminated with 75 Ω ± 5% resistor.
Note 2: Unless otherwise noted resistors are 15 Ω ± 5%.
Note 3: ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
Note 4: Event_n is used for SPD with TS. Option Resistor for it should be placed.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1,3
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1,3
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	4
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1,3
Storage temperature	TSTG	-55~+100	°C	1,2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC Operating Conditions

Recommended DC operating conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

AC & DC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		Min.	Max.		
VIH.CA(DC75)	DC input logic high	VREFCA+ 0.075	VDD	V	
VIL.CA(DC75)	DC input logic low	VSS	VREFCA-0.075	V	
VIH.CA(AC100)	AC input logic high	VREF + 0.1	Note 2	V	1
VIL.CA(AC100)	AC input logic low	Note 2	VREF - 0.1	V	1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	V	2,3

NOTE :
1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3. For reference : approx. VDD/2 ± 12mV

Timing Parameters & Specifications

Speed		DDR4 2400		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	0.833	<0.938	ns
CK high-level width	tCH	0.48	0.52	tCK
CK low-level width	tCL	0.48	0.52	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	0.16	tCK(avg) /2
DQ output hold time from DQS, /DQS	tQH	0.76	-	tCK(avg) /2
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-300	150	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	150	ps
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18		tCK
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
		1.8		tCK
DQS, /DQS differential Read postamble	tRPST	0.33	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
		1.8	NA	tCK
DQS, /DQS Write postamble	tWPST	0.33	-	tCK
DQS, /DQS differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	+0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK
Delay from start of internal write transaction to internal read com-mand for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max (4nCK,7.5ns)		
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	8	-	nCK
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK

CAS_n to CAS_n command delay for different bank group	tCCD_S	4		nCK
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5 .3ns)	-	nCK
Parameter	**Symbol**	**Min**	**Max**	**Unit**
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	RRD_S(1K)	Max(4nCK,3 .3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,3 .3ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6 .4ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4 .9ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4 .9ns)		nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)		ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	-	ns
Power-up and RESET calibration time	tZQinitl	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation short calibration time	tZQcs	128	-	nCK
Exit self refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	
Internal read to precharge command delay	tRTP	max (4nCK,7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	max (4nCK,6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	max (3nCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	ns

SERIAL PRESENCE DETECT SPECIFICATION

4096MB(512Mx72Bit) Serial Presence Detect for DDR4 ECC DIMM (PC-19200) 2400 CL=17

BYTE	FUNCTION DESCRIDED	FUNCTION SUPPORTED	HEX VALUE
0	Number of serial PD bytes written/SPD device size/CRC coverage	512B Total, 384B Used	23
1	SPD revision	Revision 1.0	10
2	Key byte/DRAM device type	DDR4 SDRAM	0C
3	Key byte/module type	UDIMM	02
4	SDRAM density and banks	4Gb, 4BG, 4Banks	84
5	SDRAM addressing	15 rows, 10 columns	19
6	SDRAM package type	Monolithic DRAM Device	00
7	SDRAM optional features	Unlimited MAC	08
8	SDRAM thermal and refresh options	—	00
9	Other SDRAM optional feature	sPPR supported	60
10	Reserved	—	00
11	Module Nominal Voltage,VDD	1.2V	03
12	Module organization	1Ranks / x8 bits	01
13	Module memory bus width	72 bits / with ECC	0B
14	Module thermal sensor	Incorporated	80
15	Reserved	—	00
16	Reserved	—	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM minimum cycle time(tCKAVG min)	0.833ns	07
19	SDRAM maximum cycle time(tCKAVG max)	1.5ns	0C
20	CAS latencies supported, first byte	CL=10,11,12,13,14,15,16,17,18	F8
21	CAS latencies supported, second byte	CL=10,11,12,13,14,15,16,17,18	0F
22	CAS latencies supported, third byte	CL=10,11,12,13,14,15,16,17,18	00
23	CAS latencies supported, fourth byte	CL=10,11,12,13,14,15,16,17,18	00
24	Minimum CAS latency time(tAA min)	13.75ns	6E
25	Minimum RAS to CAS delay time(tRCD min)	13.75ns	6E
26	Minimum Row precharge delay time(tRP min)	13.75ns	6E

27	Upper nibbles for tRAS min and tRC min	tRAS = 32ns, tRC = 45.75ns	11
28	Minimum active to precharge delay time(tRAS min), least significant byte	32ns	00
29	Minimum active to active/refresh delay time(tRC min), least significant byte	45.75ns	6E
30	Minimum refresh recovery delay time(tRFC1 min), LSB	260ns	20
31	Minimum refresh recovery delay time(tRFC1 min), MSB	260ns	08
32	Minimum refresh recovery delay time(tRFC2 min), LSB	160ns	00
33	Minimum refresh recovery delay time(tRFC2 min), MSB	160ns	05
34	Minimum refresh recovery delay time(tRFC3 min), LSB	110ns	70
35	Minimum refresh recovery delay time(tRFC3 min), MSB	110ns	03
36	Minimum four activate window time(tFAW min), most significant nibble	21ns	00
37	Minimum four activate window time(tFAW min), least significant byte	21ns	A8
38	Minimum activate to activate delay time(tRRD_S min), different bank group	3.3ns	1B
39	Minimum activate to activate delay time(tRRD_L min), same bank group	4.9ns	28
40	Minimum CAS to CAS delay time(tCCD_L min), same bank group	5ns	28
41	Upper Nibble for tWR min	15ns	00
42	Minimum Write Recovery Time (tWR min)	15ns	78
43	Upper Nibbles for tWTR min	2.5ns	00
44	Minimum Write to Read Time (tWTR_S min), different bank group	2.5ns	14
45	Minimum Write to Read Time (tWTR_L min), same bank group	7.5ns	3C
46~59	Reserved	—	00
60	Connector to SRAM bit mapping	DQ0 - 3	16
61	Connector to SRAM bit mapping	DQ4 - 7	36
62	Connector to SRAM bit mapping	DQ8 - 11	16
63	Connector to SRAM bit mapping	DQ12 - 15	36
64	Connector to SRAM bit mapping	DQ16 - 19	16
65	Connector to SRAM bit mapping	DQ20 - 23	36
66	Connector to SRAM bit mapping	DQ24 - 27	16
67	Connector to SRAM bit mapping	DQ28 - 31	36
68	Connector to SRAM bit mapping	CB0 - 3	16

69	Connector to SRAM bit mapping	CB4 - 7	36
70	Connector to SRAM bit mapping	DQ32 - 35	16
71	Connector to SRAM bit mapping	DQ36 - 39	36
72	Connector to SRAM bit mapping	DQ40 - 43	16
73	Connector to SRAM bit mapping	DQ44 - 47	36
74	Connector to SRAM bit mapping	DQ48 - 51	16
75	Connector to SRAM bit mapping	DQ52 - 55	36
76	Connector to SRAM bit mapping	DQ56 - 59	16
77	Connector to SRAM bit mapping	DQ60 - 63	36
78~116	Reserved	—	00
117	Fine offset for minimum CAS to CAS delay time (tCCD_L min), same bank group	5ns	00
118	Fine offset for minimum activate to activate delay time (tRRD_L min), same bank group	4.9ns	9C
119	Fine offset for minimum activate to activate delay time (tRRD_S min), different e bank group	3.3ns	B5
120	Fine offset for minimum activate to activate/refresh delay time(tRC min)	45.75ns	00
121	Fine offset for minimum ROW precharge delay time (tRP min)	13.75ns	00
122	Fine offset for minimum RAS to CAS delay time(tRCD min)	13.75ns	00
123	Fine offset for minimum CAS latency time (tAA min)	13.75ns	00
124	Fine offset for SDRAM maximum cycle time(tCKAVG max)	1.6ns	E7
125	Fine offset for SDRAM minimum cycle time(tCKAVG min)	0.833ns	D6
126	CRC for base configuration section section, Least significant byte	F9	F9
127	CRC for base configuration section section, Most significant byte	C1	C1
128	Raw card extension, module nominal height	R/C D, 31.25mm	11
129	Module maximum thickenss	1 < thickness ≤ 2mm	11
130	Reference raw card used	Row Card D	03
131	Address mapping from edge connector to DRAM	Standard = 0	00
132~253	Reserved	—	00
254	CRC for base configuration section section, Least significant byte	E7	E7
255	CRC for base configuration section section, Most significant byte	AF	AF
256-319	Reserved	—	00

320	Module manufacturer's ID code, least significant byte	Apacer	01
321	Module manufacturer's ID code, least significant byte	Apacer	7A
322	Module manufacturing location		00
323	Module manufacturing date		00
324	Module manufacturing date		00
325	Module serial number		00
326	Module serial number		00
327	Module serial number		00
328	Module serial number		00
329	Module part number	A	41
330	Module part number	Q	51
331	Module part number	D	44
332	Module part number	-	2D
333	Module part number	D	44
334	Module part number	4	34
335	Module part number	U	55
336	Module part number	4	34
337	Module part number	G	47
338	Module part number	E	45
339	Module part number	2	32
340	Module part number	4	34
341	Module part number	-	2D
342	Module part number	S	53
343	Module part number	G	47
344	Module part number		20
345	Module part number		20
346	Module part number		20
347	Module part number		20
348	Module part number		20

349	Module revision code		00
350	DRAM manufacturer's ID code, least significant byte		00
351	DRAM manufacturer's ID code, least significant byte		00
352	DRAM stepping		00
353-381	Module manufacturer's specific data		00
382-383	Reserved		00
384-511	End user programmable		00