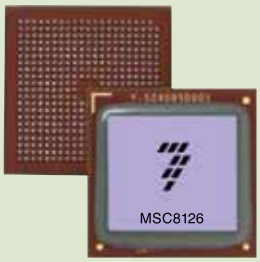
Digital Signal Processors

MSC8126



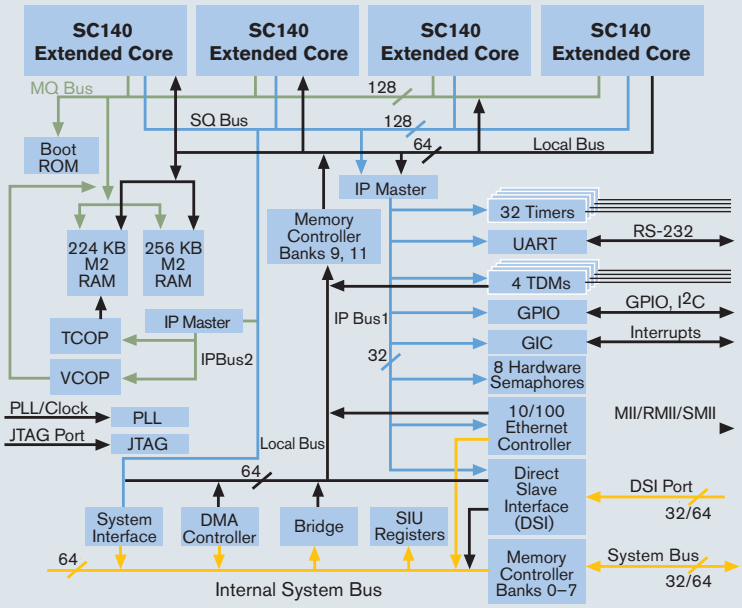
The Wireless Infrastructure DSP

What makes a wireless DSP?

Evolving standards are creating new technology demands in the wireless infrastructure market, and manufacturers and designers must meet the challenges of the rising costs of migration to new process technologies. Taking full advantage of the scalable StarCore™ architecture, the MSC8126 multicore DSP for wireless infrastructure is designed to enable developers to create next-generation networking products that offer flexibility, scalability and upgradability.

This highly integrated system-on-a-chip device integrates four SC140 extended cores and 1.43 MB of on-chip memory. It delivers 8000 MMACS (million multiply accumulates per second) of performance at 500 MHz, equivalent to 2.0 GHz effective performance. The MSC8126 signals a breakthrough for 3G wireless basestations—it is produced with 90-nanometer process technology and delivers tremendous channel density while maintaining a low power dissipation per channel.

MSC8126 BLOCK DIAGRAM

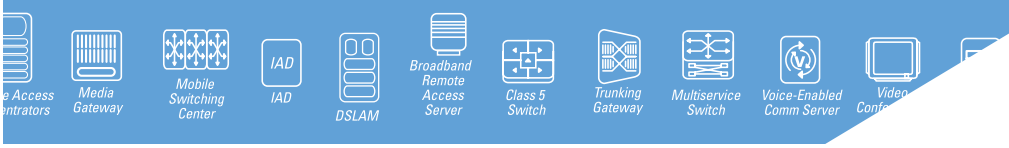


Note: The arrows show the direction from which the transfer originates.

Optimizing time in market and minimizing development costs, the MSC8126 helps speed wireless infrastructure products to market. The MSC8126 also is designed to enable Freescale's Smart Baseband Solution based upon Reconfigurable Compute Fabric (RCF) technology—a cost-effective and programmable alternative to ASIC- and FPGA-based baseband design.

The MSC8126 combines four SC140 extended cores based on StarCore technology with a turbo coprocessor (TCOP), a Viterbi coprocessor (VCOP), an RS-232 serial interface, four time division multiplexing (TDM) serial interfaces, 32 general-purpose timers, a flexible system interface unit (SIU), an Ethernet interface and a multichannel DMA engine. The MSC8126 is offered at two core speed levels: 400 MHz and 500 MHz.

Developers may design with speed and confidence: The MSC8126 is code-compatible with the existing MSC8102, MSC8101 and MSC8103 and pin-compatible with the MSC8102. In addition, development tools and off-the-shelf software are available from Freescale and third parties.



Launched by Motorola

freescale semiconductor

DIFFERENCES BETWEEN MSC8102 AND MSC8126

Feature	MSC8102	MSC8126
Core voltage	1.6V ± 0.1V	1.2V ± 0.06V (400 MHz) 1.2V ± 0.04V (500 MHz)
Target operating frequency	250 MHz and 275 MHz	400 MHz and 500 MHz
Pin definition differences	As defined in the MSC8102 Technical Data Sheet and the MSC8102 Reference Manual (MSC8102RM)*	Fifteen Ethernet signals are multiplexed with two sets of existing signal lines; an additional three dedicated Ethernet signals were converted from two power pins and one ground pin on the MSC8102
Memory maps	As defined in the MSC8102 Reference Manual (MSC8102RM)*	Adds programmable registers for the Ethernet controller in the space after the TDM registers, which can be accessed from the IPBus, local bus or DSI; adds a Pseudo Command Address space that makes a boot register available to TDM, UART and I^2C boot master devices
Ethernet controller	None	**IEEE**® Std. 802.3™, Std. 802.3u™, Std. 802.3x™ and Std. 802.3ac™ compliant; supports MII, RMII and SMII
I^2C interface	None	Engineered to support the standard I^2C signals (SDA and SCL); designed to permit boot from a slave memory device
Turbo coprocessor (TCOP)	None	Designed to support 20 384 kbps channels or three 2 Mbps channels; 3GPP and CDMA2000™ standards; 8-state PCCC as supported by the 3G standards; iterative decoding structure based on Maximum A-Posteriori probability (MAP)
Viterbi coprocessor (VCOP)	None	Fully programmable feed-forward channel decoding, feed forward channel equalization and trace-back sessions; at 500 MHz, designed to support up to 400 3GPP 12.2 kbps AMR channels

*Available at **www.freescale.com**

Features

> Four 400 MHz/500 MHz SC140 extended cores

> 224 KB of dedicated, zero-wait-states M1 memory for each extended core

> 16 KB, 16-way instruction cache in each extended core

> 476 KB of shared M2 memory between each extended core

> Viterbi coprocessor (VCOP) designed to support:

- 400 3GPP 12.2 kbps AMR channels at 500 MHz
- Fully programmable feed-forward channel decoding
- Feed-forward channel equalization
- Trace-back sessions

> Turbo coprocessor (TCOP) designed to support:

- 20 384 kbps channels or three 2 Mbps channels
- 3GPP and CDMA2000™ standards
- 8-state PCCC with polynomial as supported by the 3G standards
- Iterative decoding structure based on Maximum A-Posteriori probability (MAP)
- Flexible block size (1–32767 bits)

> Ethernet interface designed to comply with **IEEE** Std. 802.3, Std. 802.3u, Std. 802.3x and Std. 802.3ac

> Configurable dual bus architecture

> 32- or 64-bit industry-standard external 60x-compatible bus interface

> 32- or 64-bit high-performance direct slave interface (DSI)

> Four independent TDM interfaces supporting up to 1024 DS-O (64 kbps channels)

> Flexible memory controller for various external memory types

> 16-channel DMA engine designed to facilitate independent data transfers

> 32 16-bit timers with watchdog mode support

> 0.8 mm pitch 20 mm x 20 mm Flip-Chip Plastic Ball-Grid Array (FC-PBGA)

> I^2C port compatible with I^2C bus standard and widespread I^2C serial EEPROM access protocol

> 4 KB bootstrap ROM

> 1.2V extended core; 3.3V I/O

Benefits

> Up to 8000 MMACS of DSP performance capability

> Viterbi coprocessor (VCOP) and turbo coprocessor (TCOP) decoding engineered to accelerate error correction for voice and data channels

> Fast Ethernet interface provides direct access to packet networks, enabling glueless interface to onboard Ethernet switches

> Code-compatible with the existing MSC8102, MSC8101 and MSC8103

> Pin-compatible with the MSC8102

> High code density that results in low system costs

> Industry's highest channel density, enabling processing of 80 AMR channels

Software Development Tools

> Tools integrated in an integrated development environment (IDE)

> Real-time debug capability for each extended core

> Optimized C compiler designed to generate efficient control and DSP code

> Real-time operating system (RTOS) designed to fully support device architecture (multicore, memory, hierarchy, I-Cache, timers, DMA, interrupts, peripherals)

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

Document Number: MSC8126FS
REV 4

Launched by Motorola
freescale semiconductor