

# BLF189XRA; BLF189XRAS

Power LDMOS transistor

AMMPLION

Rev. 1 — 6 November 2017

Product data sheet

## 1. Product profile

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### 1.1 General description

A 1700 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 500 MHz band.

Table 1. Application information

Test signal	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	η <sub>D</sub>
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	1700	26.2	74

### 1.2 Features and benefits

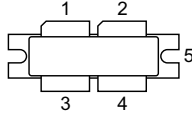
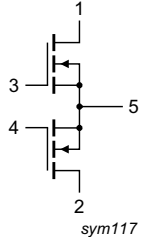
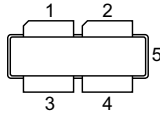
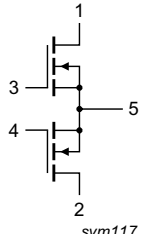
- Easy power control
- Integrated dual sided ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF189XRA (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		
<b>BLF189XRAS (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF189XRA	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF189XRAS	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	135	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature <a href="#">[1]</a>		-	225	°C

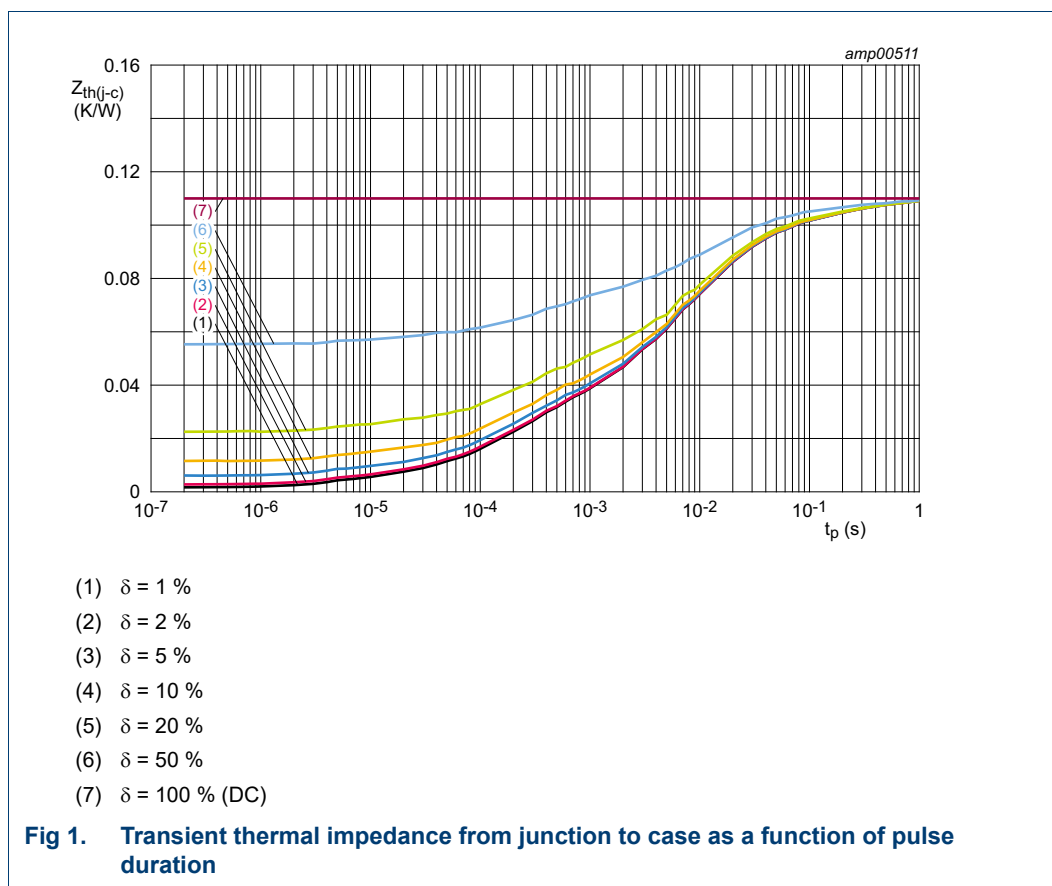
[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ °C}$ [1][2]	0.11	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ °C}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ %}$	0.033	K/W

- [1]  $T_j$  is the junction temperature.
- [2]  $R_{th(j-c)}$  is measured under RF conditions.
- [3] See [Figure 1](#).



## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C};$  per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 6.6\text{ mA}$	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 660\text{ mA}$	1.33	1.9	2.33	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 75\text{ mA}$	1.11	1.7	2.11	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$

**Table 6. DC characteristics ...continued**  
 $T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

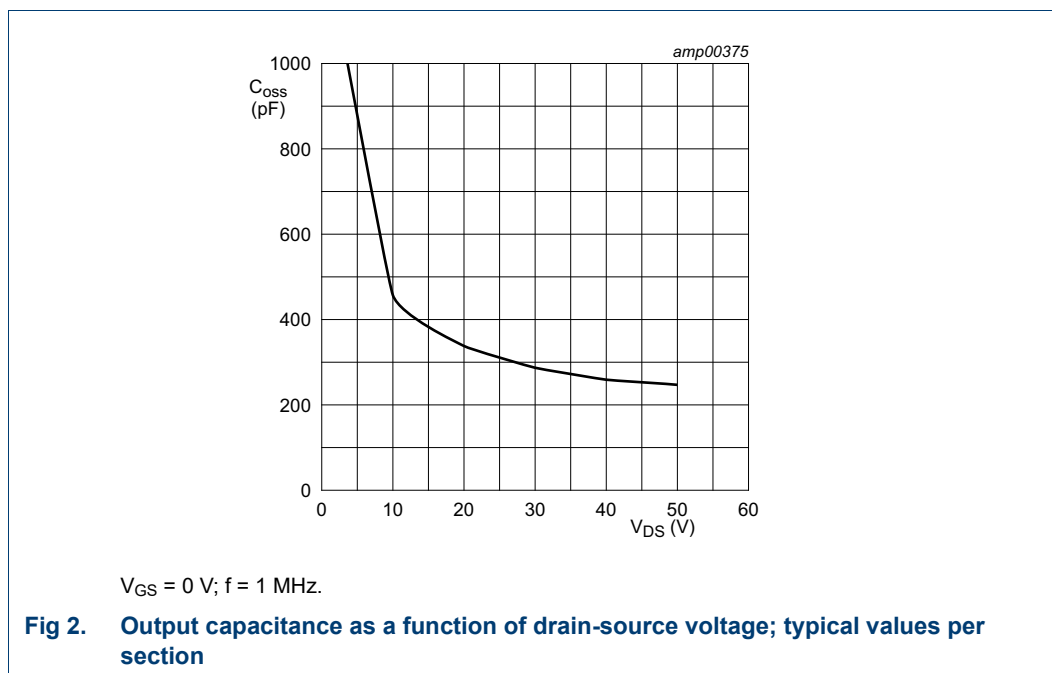
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	91	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 23.1\text{ A}$	-	0.066	-	$\Omega$

**Table 7. AC characteristics**  
 $T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	4.9	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	650	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	247	-	pF

**Table 8. RF characteristics**  
 Test signal: pulsed RF;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\%$ ;  $f = 108\text{ MHz}$ ; RF performance at  $V_{DS} = 50\text{ V}$ ;  
 $I_{Dq} = 150\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 1700\text{ W}$	24.5	26.2	-	dB
$RL_{in}$	input return loss	$P_L = 1700\text{ W}$	-	-14	-	dB
$\eta_D$	drain efficiency	$P_L = 1700\text{ W}$	71	74	-	%



## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF189XRA and BLF189XRAS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions:  $V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 150\text{ mA}$ ;  $P_L = 1700\text{ W}$  pulsed;  $f = 108\text{ MHz}$ .

### 7.2 Impedance information

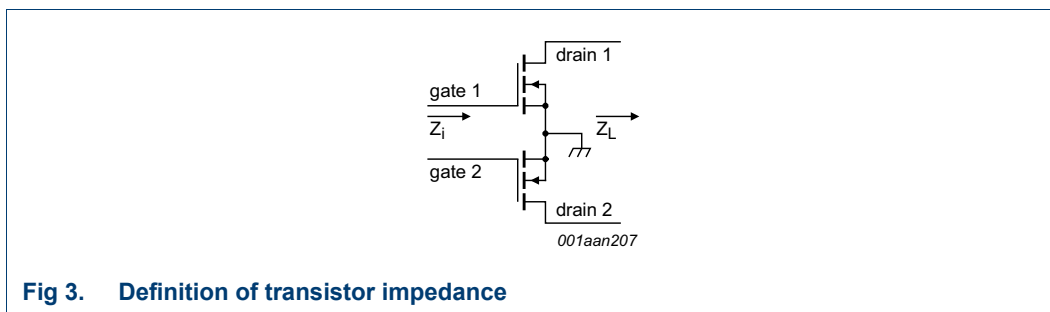


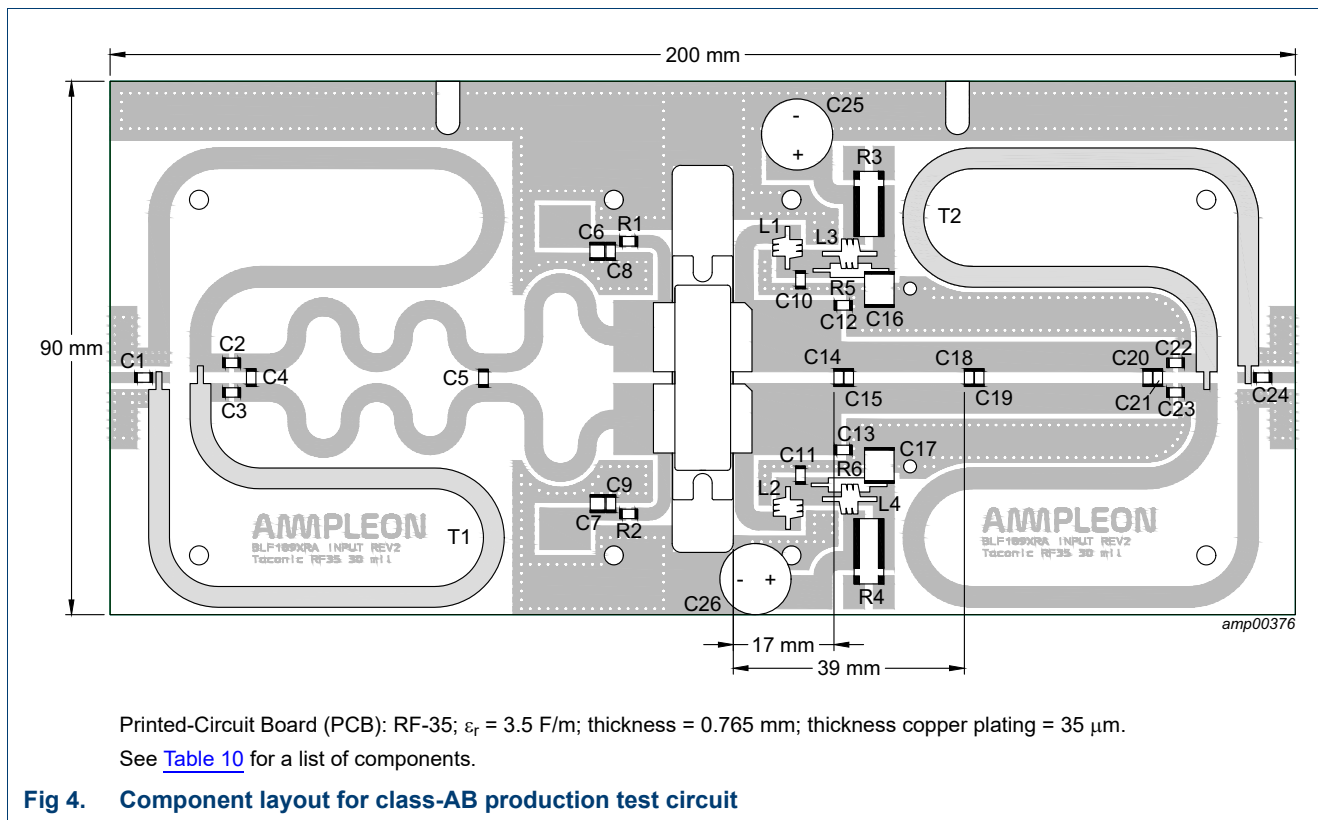
Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated  $Z_i$  and  $Z_L$  device impedance; impedance info at  $V_{DS} = 50\text{ V}$  and  $P_L = 1700\text{ W}$ .

f	$Z_i$	$Z_L$
(MHz)	( $\Omega$ )	( $\Omega$ )
108	$2.3 - j7.6$	$2.3 + j0.4$

7.3 Test circuit



**Table 10. List of components**

For test circuit see [Figure 4](#).

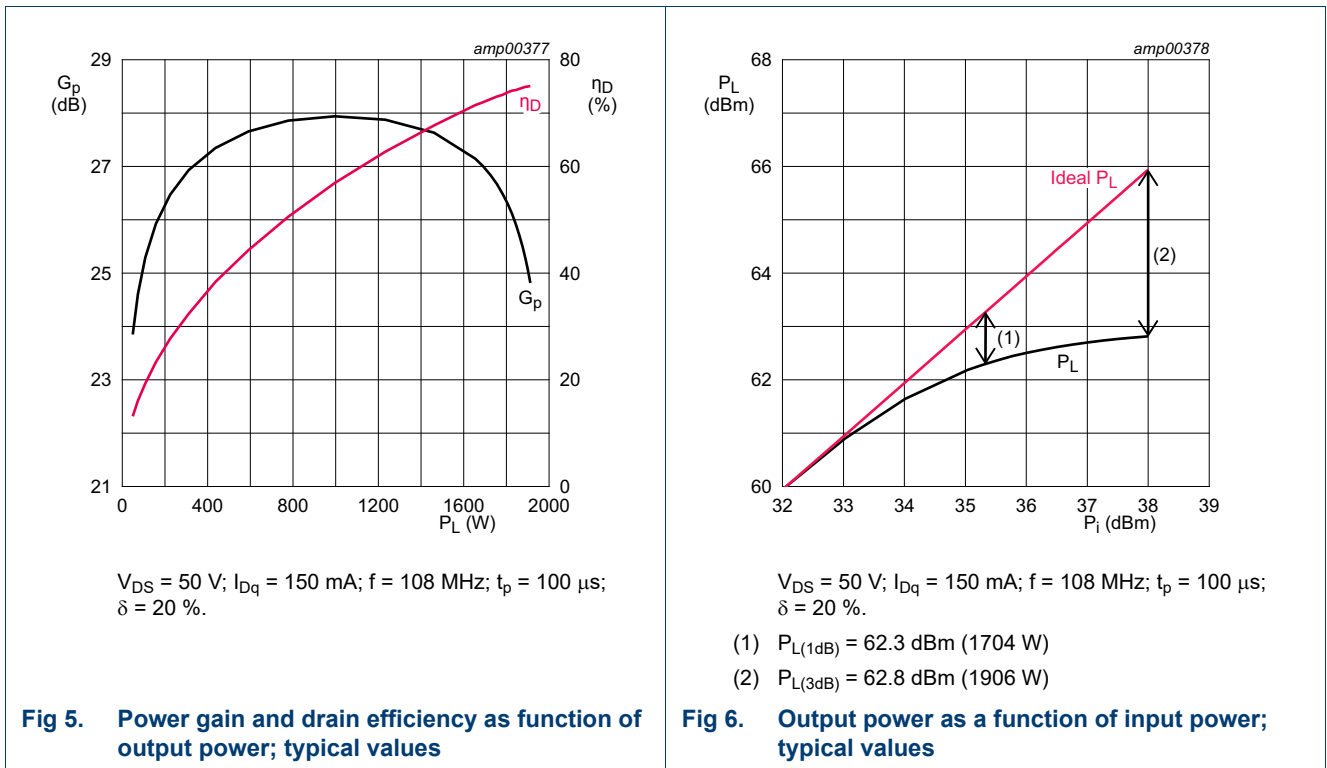
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	470 pF	[1]
C2, C3	multilayer ceramic chip capacitor	68 pF	[1]
C4	multilayer ceramic chip capacitor	51 pF	[1]
C5	multilayer ceramic chip capacitor	300 pF	[1]
C6, C7	multilayer ceramic chip capacitor	4.7 $\mu$ F, 50 V	
C8, C9	multilayer ceramic chip capacitor	920 pF	[1]
C10, C11	multilayer ceramic chip capacitor	920 pF	[1]
C12, C13	multilayer ceramic chip capacitor	180 pF	[1]
C14, C15	multilayer ceramic chip capacitor	91 pF	[1]
C16, C17	multilayer ceramic chip capacitor	4.7 $\mu$ F, 100 V	
C18, C19	multilayer ceramic chip capacitor	56 pF	[1]
C20, C21	multilayer ceramic chip capacitor	51 pF	[1]
C22, C23	multilayer ceramic chip capacitor	100 pF	[1]
C24	multilayer ceramic chip capacitor	470 pF	[1]
C25, C26	electrolytic capacitor	2200 $\mu$ F, 64 V	
L1, L2	air inductor	3 turns, D = 4 mm, d = 1 mm	1 mm copper wire

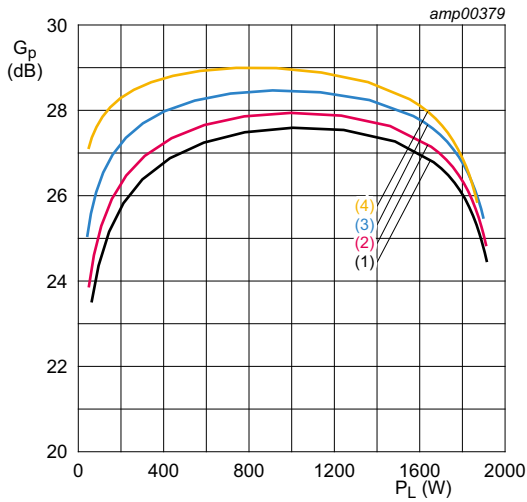
**Table 10. List of components ...continued**  
For test circuit see [Figure 4](#).

Component	Description	Value	Remarks
L3, L4	air inductor	5 turns, D = 4 mm, d = 1 mm	1 mm copper wire
R1, R2	resistor	4.7 kΩ	SMD 1206
R3, R4	resistor	0.01 Ω	FC4L110R010FER
R5, R6	resistor	4.7 Ω, 0.6 W	SMD 1206
T1, T2	semi rigid coax	50 Ω, 160 mm	EZ141-AL-TP/M17

[1] American Technical Ceramics type 100B or capacitor of same quality

### 7.4 Graphical data

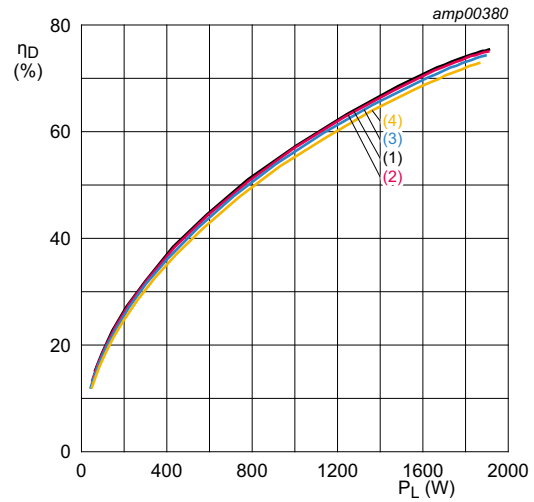




$V_{DS} = 50\text{ V}$ ;  $f = 108\text{ MHz}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\text{ }\%$ .

- (1)  $I_{Dq} = 50\text{ mA}$
- (2)  $I_{Dq} = 150\text{ mA}$
- (3)  $I_{Dq} = 600\text{ mA}$
- (4)  $I_{Dq} = 2000\text{ mA}$

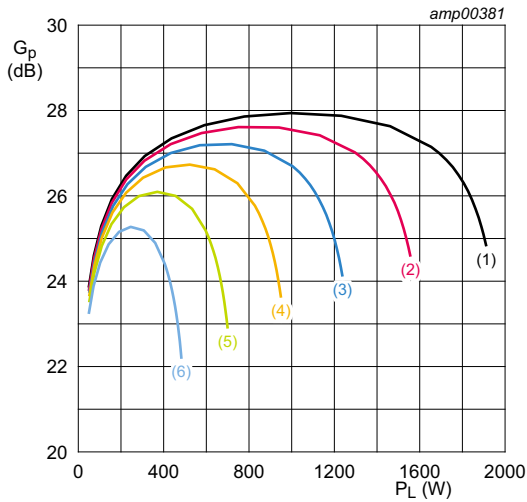
**Fig 7. Power gain as a function of output power; typical values**



$V_{DS} = 50\text{ V}$ ;  $f = 108\text{ MHz}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\text{ }\%$ .

- (1)  $I_{Dq} = 50\text{ mA}$
- (2)  $I_{Dq} = 150\text{ mA}$
- (3)  $I_{Dq} = 600\text{ mA}$
- (4)  $I_{Dq} = 2000\text{ mA}$

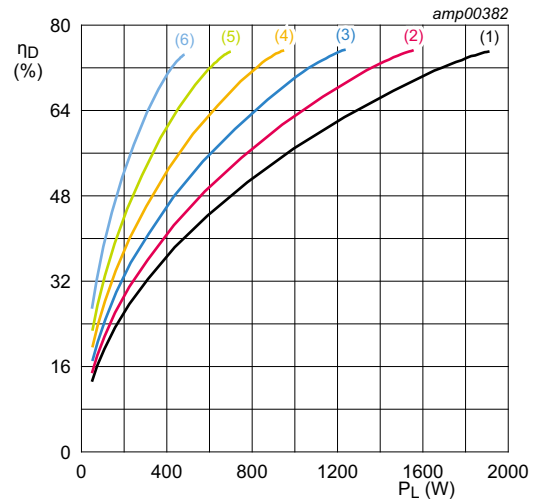
**Fig 8. Drain efficiency as a function of output power; typical values**



$I_{Dq} = 150\text{ mA}$ ;  $f = 108\text{ MHz}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\text{ }\%$ .

- (1)  $V_{DS} = 50\text{ V}$
- (2)  $V_{DS} = 45\text{ V}$
- (3)  $V_{DS} = 40\text{ V}$
- (4)  $V_{DS} = 35\text{ V}$
- (5)  $V_{DS} = 30\text{ V}$
- (6)  $V_{DS} = 25\text{ V}$

**Fig 9. Power gain as a function of output power; typical values**



$I_{Dq} = 150\text{ mA}$ ;  $f = 108\text{ MHz}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\text{ }\%$ .

- (1)  $V_{DS} = 50\text{ V}$
- (2)  $V_{DS} = 45\text{ V}$
- (3)  $V_{DS} = 40\text{ V}$
- (4)  $V_{DS} = 35\text{ V}$
- (5)  $V_{DS} = 30\text{ V}$
- (6)  $V_{DS} = 25\text{ V}$

**Fig 10. Drain efficiency as a function of output power; typical values**



8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

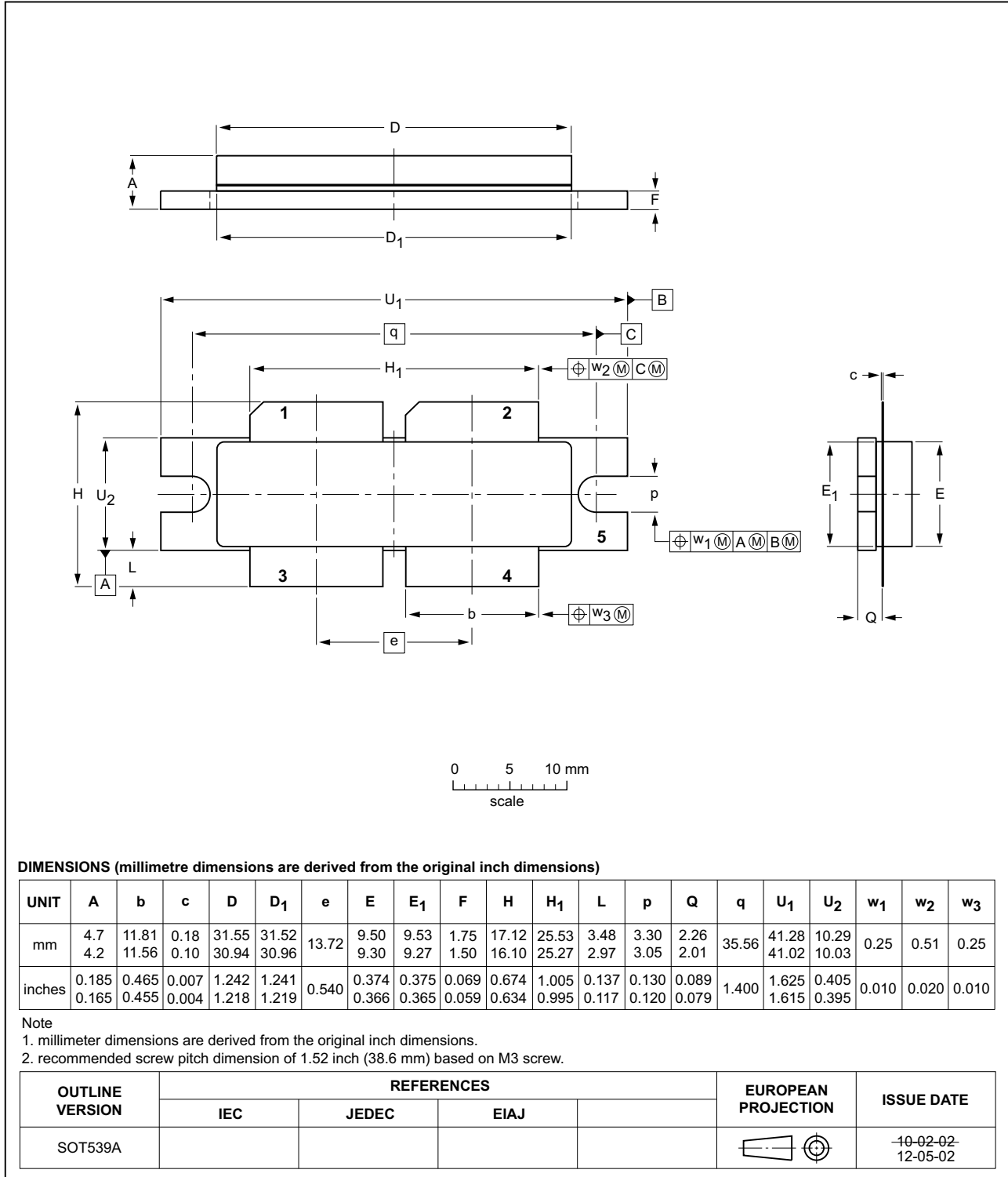


Fig 11. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

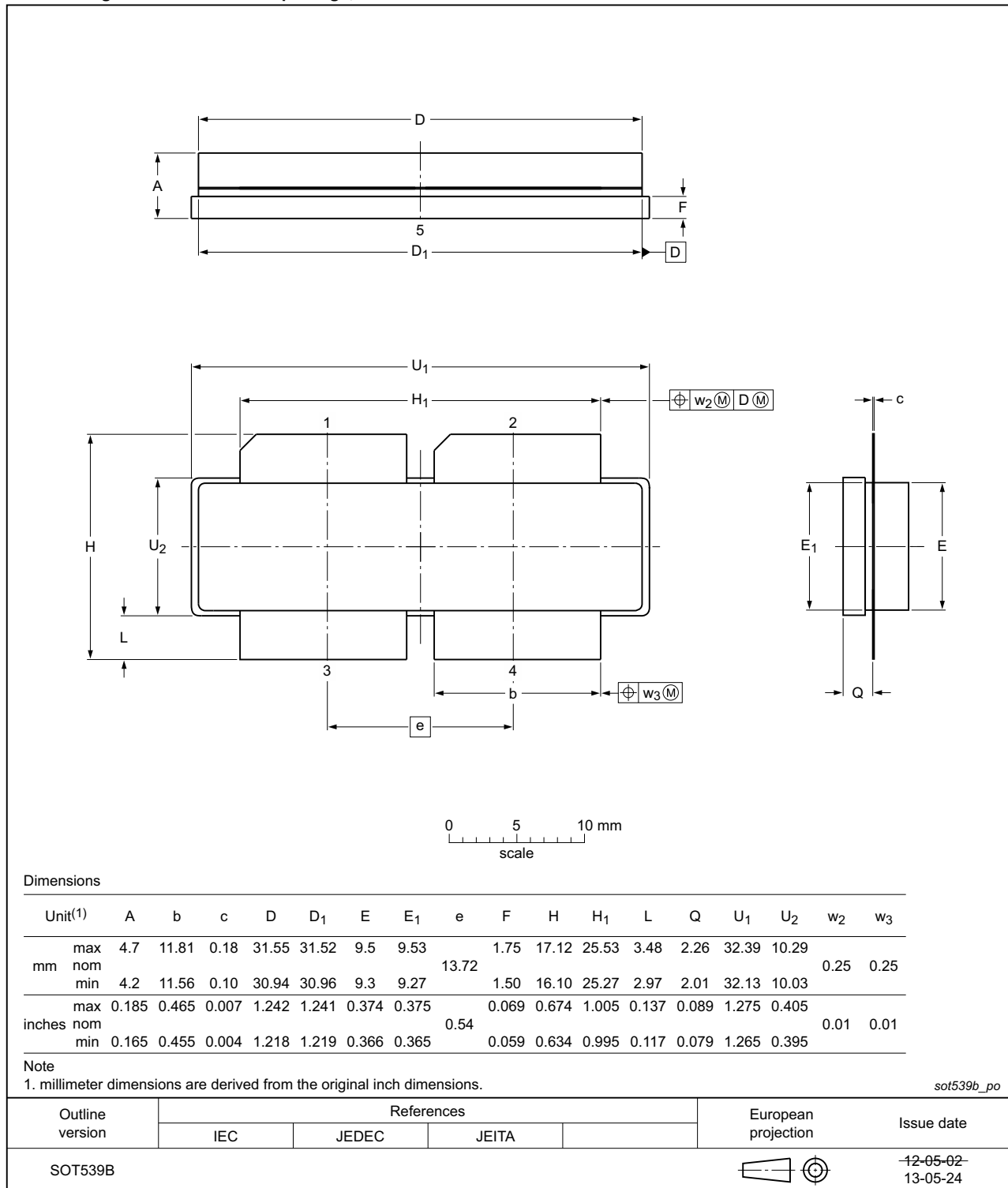


Fig 12. Package outline SOT539B

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 11. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 12. Abbreviations**

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

**Table 13. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF189XRA_BLF189XRAS v.1	20171106	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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