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June 2014

FDMC86261P

P-Channel PowerTrench® MOSFET
-150 V, -9 A, 160 mΩ

Features

- Max $r_{DS(on)}$ = 160 mΩ at V_{GS} = -10 V, I_D = -2.4 A
- Max $r_{DS(on)}$ = 185 mΩ at V_{GS} = -6 V, I_D = -2.2 A
- Very low RDS-on mid voltage P channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant

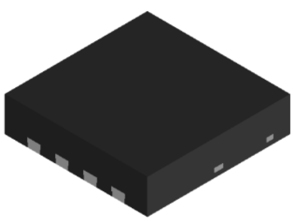
General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

Applications

- Active Clamp Switch
- Load Switch

Top



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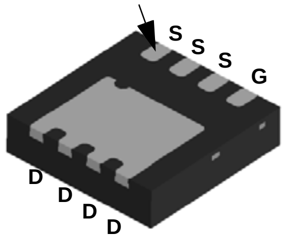
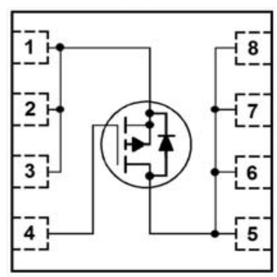




MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-150	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous	T_C = 25 °C		-9	A
	-Continuous	T_A = 25 °C	(Note 1a)	-2.7	
	-Pulsed			-20	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
P_D	Power Dissipation	T_C = 25 °C		40	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to + 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

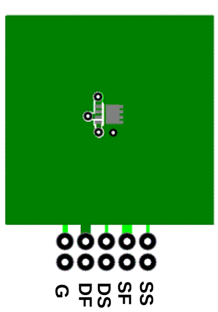
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86261P	FDMC86261P	Power 33	13''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

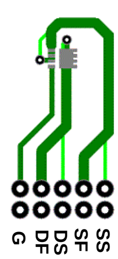
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-132		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-2	-3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -2.4 A		130	160	mΩ
		V_{GS} = -6 V, I_D = -2.2 A		141	185	
		V_{GS} = -10 V, I_D = -2.4 A, T_J = 125 °C		218	269	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.4 A		9		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -75 V, V_{GS} = 0 V, f = 1 MHz		1021	1360	pF
C_{oss}	Output Capacitance			87	120	pF
C_{rss}	Reverse Transfer Capacitance			4.7	10	pF
R_g	Gate Resistance		0.1	1.7	3.4	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75 V, I_D = -2.4 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Rise Time			2.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			9.2	20	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -75 V, I_D = -2.4 A		17	24	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -6 V		11	16	nC
Q_{gs}	Total Gate Charge			4.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.4 A (Note 2)		-0.81	-1.3	V
		V_{GS} = 0 V, I_S = -1.9 A (Note 2)		-0.80	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -2.4 A, di/dt = 100 A/μs		81	130	ns
Q_{rr}	Reverse Recovery Charge			197	315	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -9 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -28 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

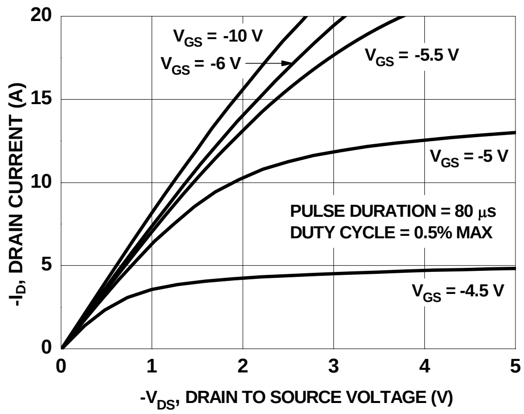


Figure 1. On Region Characteristics

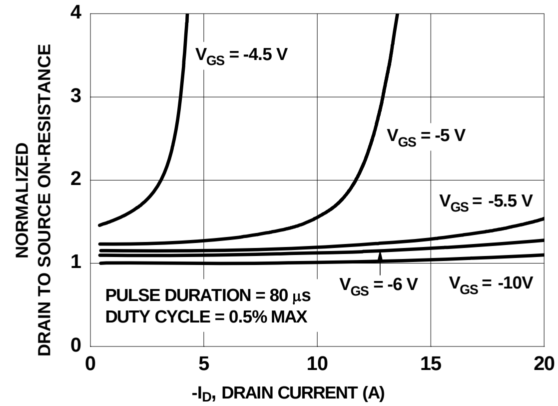


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

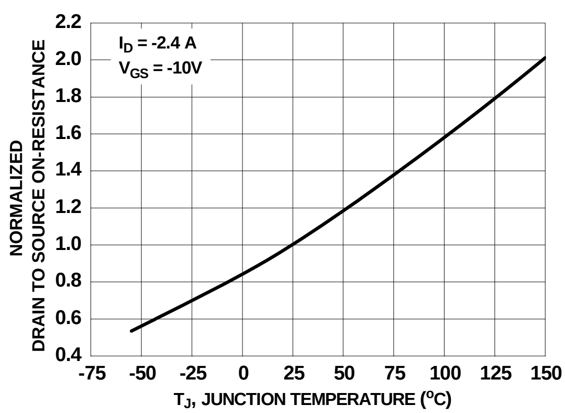


Figure 3. Normalized On Resistance vs Junction Temperature

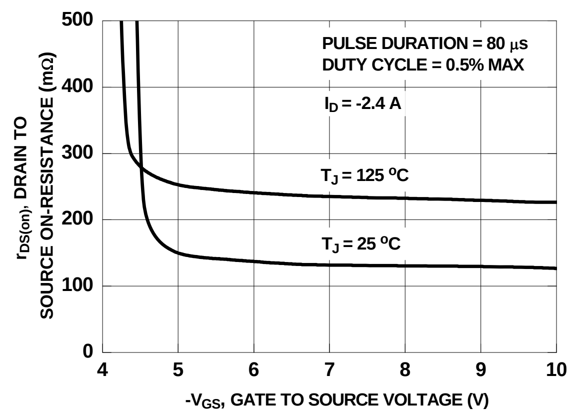


Figure 4. On-Resistance vs Gate to Source Voltage

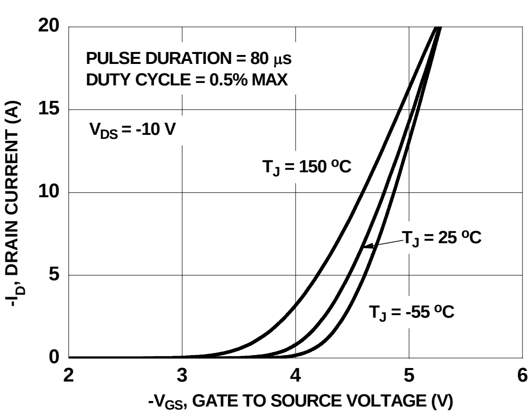


Figure 5. Transfer Characteristics

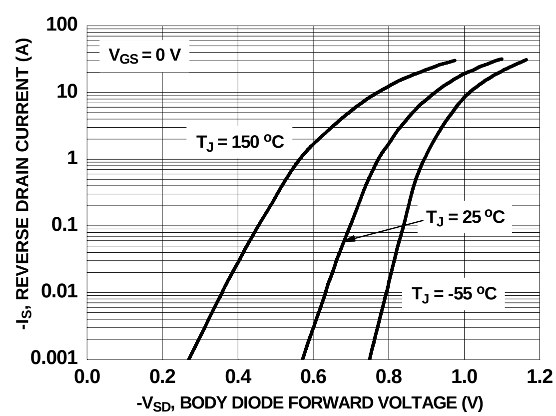


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

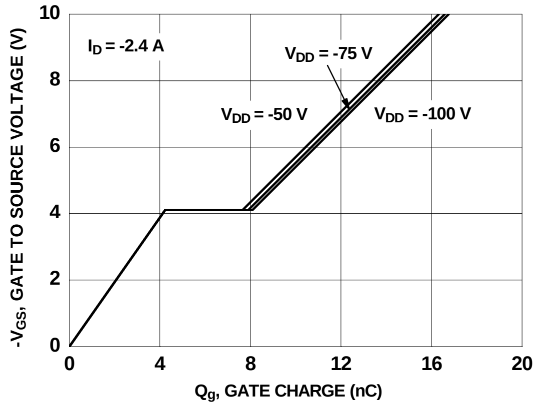


Figure 7. Gate Charge Characteristics

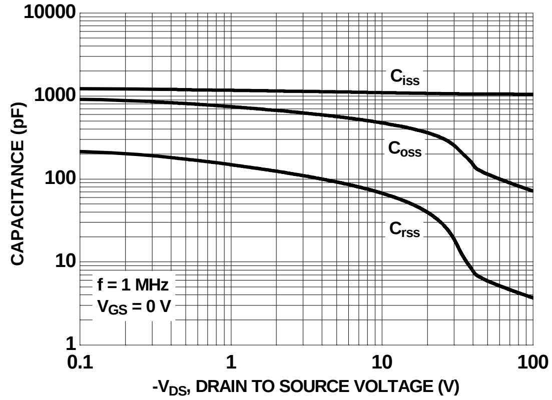


Figure 8. Capacitance vs Drain to Source Voltage

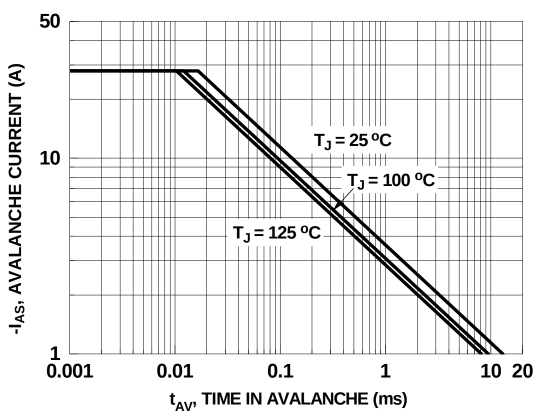


Figure 9. Unclamped Inductive Switching Capability

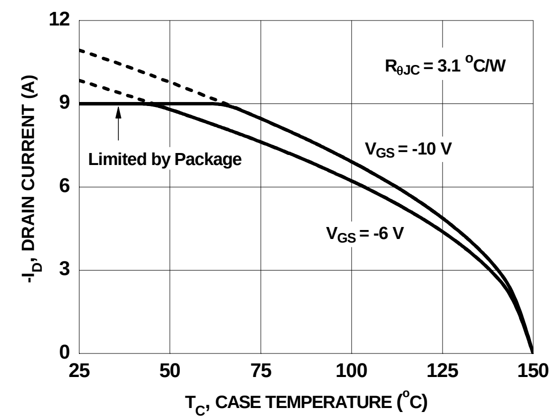


Figure 10. Maximum Continuous Drain Current vs Case Temperature

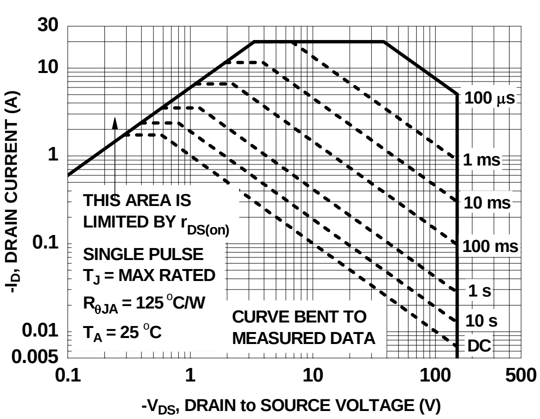


Figure 11. Forward Bias Safe Operating Area

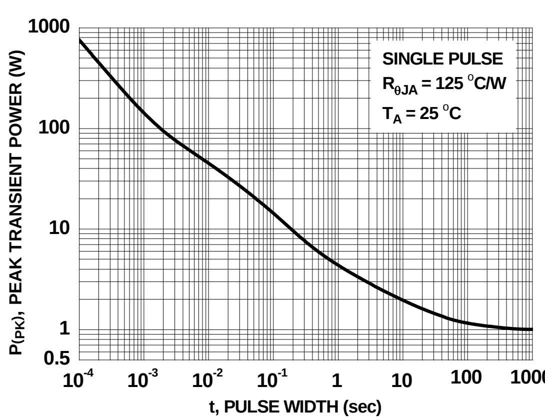


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

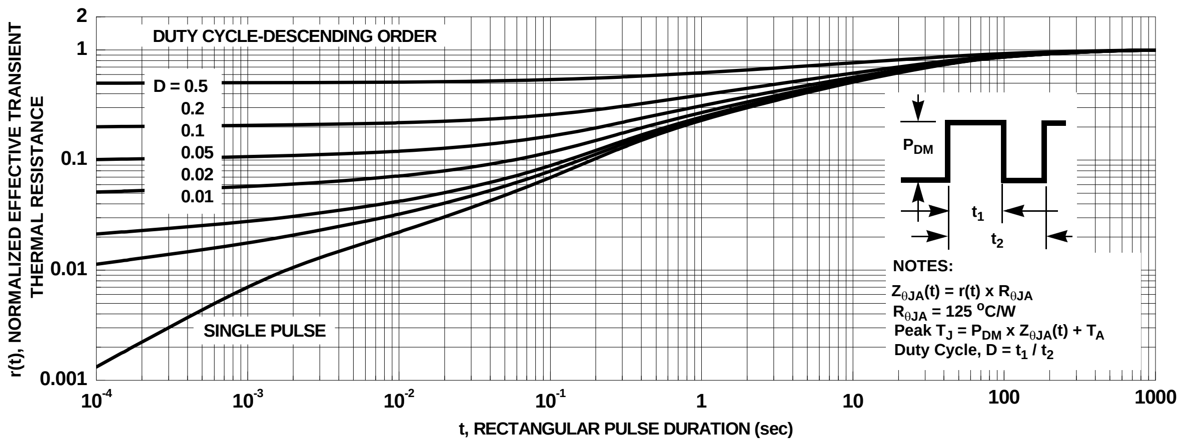
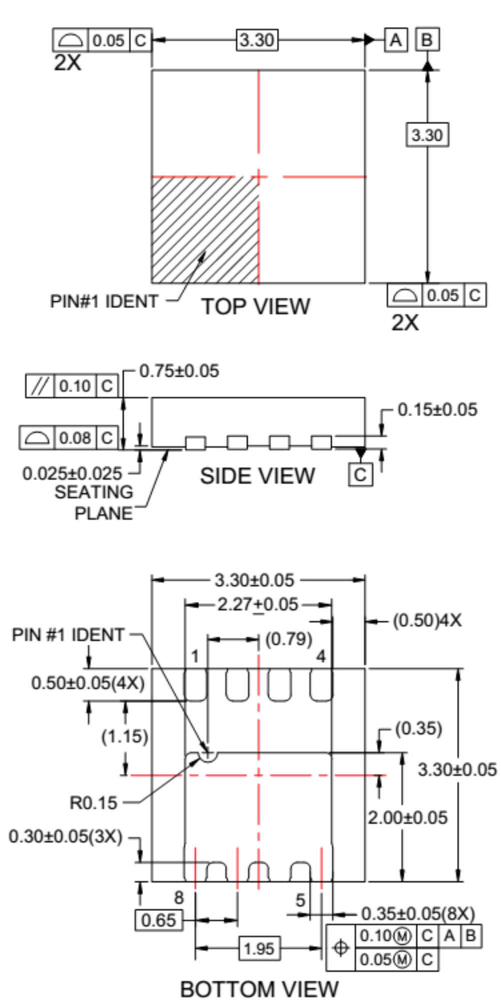
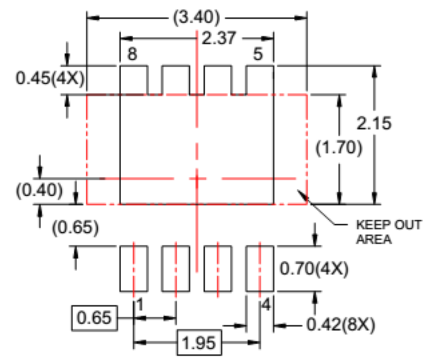


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout





RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I68

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