[MG2420] Datasheet

(No. ADS0701)

V1.2

REVISION HISTORY

Version	Date	Description
V1.0	2013.10.24	▪ First version release.
V1.1	2014.04.21	▪ Sec 4.1 - Temperature updated. ▪ Sec 5 - Application circuit is updated.
V1.2	2014.09.01	▪ Sec 4.8 - Crystal Oscillator parameters (TYP and MAX value for ESR, C_O and C_L) are updated. ▪ Sec 5 - Table 3. Bill of Materials is updated. C_{11} and C_{12} is changed from 30pF to 13pF.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

MG2420 is a low-power 2.4GHz IEEE 802.15.4 and ZigBee compliant radio transceiver. Operation frequency of MG2420 covers an ISM band of 2.4~2.48GHz. In addition to the standard data-rate specified in IEEE802.15.4, MG2420 provides enhanced multiple data rates with channel coding (1M~3Mbps).

MG2420 can be controlled by an external microcontroller, and its operations can be configured through a high speed Serial Peripheral Interface (SPI).

Ultra Low Power Consumption:
The current consumption of MG2420 is very low; which is 15.4 mA in Rx mode and 16.1 mA in Tx mode with output Power of 0 dBm. Utilization of higher data rate (~3Mbps) helps minimizing the time for transmission and reception, which leads to further reduction of power consumption.

Low Cost Solution:
MG2420 is a single chip RF transceiver, which includes RF front-end, VCO, PLL, and digital block including baseband modem, MAC, power management, and a high-speed SPI. It's packaged in compact 4x4mm package. Only small numbers of external components - RF matching network, crystal, bias resistor and antenna - are required as application circuit; this leads to the low cost solution.

Improved Interference Rejection and Longer Range:
MG2420 shows excellent interference rejection performance; it can receive wanted signal with the presence of interference from ZigBee or other communication devices (i.e. Wi-Fi or Bluetooth). It has a longer communication range based on high transmit power up to +9 dBm and high sensitivity of -97dBm at 250Kbps mode.

1.1. APPLICATIONS

- Home Automation and Security
- Automatic Meter Reading
- Factory Automation and Motor Control
- Energy Management
- Remote Keyless Entry with Acknowledgement
- Low Power Telemetry
- Health-care equipment
- PC peripherals
- Toys and Gaming peripherals
- Remote Controller for Consumer Electronics
- Audio and Video Applications

2. KEY FEATURES

2.1. RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low-power consumption
  - 15.4mA at RX mode
  - 16.1mA at TX mode with 0 dBm output
  - 28.4mA at TX mode with +9 dBm output
- High RX Sensitivity
  - -97dBm @ 250kbps (2Mcps Mode)
  - -93dBm @ 1Mbps (2Mcps Mode)
  - -90dBm @ 2Mbps (4Mcps Mode)
  - -86dBm @ 3Mbps (4Mcps Mode)
- No External T/R Switch and Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9 dBm
- Excellent TX EVM: 6% for 2Mcps mode, 8% for 4Mcps mode
- Direct Sequence Spread Spectrum
- MSK(O-QPSK) Modulation
- Channel coding with various rates of 1/2, 3/4
- Scalable Data Rate
  - 250kbps for IEEE 802.15.4 and ZigBee applications
  - 1Mbps for applications beyond IEEE 802.15.4 with RF bandwidth of 2MHz
  - 2~3Mbps for applications beyond IEEE 802.15.4 with RF bandwidth of 4MHz
- Digital RSSI Output
- Compliant to IEEE802.15.4

2.2. Integrated MAC

- Two 256-byte FIFOs
- FIFO management
- AES-128 Engine
- CRC-16 Computation and Check
- Automatic ACK transmission

2.3. Clock Inputs

- 32MHz Crystal for System Clock

2.4. Power

- 1.2V(Core)/1.8~3.6V(I/O) Operation
- Several On-chip Voltage Regulator for Analog part and Digital part separately.
- Power Supply Range for Internal Regulator(1.8V(Min) ~ 3.6V(Max))
- Power Management Scheme with Deep Sleep Mode Support; Current consumption under 1μA

2.5. Package

- Lead-Free/RoHS 28-pin QFN Package (4mm x4mm x 0.85mm)

3. PIN DESCRIPTION

MG2420 pin-out diagram and description are shown in [**Figure 1**] and [**Table 1**], respectively.

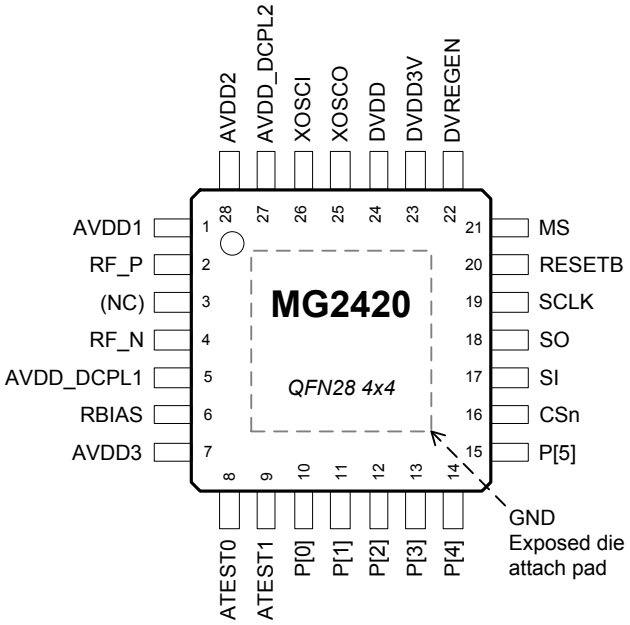


Figure 1. MG2420 Pin-out Diagram

Note: *The exposed die pad is located at the bottom of a chip and electrically connected to the die ground inside the package. It shall be soldered to ground on the board.*

Table 1. MG2420 Pin Description

Radio, Synthesizer, and Oscillator			
Pin	**Pin Name**	**Pin type**	**Pin Description**
2	RF_P	RF I/O	Positive RF input signal to LNA in RX mode. Positive RF output signal from PA in TX mode. It should be biased by AVDD_DCPL1. Refer to Figure 2 (Sec.5).
4	RF_N	RF I/O	Negative RF input signal to LNA in RX mode. Negative RF output signal from PA in TX mode. It should be biased by AVDD_DCPL1. Refer to Figure 2 (Sec.5).
6	RBIAS	Analog I/O	External precision bias resistor (510K) to generate the reference current.
25	XOSCO	Analog I/O	X-tal osc. buffer output or Crystal-unit pin-2
26	XOSCI	Analog I/O	X-tal osc. buffer input or Crystal-unit pin-1
1	AVDD1	Power I	1.8V to 3.6V RF/analog power supply connection
28	AVDD2	Power I	1.8V to 3.6V RF/analog power supply connection
7	AVDD3	Power I	1.8V to 3.6V RF/analog power supply connection
5	AVDD_DCPL1	Power O	Regulated Output of AVDD1 for PA bias
27	AVDD_DCPL2	Power O	Regulated Output of AVDD2 for decoupling
8	ATEST0	Analog O	Analog Temperature sensor output Analog test signal output
9	ATEST1	Analog O	Analog test signal output
Digital			

Pin	Pin Name	Pin type	Pin Description
19	SCLK	Digital I	SPI Interface: Serial Clock.
18	SO	Digital O	SPI Interface: Serial Out
17	SI	Digital I	SPI Interface: Serial In
16	CSn	Digital I	SPI Interface: Chip Select. Active low.
20	RESETB	Digital I	External reset. Active low.
10	P[0]	Digital I/O	General purpose digital I/O. Typical usage is setting to output mode to interface with MCU. When the SIGNAL_OUT (0x2F6[6:4]) sets to 0x2, P[0]~P[5] are assigned to TRSW, nTRSW, IRQ, CRCOK, PLL_LOCK and EXTCLK, respectively; for details, refer to Sec.7.4 and Sec.9.3.
11	P[1]	Digital I/O	
12	P[2]	Digital I/O	
13	P[3]	Digital I/O	
14	P[4]	Digital I/O	
15	P[5]	Digital I/O	
22	DVREGEN	Digital I	Digital VREG enable input. When high, digital voltage regulator is active.
24	DVDD	Power O	Regulated Output of DVDD3V for decoupling
23	DVDD3V	Power I	1.8V to 3.6V digital power supply connection
21	MS	Digital I	NC(Not Connected)
Ground and NC			
Pin	**Pin Name**	**Pin type**	**Pin Description**
Exposed bottom	GND	Ground	Ground for RF, analog, digital core, and IO
3	NC		NC It can be connected to GND.

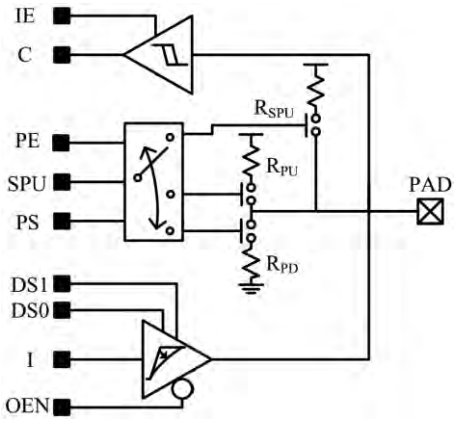
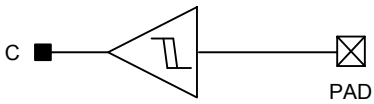
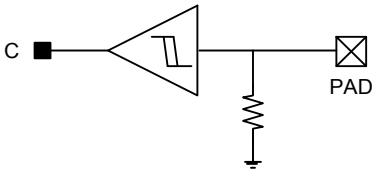
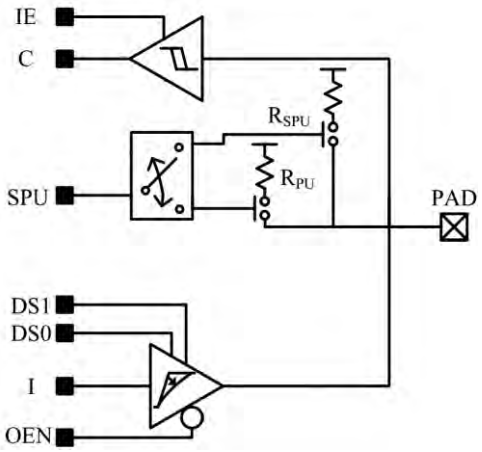
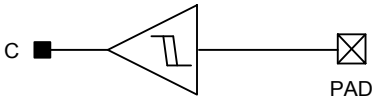
RF_P and RF_N are the differential RF input/output ports. The balun and impedance matching circuits are required to interface a single-ended 50-Ohm antenna.

There are 4 pins connected to 3.0V supply, which is applied to internal voltage regulators. And there are 3 output pins of the regulated 1.2V voltages for decoupling. These regulated outputs should not be used to supply power to external circuits. DVDD is the output of the internal digital regulator which is controlled by the DVREGEN pin. Other analog voltage regulators are controlled by the power management block and activated by the power mode.

SCLK, SO, SI, and CSn are used in slave SPI interface. RESETB is an external reset input with active low.

The exposed die pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It shall be soldered to the board ground.

Table 2. I/O Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIO (P[5:0])		
	Input with pull-up	Refer to Sec.7.4. In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
SCLK, SI, CSn, RESETB		
	Input with HiZ	In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
MS		
	Input with pull-down	In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
SO		
	Input with pull-up	Output @ CSn=low Otherwise, input with pull-up In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
DVREGEN		
	Input	

4. ELECTRICAL CHARACTERISTICS

4.1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DDIO}	Digital I/O supply voltage	-0.3 to 3.6	V
V_{DDA}	Analog supply voltage	-0.3 to 3.6	V
V_{DD12}	Regulated output voltage on pins 5, 24, 27	-0.3 to 1.32	V
T_{STG}	Storage Temperature	-40 to 150	°C
ESD	HBM MM CDM	2000 200 750	V

Stress exceeding one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only. And functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL CHARACTERISTICS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE1: All voltage values are based on V_{SS} and V_{SSIO}.
NOTE2: These values were obtained under worst-case test conditions specially prepared for MG2420 and these conditions are not sustained in normal operation environment.

CAUTION: *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

4.2. Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	Digital I/O supply voltage (DVDD3V)	1.8	3.0	3.6	V
V_{DDA}	Analog supply voltage on pins 1, 7, 28	1.8	3.0	3.6	V
T_{OP}	Operating temperature range	-40		85	°C

4.3. Digital I/O DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	I/O supply voltage(DVDD3V)	1.8	3.0	3.6	V
AGND	Chip ground		0		V
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{OH}	Output high voltage	2.4			V
V_{OL}	Output low voltage			0.4	V
R_{PU}	Pull-up Resistance		66		kΩ
R_{PD}	Pull-down Resistance		66		kΩ
R_{SPU}	Strong Pull-up Resistance DVDD3V=3.3V	1.42	1.62	1.92	kΩ

4.4. Current Consumption

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz, Data rate=250Kbps

Parameter	MIN	TYP	MAX	UNIT	Note
TX Mode @+9dBm Output Power @+8dBm Output Power @+7dBm Output Power @+6dBm Output Power @+5dBm Output Power @+4dBm Output Power @+3dBm Output Power @+2dBm Output Power @+1dBm Output Power @ 0dBm Output Power		 28.4 24.7 22.1 21.1 20.5 19.1 18.5 17.4 16.4 16.1		mA	Measured at 2450MHz Channel AES, Peripheral, and Temp. Sensor Disabled
RX Mode		15.4		mA	AES, Peripheral, and Temp. Sensor Disabled
Deep Sleep Mode			1	μA	DVREGEN=0
Analog Temperature Sensor		0.06		mA	Current consumption increases at using this

4.5. RF Receive Section

4.5.1. Chip Rate of 2Mcps (RF Bandwidth: 2MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
RF Frequency Range (Center Frequency)	2405		2480	MHz	
Maximum Input Level 1000 kbps 250 kbps		 -3.7 -2		dBm	PER≤1% Packet length of 20-byte
Spurious Radiation 30-1000 MHz 1-12.75 GHz		 -60 -60		dBm	Compiles with EN 300 328, EN 300 400, FCC, and ARIB STD-T66.
Received RF Bandwidth (Chip Rate)		2		MHz	
Channel Spacing		5		MHz	Compiles with IEEE 802.15.4
Receiver Sensitivity 1000 kbps 250 kbps		 -93 -97		dBm	PER≤1% Packet length of 20-byte
Adjacent Channel Rejection +5MHz -5MHz		 30 31		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Adjacent Channel Rejection +5MHz -5MHz		 48 49		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +10MHz -10MHz		 53 56		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +10MHz -10MHz		 58 59		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Filtered IEEE 802.15.4 interferer signal
Others Channel Rejection ≥ +15MHz ≥ -15MHz		 65 65		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Co-channel Rejection		-6.6		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Wi-Fi IEEE 802.11n Rejection		47		dB	250Kbps, 40-byte WANTED Signal -82dBm, Interference 802.11n (BW40MHz) +27/-27Mhz

Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -20 -23 -23 -25 -23 -23		dBm	250kbps, 20-byte P_{RF} = sensitivity+3 ETSI EN 300 440-1 V1.6.1 (2010-04)-37[2] blocking/desensitization

4.5.2. Chip Rate of 4Mcps (RF Bandwidth: 4MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
RF Frequency Range (Center Frequency)	2405		2480	MHz	
Maximum Input Level 3000 kbps 2000 kbps		 2.3 -0.2		dBm	PER≤1% Packet length of 20-byte
Spurious Radiation 30-1000 MHz 1-12.75 GHz		 -60 -60		dBm	Compiles with EN 300 328, EN 300 400, FCC, and ARIB STD-T66.
Received RF Bandwidth (Chip Rate)		4		MHz	
Channel Spacing		10		MHz	Recommended.
Receiver Sensitivity 3000 kbps 2000 kbps		 -86 -90		dBm	PER≤1% Packet length of 20-byte
Adjacent Channel Rejection +10MHz -10MHz		 41 41		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +20MHz -20MHz		 60 61		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Others Channel Rejection ≥ +30MHz ≥ -30MHz		 61 62		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Co-channel Rejection		-6		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal

Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -24 -28 -28 -29 -28 -27		dBm	2Mbps, 20-byte [2] P_{RF} = sensitivity+3

4.6. RF Transmit Section

4.6.1. Chip Rate of 2Mcps (RF Bandwidth: 2MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Transmit Chip Rate		2		Mcps	
TX Output Power		9		dBm	Using the recommended matching circuit
Error Vector Magnitude (EVM)		6		%	
Harmonics 2nd harmonic 3rd harmonic		 -45 -45		dBm	Using the recommended matching circuit
Spurious Emission 30Hz~1GHz 1GHz~2.5GHz 2.5GHz~12.7GHz 5.15~5.3GHz		 -60 -60 -60 -60		dBm	Complies with EN 300 440, FCC, and ARIB STD-T66.

4.6.2. Chip Rate of 4Mcps (RF Bandwidth: 4MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Transmit Chip Rate		4		Mcps	
TX Output Power		9		dBm	Using the recommended matching circuit
Error Vector Magnitude (EVM)		8		%	
Harmonics 2nd harmonic 3rd harmonic		 -45 -45		dBm	Using the recommended matching circuit
Spurious Emission 30Hz~1GHz 1GHz~2.5GHz 2.5GHz~12.7GHz 5.15~5.3GHz		 -60 -60 -60 -60		dBm	Complies with EN 300 440, FCC, and ARIB STD-T66.

4.7. Frequency Synthesizer Characteristics

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Phase Noise @ 100KHz offset @ 1MHz offset @ 2MHz offset @ 3MHz offset @ 5MHz offset @ 10MHz offset @ 50MHz offset		 -82.2 -110.3 -117.0 -119.5 -123.3 -134.0 -149.0		dBc/Hz	
PLL Lock Time			80	μsec	

4.8. Crystal Oscillator

Parameter	MIN	TYP	MAX	UNIT	Note
Crystal Oscillator Frequency		32		MHz	
Crystal Frequency Accuracy Requirement	-40		+40	ppm	
Equivalent series resistance (ESR)		30[1]	60[2]	Ω	
Crystal shunt capacitance (C_O)		3	5	pF	
Crystal load capacitance (C_L)		9[1]	13[2]	pF	
Start-up time			0.8	ms	

4.9. Analog Temperature Sensor

Test Conditions: V_{DDA}=V_{DDIO}=3.0V

Parameter	MIN	TYP	MAX	UNIT	Note
Output voltage at -40°C		0.8276		V	
Output voltage at 0°C		0.7709		V	
Output voltage at +27°C		0.7322		V	
Output voltage at +85°C		0.6463		V	
Temperature coefficient		-1.4526		mV/°C	Linear fitted from -40°C to 85°C
Current consumption		0.06		mA	

[1] The negative resistance of driving circuit is five times larger than the ESR of crystal oscillator with crystal satisfying above TYP conditions.
[2] The negative resistance of driving circuit is two times larger than the ESR of crystal oscillator with crystal satisfying above MAX conditions.

5. APPLICATION

A typical application diagram of MG2420 is shown in [Figure 2]. A few external components are required as shown in the figure. [Table 3] describes the external components and lists their typical values.

The inductor, L1 is used as an RF matching and as an output load of the PA(power amplifier) simultaneously. The components near the RF_P/RF_N pins, L2, L3, C2, and C3 form a balun which converts the differential RF signals to a single-ended RF signal. L4, C4, and C5 form an LC harmonic filter to suppress the TX output harmonics. In addition, C4 is used for DC blocking. All together with adequate values, they also transform the impedance to match a 50-Ohm antenna.

As shown in [Figure 2], RF_P and RF_N are biased by AVDD_DCPL1 through L1 and L3.

The 32MHz crystal with loading capacitors is connected to MG2420. It provides the reference frequency source for MG2420.

CD1, CD2, and CD3 are supply decoupling capacitors, whose values depend on PCB artwork and stack-up information.

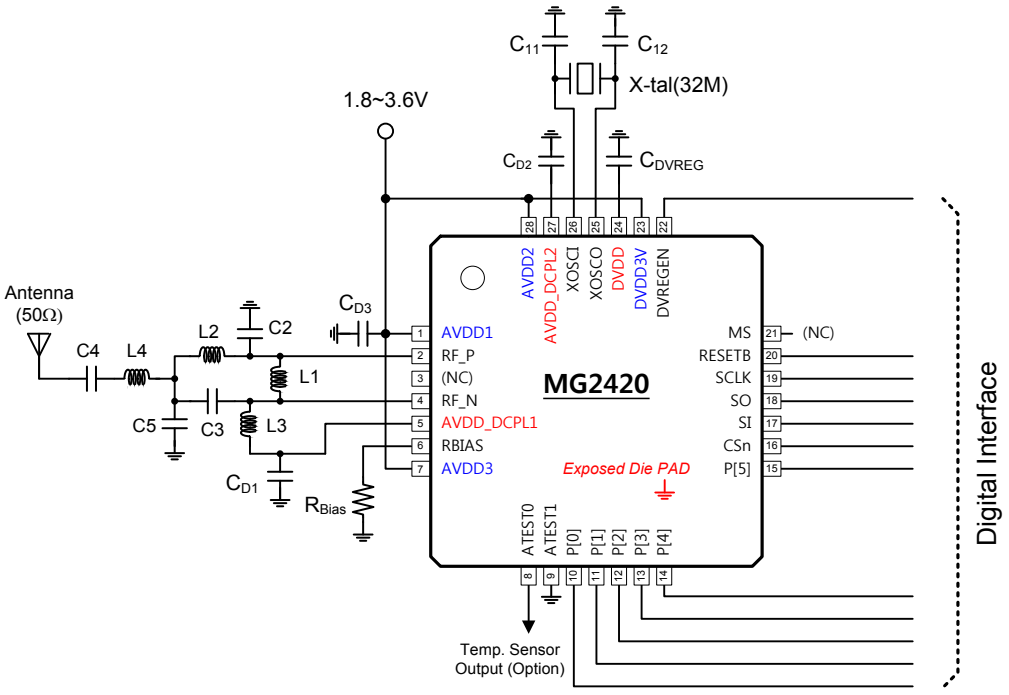


Figure 2. MG2420 Application Circuit

Table 3. Bill of Materials for Figure 2

No	Component	Description	Value
1	L1	RF matching inductor	5.1nH
2	L2, L3	RF balun inductors	2.4nH
3	C2	RF balun capacitor	1.2pF
4	C3	RF balun capacitor	1.0pF
5	L4	RF LC filter/matching inductor	3.9nH
6	C5	RF LC filter/matching capacitor	1.5pF
7	C4	DC blocking capacitor	1.0pF
8	Rbias	Resistor for internal bias current reference	510KΩ
9	X-tal	32MHz crystal unit	32M (±40ppm, 16pF)
10	C11, C12	Crystal loading capacitors	13pF[3]
11	C_{DVREG}	Decoupling capacitor for DVDD (digital voltage regulator output)	1uF
12	C_{D1}	Decoupling capacitor for AVDD_DCPL1	1nF
13	C_{D2}	Decoupling capacitor for AVDD_DCPL2	1uF
14	C_{D3}	Decoupling capacitor for AVDD1	1uF

[3] The value of crystal loading capacitance depends on crystal oscillator.

6. FUNCTIONAL DESCRIPTION

6.1. Block Diagram

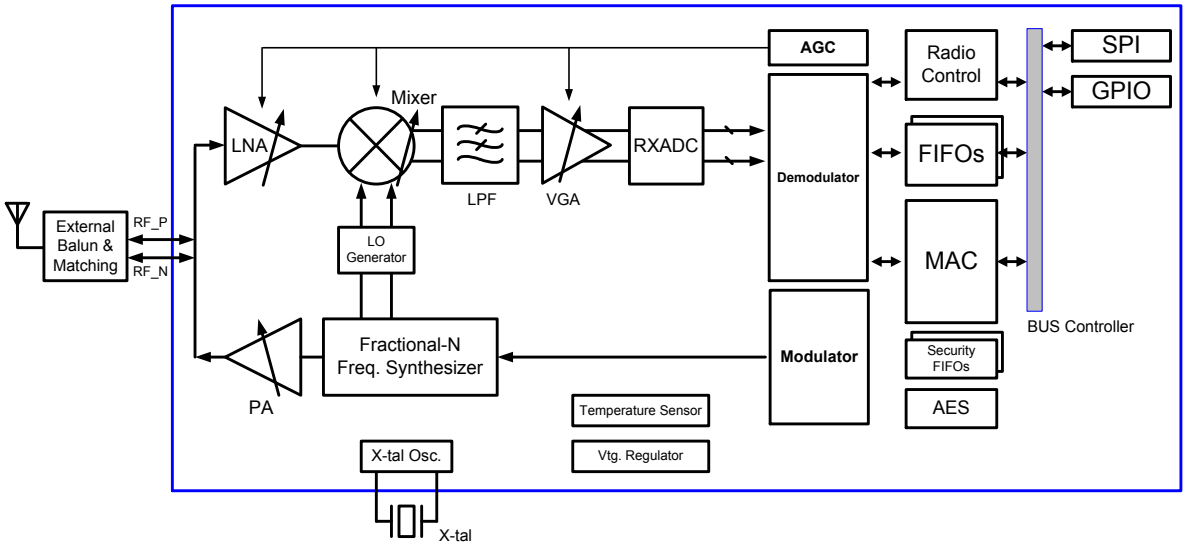


Figure 3. MG2420 block diagram.

A simplified block diagram of MG2420 is shown in [Figure 3]. Since the bidirectional differential RF pins are used for RX and TX, no external T/R switch is required. The receiver is designed with direct-conversion architecture, and it operates in the 2.4GHz band with excellent receiver sensitivity and robustness to interfererence. Transmitter architecture is based on direct-modulation technique using direct RF frequency synthesis.

The LNA amplifies the received RF signal at RF_P and RF_N pins, and the RX Mixer converts the RF signal to the baseband frequency in quadrature(I and Q). Gains of LNA and mixer are controlled coarsely by AGC block.

Channel filtering occurs in the LPF(low-pass filter). The VGA(variable-gain amplifier) provides sufficient gain, controlled by the AGC, to drive the RXADC(analog-to-digital converter). And, the RX ADC converts the VGA output signals to the signed binary digital signals.

The frequency synthesizer (PLL) generates the carrier signals for channel frequency.

The LO generator transforms the differential outputs of the PLL into the quadrature(I, Q) signals required for local signals in the RX Mixer.

The PA(power amplifier) amplifies the modulated RF signal from the PLL. TX output power level is controlled in the PA by register setting.

The modulator transforms the raw data came from TX FIFO into the modulated signals. It consists of the bit-to-symbol mapping block, the spreading block, the convolution encoder, the interleaver, and the mapping circuit for direct-modulation.

The demodulator processes the digitized RX signals of the ADC outputs, which store the RX

FIFO after processing correlation, frequency offset control, timing synchronization, deinterleaver, and viterbi decoder.

The AGC(automatic gain controller) controls gains of RF circuits to maintain the input level of the RXADC.

The functions of the MAC are to transfer the data from higher layer to PHY block, to send the received data from PHY to higher layer, and to encrypt/decrypt the data in the AES.

The Radio Controller module controls the operation state, the FIFOs, power up/down of RF/Analog blocks, and clock on/off of modem sub blocks. It provides operating sequences for both transmit and receive. Also it controls the sleep mode.

The X-tal oscillator generates a reference clock for RF and digital blocks.

Several voltage regulators are integrated to provide the operating voltage for analog and digital blocks.

An SPI serial interface is used for radio configuration and packet handling. GPIO pins are typically used for microcontroller interface.

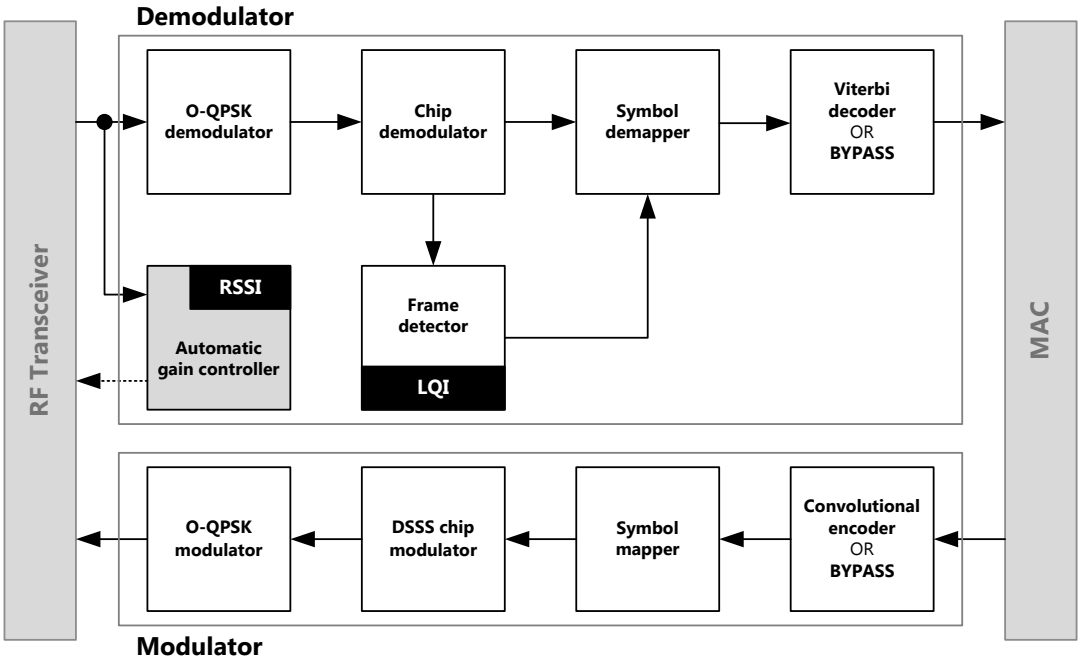


Figure 4. Baseband PHY block diagram

The baseband PHY (i.e. modem) is composed of the O-QPSK modulator and demodulator with simple convolutional channel coder. [Figure 4] shows the baseband PHY block diagram.

The modulation starts from fetching the data in the TX MAC FIFO. The PHY payload (PHY service data unit; PSDU) is optionally encoded with the convolutional channel encoder. After appending the preamble, SFD and length field to the PHY payload, a constructed frame (PHY protocol data unit; PPDU) is mapped to designated symbols according to the data-rate

control of the PHY controller. Each symbol is spread accordingly by the DSSS chip modulator. The spread PHY bit stream in the chip-level is then modulated to the O-QPSK signal and transmitted by the RF transmitter. Especially for the 250Kbps data-rate packet, its structure is fully compliant to the IEEE802.15.4 O-QPSK PHY specification.

With the RF receiver, the received O-QPSK signal is demodulated to the chip sequences. The gain amplifying blocks in the RF receiver are controlled by the automatic gain controller (AGC). The chip sequence is appropriately de-spread by the chip demodulator, and then the start of the designated frame is determined by detecting the synchronization header (preamble and SFD). When the SFD is detected, the baseband PHY generates the interrupt which indicates the start of a packet.

The length and the PHY payload followed by the synchronization header are decoded by the symbol demapper and Viterbi decoder (if the convolutional encoding is applied), and stored in the RX MAC FIFO. When the last data of the PHY payload is stored, the interrupt is generated to indicate the end of the packet reception. After a packet reception interrupt occurs, the RX MAC procedure is performed.

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI) and the link quality indicator (LQI) automatically. They are used to decide the quality of the communication channel.

While a packet does not exist, the baseband PHY continuously provides the RSSI of the RF signal at antenna. The measured RSSI is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined as busy, packet transmission is deferred until the channel state changes to idle.

6.2. Data Rate

MG2420 supports various data rates of 1~3Mbps for applications beyond IEEE 802.15.4 compliances.

The 1Mbps modes, which is listed in [Table 4], occupy 2MHz RF channel bandwidth which is same as the IEEE 802.15.4-2.4GHz 250Kbps standard mode.

The 2M~3Mbps modes, which are listed in [Table 5], occupy an RF channel bandwidth of 4MHz.

The high data rate modes of 1M~3Mbps use decreased spreading factor with the same preamble structure as 250Kbps. Also, they can use the FEC. The data rate is selected by writing to the registers: SEL_TXDR (0x211[3:0]) and CLK_SEL(0x2C6[1]).

Table 4. Data Rate Modes for 2Mcps (PER≤1%, Packet length of 20-byte)

RF Bandwidth=2MHz (Chip Rate: 2Mcps) / CLK_SEL=1			
Data Rate	**Sensitivity**	**SEL_TXDR**	**Comment**
1Mbps	-93 dBm	0x1	Using 1/2 FEC
250Kbps	-97 dBm	0x6	IEEE802.15.4 compliant

Table 5. Data Rate Modes for 4Mcps (PER≤1%, Packet length of 20-byte)

RF Bandwidth=4MHz (Chip Rate: 4Mcps) / CLK_SEL=0			
Data Rate	**Sensitivity**	**SEL_TXDR**	**Comment**
3Mbps	-86 dBm	0x3	Using 3/4 FEC
2Mbps	-90 dBm	0x1	Using 1/2 FEC

The modulated output spectrum for 2Mcps mode is shown in [Figure 5], and occupied RF bandwidth is 2MHz. The modulated output spectrum for 4Mcps mode is shown in [Figure 6]. For 4Mcps mode, occupied RF bandwidth is 4MHz.

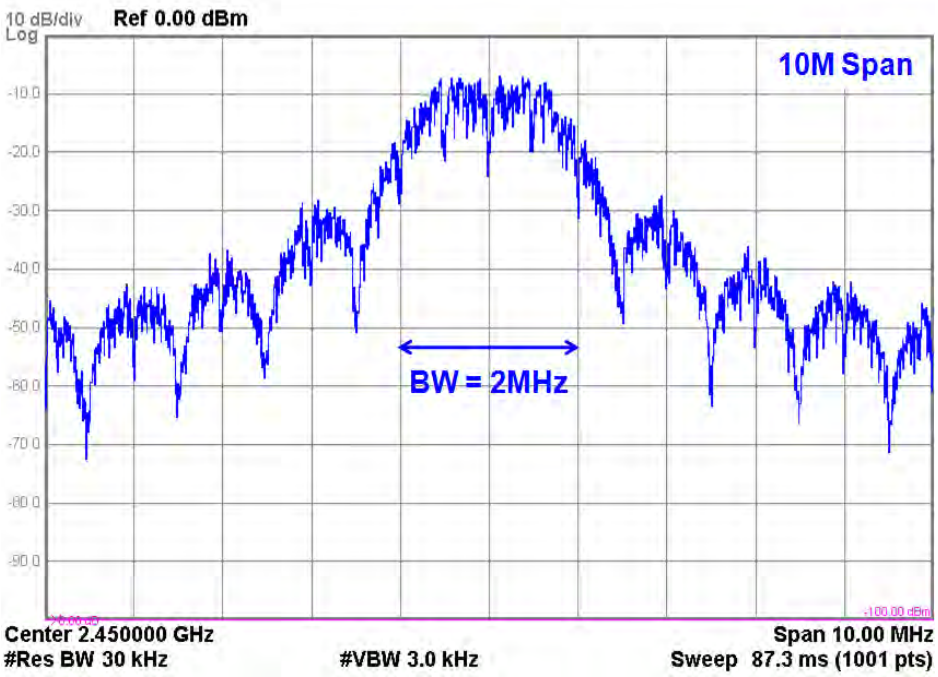


Figure 5. Modulated signal spectrum for 2Mcps mode.

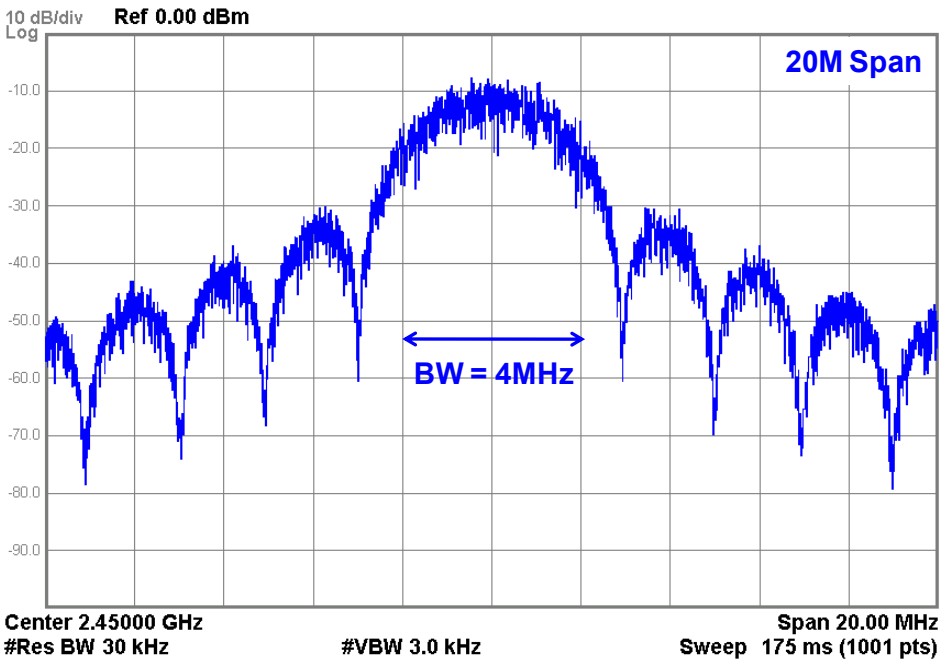


Figure 6. Modulated signal spectrum for 4Mcps mode.

6.3. Forward Error Correction(FEC)

Especially for higher data rate modes, MG2420 provides the variable-rate convolutional channel coding for forward error correction (FEC). MG2420 supports the convolution coding with the rates of 1/2 and 3/4

As shown in [Figure 7], the convolutional encoder with the constraint length of 5 is used for the mother convolutional encoder with the rate of 1/2. G1(x) = $x^4 + x + 1$. G2(x) = $x^4 + x^3 + x^2 + 1$. The rates of 3/4 are available by puncturing of the output of the mother convolutional encoder as shown in [Table 6].

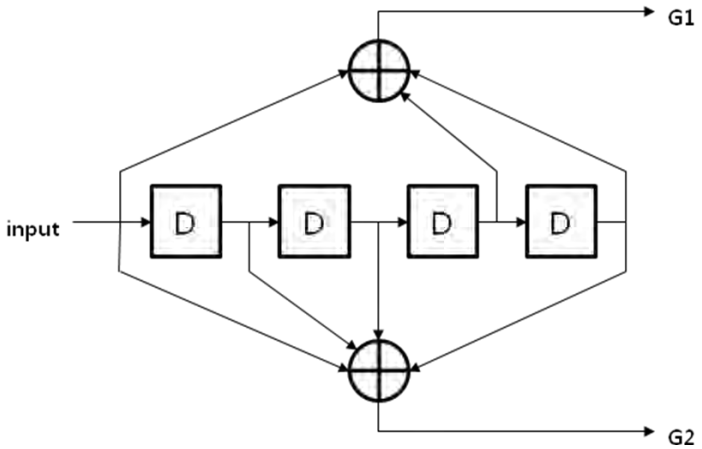


Figure 7. Convolutional encoder with rate of 1/2.

Table 6. Puncturing Pattern

Code Rate	Puncturing Matrix	Transmitted Sequence
1/2	G1: 1 G2: 1	G1[0] G2[0]
3/4	G1: 1 0 1 G2: 1 1 0	G1[0] G2[0] G2[1] G1[2]

6.4. Packet Format

MG2420 supports multiple data rates ranged from 1Mbps to 3Mbps including 250Kbps. The data rate is selected by writing to the registers: SEL_TXDR(0x211[3:0]) and CLK_SEL(0x2C6[1]).

The packet format comparison for high data rates(≥250Kbps) with an example PAYLOAD length of 60-Byte is shown in [Figure 8]. The period of the preamble, SFD, and LEN for 1Mbps modes is the same for 250Kbps mode. Only PAYLOAD period is reduced. The total packet times for 2Mbps and 3Mbps modes become half compared to 1Mbps and 1.5Mbps modes respectively. Consequently, using high data rate modes leads to significant reduction of both communication time and power consumption.

The effective payload data rate is shown in [Figure 9]. Due to the overhead caused by the preamble, SFD, and length field, the effective data rate is lower than the configured data rate. Furthermore, the effective data throughput including the MAC overhead would be lowered further.

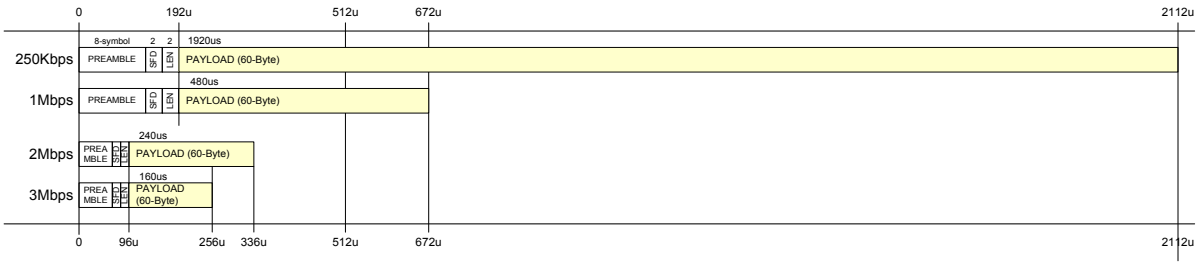
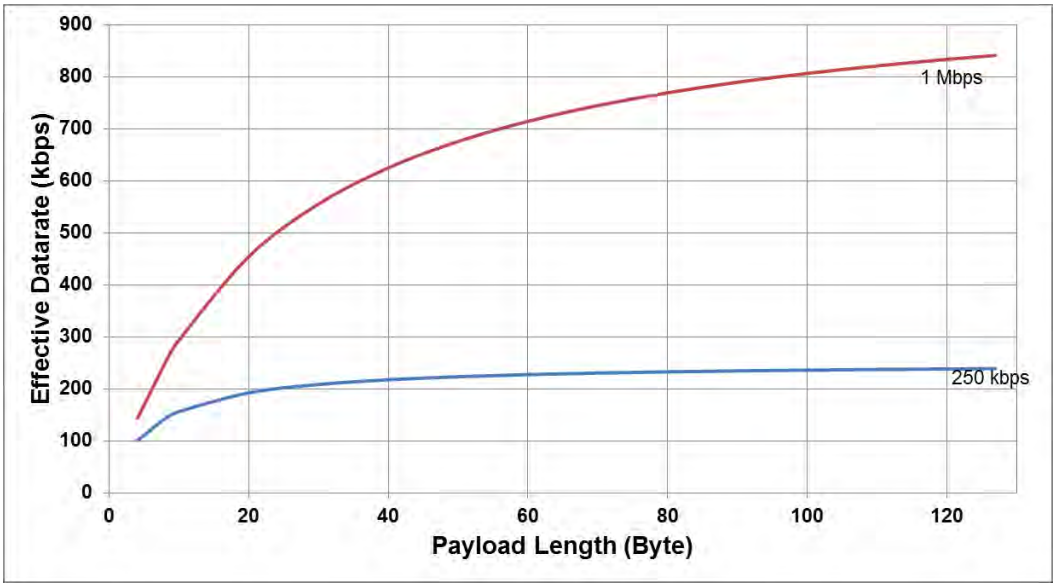
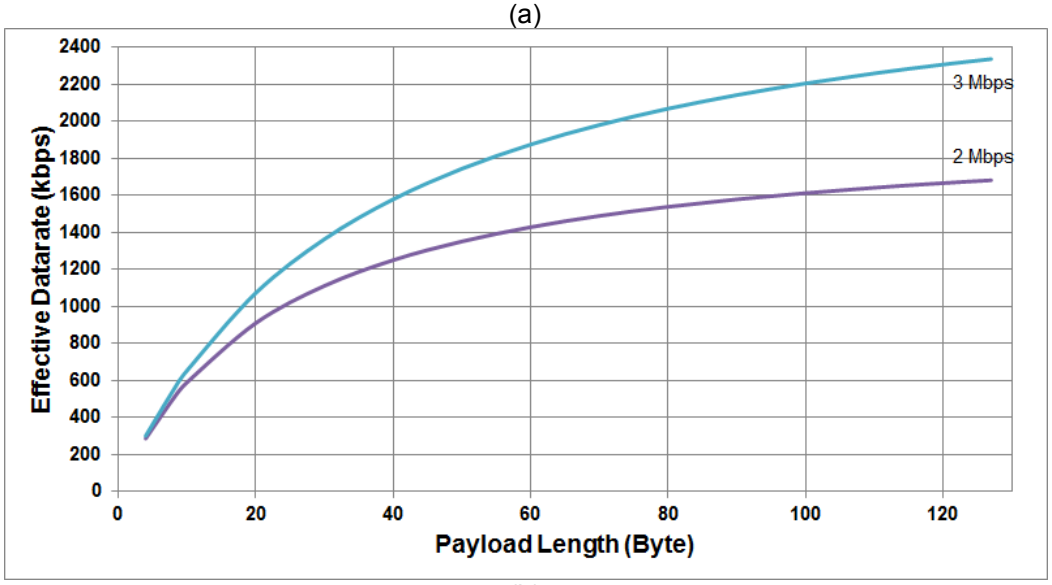


Figure 8. Packet format



(a)



(b)

Figure 9. Effective payload data rate. (a) 2Mcps mode. (b) 4Mcps mode.

6.5. RSSI and Energy Detection

When a packet is received, a modem block automatically provides the Received Signal Strength Indicator(RSSI). RSSI is measured by averaging the power level of the received signal for a certain period. RSSI value is stored in a register and the stored value is kept until the new packet is received.

While a packet is not received, a modem block continuously provides the RF channel energy level at antenna. Measured energy level is used in order to decide the communication channel state.

As shown in [Table 7], RXENRG register indicates the averaged energy level of the received signal at antenna. Its value is a 2's complement integer in dBm. The PKTENRG register shows the energy level of the last received packet. Its value is retained until another packet is received.

A typical RSSI value as RX input power for 250kbps is shown in [Figure 10].

Table 7. RSSI measurement

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x274	[7:0]	RXENRG	0x00	R	Averaged energy level of the received RF signal at antenna (in dBm)
0x275	[7:0]	PKTENRG	0x00	R	Averaged energy level of the received packet (in dBm)

Table 8. RSSI Characteristics

Parameter	MIN	TYP	MAX	UNIT	Note
RSSI Range		100		dB	
RSSI Accuracy		+2/-4		dB	
Step Size		1		dB	

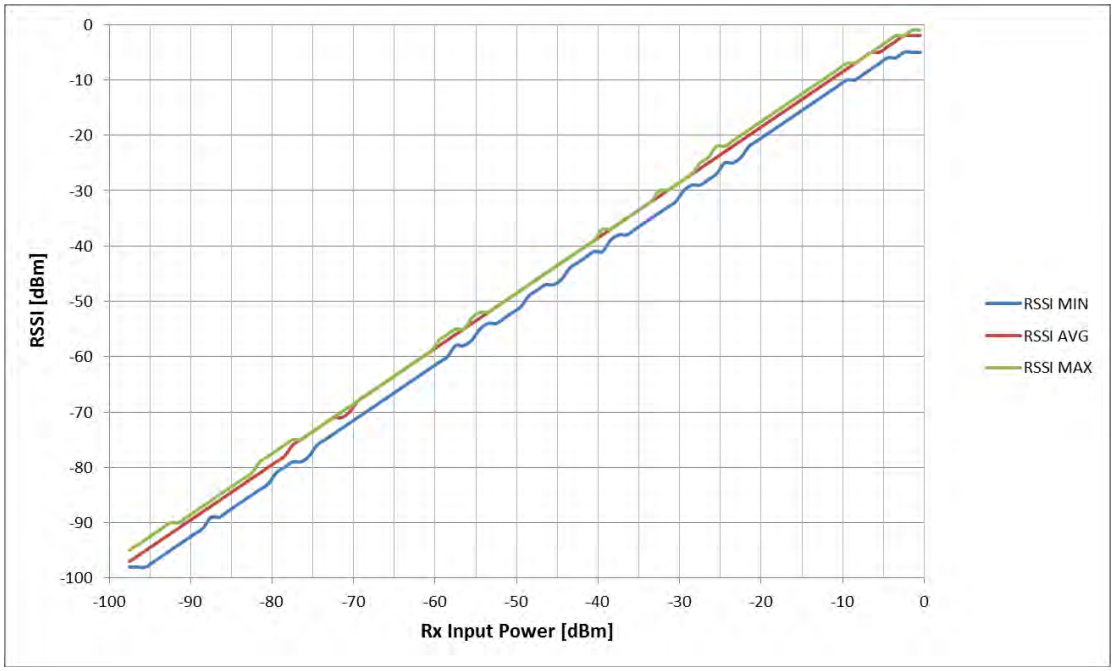


Figure 10. Typical RSSI value vs. RX input power for 250kbps.

6.6. Clear Channel Assessment (CCA)

While a packet does not exist, the baseband PHY continuously provides the RF channel energy level at antenna. As described before, the measured energy level is used in order to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used in order to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined as busy, packet transmission is deferred until the channel state changes to idle.

The CCA operation is configured through the register (0x24C) as depicted in [Table 9].

Table 9. CCA configuration

<table>
<tr><th>Address (hex)</th><th>Bit</th><th>Name</th><th>Reset Value</th><th>R/W</th><th>Description</th></tr>
<tr><td rowspan="4">0x24C</td><td>[7:6]</td><td>(Reserved)</td><td>00</td><td>R/W</td><td>Only ‘00’ allowed.</td></tr>
<tr><td>[5]</td><td>CCA_FIX</td><td>1</td><td>R/W</td><td>It fixes the communication channel state to idle. A communication channel state is determined by the CCA circuit in MG2420. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to ‘1’, the channel is always in idle state.</td></tr>
<tr><td>[4:2]</td><td>(Reserved)</td><td>000</td><td>R/W</td><td>Only ‘000’ allowed.</td></tr>
<tr><td>[1:0]</td><td>CCAMD</td><td>00</td><td>R/W</td><td>This field sets the method to determine the communication channel state. The following describes the three methods to detect the channel state.
Energy detection (ED)
This method determines the channel state as ‘busy’ when the energy of received signal is higher than the defined level.
Carrier detection (CD)
This method determines the channel state as ‘busy’ when an IEEE802.15.4 carrier is detected.
Frame detection (FD)
This method determines the channel state as ‘busy’ when the normal IEEE802.15.4 packet is detected.
<table>
<tr><th>CCAMD (binary)</th><th>Method</th></tr>
<tr><td>00</td><td>ED</td></tr>
<tr><td>01</td><td>CD</td></tr>
<tr><td>10</td><td>FD</td></tr>
</table>
</td></tr>
</table>

6.7. Link Quality Indicator (LQI)

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI) and the link quality indicator (LQI). They are used in order to decide the quality of the communication channel.

MG2420 uses correlation results of multiple symbols in order to calculate an estimate of the LQI value. If LQI_EN is “0x1”, then LQI estimation is automatically performed for every received frame. LQI values are integers ranging from 0 to 255 as required by the IEEE 802.15.4 standard.

After receiving 8 first symbols following the SFD, MG2420 provides a correlation average value as an LQI. This is indicated by the LQI_VALID register.

Table 10. LQI configuration

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x26E	[7]	LQI_VALID	0x0	R	LQI valid indicator
	[6:4]	(Reserved)	0x0	R/W	Only 0x0 allowed
	[3]	LQI_EN	0x0	R/W	LQI enable register (0: Disable, 1: Enable)
	[2:0]	(Reserved)	0x0	R/W	Only 0x0 allowed
0x26F	[7:0]	LQI	0x0	R	LQI value (0 ~ 255)

6.8. Integrated MAC

The integrated MAC block transmits the data received from high layer to baseband modem, or encrypts it and then transmits to baseband modem. In addition, it indicates the status of PHY and transmits the data received from baseband modem to high layer, or transmits the decrypted data to high layer.

[Figure 11] shows the integrated MAC structure. The RX and TX FIFOs are separately implemented. The size of each FIFO is 256 bytes in order to process one IEEE802.15.4 packet along with buffering one packet. Each MAC FIFO is accessed through the dedicated FIFO access function of the SPI(Refer to Sec 7.1.3.). The MAC FIFO and security FIFO shares the address space and are distinguished by setting the register of SECMAP (0x19F).
[
Table **11**] shows the address space of each FIFO.

When AUTO_ACK (0x191) is set to ‘1’, the ACK packet for the correctly received packet is automatically generated and sent.

[Table 12] describes general MAC/security control registers except for FIFO control registers.

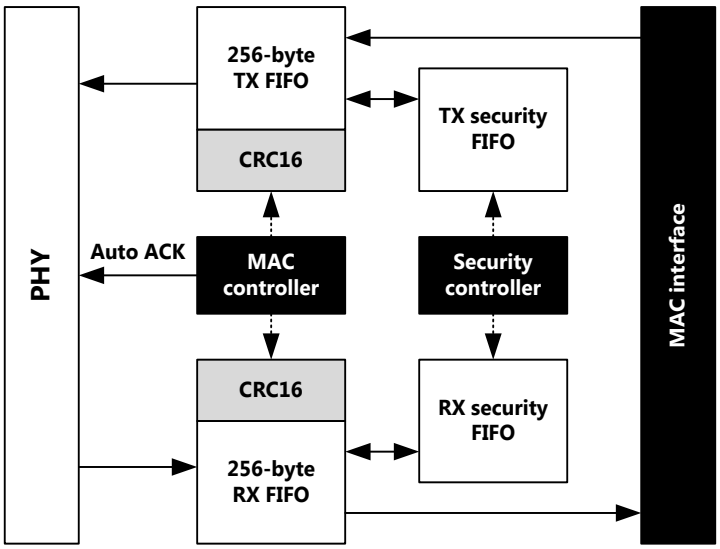


Figure 11. Integrated MAC structure

Table 11. MAC/security FIFO Address Map

Address (hex)	Name	R/W	Description
0x300 ~ 0x3FF	MTXFIFO or STXFIFO	R/W	Random access space for MAC TX FIFO (MTXFIFO; SECMAP = 0) or TX security FIFO (STXFIFO; SECMAP = 1)
0x400 ~ 0x4FF	MRXFIFO or SRXFIFO	R/W	Random access space for MAC RX FIFO (MRXFIFO; SECMAP = 0) or RX security FIFO (SRXFIFO; SECMAP = 1)

Table 12. MAC/security control registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x100 ~ 0x10F	[127:0]	KEY0		R/W	16-byte key (KEY0) for AES-128 0x10F: Most significant byte
0x110 ~ 0x11C	[103:0]	RXNONCE		R/W	Used for decryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x11C: Most significant byte of source address 0x114: Most significant byte of frame counter 0x110: Key sequence counter
0x120 ~ 0x12F	[127:0]	SAESBUF		R/W	Standalone encrypt/decrypt data buffer: After the AES-128 operation, the result is stored in this register. 0x12F: Most significant byte of plain-text and cipher-text
0x130 ~ 0x13F	[127:0]	KEY1		R/W	16-byte key (KEY0) for AES-128 0x13F: Most significant byte
0x140 ~ 0x14C	[103:0]	TXNONCE		R/W	Used for encryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x14C: Most significant byte of source address 0x144: Most significant byte of frame counter 0x140: Key sequence counter
0x150 ~ 0x157	[63:0]	IEEE_ADDR		R/W	64-bit IEEE address 0x157: Most significant byte
0x158 ~ 0x159	[15:0]	PAN_ID		R/W	16-bit PAN ID 0x159: Most significant byte

0x15A ~ 0x15B	[15:0]	SHORT_ADDR		R/W	16-bit short (network) address 0x15B: Most significant byte
0x180	[7]	ENCDEC_STS	0x0	R	When this field is set to '1', there is data in the encryption or decryption.
	[6]	TX_BUSY	0x0	R	When this field is set to '1', data in the TX FIFO is transmitted to a modem.
	[5]	RX_BUSY	0x0	R	When this field is set to '1', data is transmitted from a modem to the RX FIFO.
	[4]	SAES_DONE	0x0	R/W	When standalone AES operation is finished, this field is set to '1'.
	[3]	DECODE_OK	0x0	R	This field checks the validity of data according to the type of data received or the address mode. If there is no problem, this field is set to '1'.
	[2]	ENC_DONE	0x0	R/W	When encryption operation is finished, this field is set to '1'.
	[1]	DEC_DONE	0x0	R/W	When decryption operation is finished, this field is set to '1'.
	[0]	CRC_OK	0x0	R/W	If there is no problem for checking CRC of received packet, this field is set to '1'.
0x18E	[7:1]	(Reserved)		R	
	[0]	SAES	0x0	W	When this field is set to '1', the AES operation is done by data in SAESBUF and KEY selected by the SA_KEYSEL. This field is automatically cleared.
0x190	[7]	RST_FIFO	0x0	R/W	When this field is set to '1', the MAC FIFO is initialized.
	[6]	RST_TSM	0x0	R/W	When this field is set to '1', the MAC TX state machine is initialized.
	[5]	RST_RSM	0x0	R/W	When this field is set to '1', the MAC RX state machine is initialized.
	[4]	RST_AES	0x0	R/W	When this field is set to '1', the AES engine is initialized.
	[3:0]	(Reserved)		R	
0x191	[7:5]	(Reserved)		R	
	[4]	PREVENT_ACK	0x0	R/W	When this field is set to '1', the RX interrupt doesn't occur when the DSN field of received ACK packet is different from the value in MACDSN register during packet reception.
	[3]	PAN_COORDINATOR	0x0	R/W	When this field is set to '1', function for PAN coordinator is enabled.
	[2]	ADR_DECODE	0x1	R/W	When this field is set to '1', the RX interrupt doesn't occur when address information of the received packet is not matched with device itself.
	[1]	AUTO_CRC	0x1	R/W	When this field is set to '1', the RX interrupt doesn't occur when the CRC of the received packet is not valid.
	[0]	AUTO_ACK	0x0	R/W	When this field is set to '1', the ACK packet is automatically sent when the designated packet is correctly received.
0x192	[7:0]	MACDSN	0x00	R/W	If the DSN field of the received ACK packet is not equal to MACDSN, the RX interrupt does not occurred.
0x193	[7]	SA_KEYSEL	0x0	R/W	Selects the KEY value for standalone SAES operation. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.
	[6]	TX_KEYSEL	0x0	R/W	Selects the KEY value for AES operation during

<table>
<tr><td rowspan="4"></td><td></td><td></td><td></td><td></td><td>packet transmission. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td></tr>
<tr><td>[5]</td><td>RX_KEYSEL</td><td>0x0</td><td>R/W</td><td>Selects the KEY value for AES operation when packet reception. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td></tr>
<tr><td>[4:2]</td><td>SEC_M</td><td>0x0</td><td>R/W</td><td>In CBC-MAC operation, it represents the data length used in the authentication field in byte.
<table><tr><th>SEC_M</th><th>Authentication field length</th></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>10</td></tr><tr><td>5</td><td>12</td></tr><tr><td>6</td><td>14</td></tr><tr><td>7</td><td>16</td></tr></table></td></tr>
<tr><td>[1:0]</td><td>SEC_MODE</td><td>0x0</td><td>R/W</td><td>Security mode.
0x0: No security
0x1: CBC-MAC mode
0x2: CTR mode
0x3: CCM mode</td></tr>
<tr><td rowspan="2">0x194</td><td>[7]</td><td>(Reserved)</td><td></td><td>R</td><td></td></tr>
<tr><td>[6:0]</td><td>TXL</td><td>0x00</td><td>R/W</td><td>This field represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows.

Security mode: CTR
It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO.

Security mode: CBC-MAC
It represents the number of byte between length byte and the data to be authenticated.

Security mode: CCM
It represents the length of data which is used not in encoding or decoding but in authentication.</td></tr>
<tr><td rowspan="2">0x195</td><td>[7]</td><td>(Reserved)</td><td></td><td>R</td><td></td></tr>
<tr><td>[6:0]</td><td>RXL</td><td>0x00</td><td>R/W</td><td>This field represents the length used in the AES operation for the received packet and it has a different meaning for each security mode as follows.

Security mode: CTR
It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO.

Security mode: CBC-MAC
It represents the number of bytes between length byte and the data to be authenticated.

Security mode: CCM
It represents the length of data which is used not in encoding or decoding but in authentication.</td></tr>
<tr><td>0x19F</td><td>[7:1]</td><td>(Reserved)</td><td></td><td>R</td><td></td></tr>
</table>

	[0]	SECMAP	0x0	R/W	Security control/FIFO selection 0x0: MAC control / MAC FIFO selected 0x1: Security control / security FIFO selected

6.8.1. RX Mode

When receiving the data from the PHY, the MAC block stores the data in the RX FIFO. The data in the RX FIFO is decrypted or it is read through either the burst access of the SPI or single register access. Data decryption is implemented in AES-128 algorithm. The RX MAC controller controls the process described above. When decrypting the data, the received frame data length is modified and the modified value is automatically stored in the same address.

The RX FIFO is implemented in a circular FIFO structure with a write pointer and a read pointer. The RX FIFO can store several frame data received from the PHY block. Since the first byte of each frame data represents the frame data length, it is accessed by the write pointer and the read pointer.

When the data is received from the PHY block, the CRC information is checked to verify data integrity. When AUTO_CRC control bit is set to ‘1’, CRC information is automatically verified by the RX CRC block. To check the result, refer to the CRC_OK bit of 0x180 register. When the value of CRC_OK is set to ‘1’, there is no problem with CRC information. When the AUTO_CRC control bit is not set to ‘1’, the CRC information should be verified externally.

When a packet reception is completed in the PHY block, a PHY interrupt occurs.

[Table 13] shows the RX FIFO control registers. Register address space is shared with the security-related register address space. Therefore, the RX FIFO control registers in [Table 13] are accessible when SECMAP is 0x0.

Table 13. RX FIFO Control Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x080	[7:0]	MRFCPOP		R	Through this register, data in RX FIFO is read. The RX FIFO data is read with either the single register access (this register) or the burst mode of the SPI.
0x081	[7:0]	MRFCWP	0x00	R/W	RX FIFO write pointer Total size of the write pointer is 9-bit with MRFCWP8 in 0x084 register. It is increased by ’1’ whenever data is written to the RX FIFO.
0x082	[7:0]	MRFCRP	0x00	R/W	RX FIFO read pointer Total size of the read pointer is 9-bit with MRFCRP8 in 0x084 register. It is increased by ’1’ whenever data is read from the RX FIFO.
0x083	[7:3]	(Reserved)		R	
	[2]	ASA	0x1	R/W	When this field is set to ‘1’, it automatically sets the starting address of a packet and the length of a packet decrypted by the AES engine to the information of the received packet.
	[1]	ENA	0x1	R/W	When this field is set to ‘1’, RX FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to ‘1’, MRFCWP, MRFCRP, 0x084, MRFCSIZE registers are initialized.
0x084	[7]	MRFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with MRFCWP. This field is MSB, and is used to detect

					wrap-around of a circular FIFO.
	[6]	MRFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with MRFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	RX FIFO full This field is set to '1' when data size in RX FIFO is 256 byte.
	[0]	EMPTY	0x0	R	RX FIFO empty This field is set to '1' when data size in RX FIFO is '0'.
0x085	[7:0]	MRFCSIZE	0x00	R/W	This field represents the number of valid data bytes of RX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MRFCWP and MRFCRP.
0x086	[7:0]	MRFCROOM	0x00	R/W	Threshold control for RX FIFO empty and full

6.8.2. TX Mode

To transmit the data from a higher layer to the PHY, the data is stored in the TX FIFO of the MAC block through the SPI access. The TX FIFO is implemented by a circular FIFO structure with a write pointer and a read pointer. Since each data in TX FIFO is mapped to the memory addressing space, it is written or read directly through the single register access.

The data stored in the TX FIFO is encrypted or transmitted to the PHY block by the TX_REQ register. The TX MAC controller controls the process. The data length which is to be transmitted is stored in the first byte of each frame when the frame data is stored in TX FIFO. When the data in TX FIFO is encrypted, the data length is modified and then stored in the same address.

When transmitting the data in the TX FIFO, the CRC-16 bytes are attached in order for the receiver to verify data integrity. When the AUTO_CRC control bit of 0x191 register is set to '1', CRC information is automatically generated by TX CRC block. Otherwise, CRC operation should be performed externally.

When the data transmission to the PHY block is completed, a PHY interrupt occurs.

[Table 14] shows the TX FIFO control registers. As described above, the register address space is shared with the security-related register address space. Therefore, the TX FIFO control registers in [Table 14] are accessible when SECMAP is 0x0.

Table 14. TX FIFO control registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x000	[7:0]	MTFCPUSH		W	When data is written to this register, it is stored in TX FIFO. The TX FIFO data is written with either the single register access (this register) or the burst mode of the SPI.
0x001	[7:0]	MTFCWP	0x00	R/W	TX FIFO write pointer Total size of the write pointer is 9-bit with MTFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the TX FIFO.
0x002	[7:0]	MTFCRP	0x00	R/W	TX FIFO read pointer Total size of the read pointer is 9-bit with MTFCRP8 in

					0x004 register. It is increased by ’1’ whenever data is read from the TX FIFO.
0x003	[7:3]	(Reserved)		R	
	[2]	ASA	0x1	R/W	When this field is set to ‘1’, it automatically sets the starting address of a packet and the length of a packet encrypted by the AES engine to the information of the packet which is to be transmitted.
	[1]	ENA	0x1	R/W	When this field is set to ‘1’, TX FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to ‘1’, MTFCWP, MTFCRP, 0x004, and MTFCSIZE registers are initialized.
0x004	[7]	MTFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with MTFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	MTFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with MTFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	TX FIFO full This field is set to ‘1’ when data size in TX FIFO is 256 byte.
	[0]	EMPTY	0x0	R	TX FIFO empty This field is set to ‘1’ when data size in TX FIFO is ‘0’.
0x005	[7:0]	MTFCSIZE	0x00	R/W	This field represents the number of valid data bytes of TX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MTFCWP and MTFCRP.
0x006	[7:0]	MTFCROOM	0x00	R/W	Threshold control for TX FIFO empty and full
0x009 ~0x00A	[15:0]	AACKFC	0x00	R/W	Frame control field for transmitted auto-ACK packet. The most significant byte is 0x00A.
0x00B	[7:0]	AACKDSN	0x00	R/W	DSN value for transmitted auto-ACK packet
0x00C	[7:1]	(Reserved)		R	
	[0]	PENDING	0	R/W	Frame-pending subfield for transmitted auto-ACK packet

6.8.3. Data Encryption

Data encryption or decryption is done by the security controller block. The security controller consists of the encryption/decryption units and relevant controller. It supports the CCM* mode specified in ZigBee and CTR/CBC-MAC/CCM mode specified in IEEE802.15.4-2003 [1].

In order to encrypt or decrypt MAC payload, 128-bit key value and a nonce are needed. MG2420 can have two 128-bit key values, KEY0 and KEY1. For encryption, the desired nonce value should be stored in the TXNONCE and KEY0 or KEY1 should be selected for use. For decryption, the desired nonce value should be stored in the RXNONCE and KEY0 or KEY1 should be selected for use. For more detailed information, refer to the IEEE802.15.4 standard document.

The SAES (0x18E) register is used only for AES operation. In this case, required data for this operation should be stored in SAESBUF register and KEY0 or KEY1 should be selected for use.

[Table 15 and Table 16] describe TX and RX security FIFO control registers, respectively. They are accessible when SECMAP is 0x1.

Table 15. TX security FIFO control registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x000	[7:0]	STFCPUSH		W	When data is written to this register, it is stored in TX security FIFO. The TX security FIFO data is written with the single register access (this register), the burst mode of the SPI, or direct transfer between the TX security FIFO and the TX FIFO.
0x001	[7:0]	STFCWP	0x00	R/W	TX security FIFO write pointer Total size of the write pointer is 9-bit with STFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the TX security FIFO.
0x002	[7:0]	STFCRP	0x00	R/W	TX security FIFO read pointer Total size of the read pointer is 9-bit with STFCRP8 in 0x004 register. It is increased by '1' whenever data is read from the TX security FIFO.
0x003	[7:2]	(Reserved)		R	
	[1]	ENA	0x1	R/W	When this field is set to '1', TX security FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to '1', STFCWP, STFCRP, 0x004, STFCSIZE registers are initialized.
0x004	[7]	STFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with STFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	STFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with STFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	TX security FIFO full This field is set to '1' when data size in TX security FIFO is 256 byte.
	[0]	EMPTY	0x0	R	TX security FIFO empty This field is set to '1' when data size in TX security FIFO is '0'.
0x005	[7:0]	STFCSIZE	0x00	R/W	This field represents the number of valid data bytes of TX security FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between STFCWP and STFCRP.
0x006	[7:0]	STFCROOM	0x00	R/W	Threshold control for TX security FIFO full and empty
0x007	[7:0]	STFCSECBASE	0x00	R/W	Frame base address for encryption
0x008	[7:0]	STFCSECLEN	0x00	R/W	Frame length for encryption
0x009	[7:0]	STFDMALEN	0x00	R/W	Data size of direct transfer between the TX security FIFO and the TX FIFO.
0x00A	[7:3]	(Reserved)		R	
	[2]	DONE	0x0	R	This field is set to '1', when direct transfer between the TX security FIFO and the TX FIFO is done.
	[1]	BUSY	0x0	R	When this field is set to '1', data transfer between the TX security FIFO and the TX FIFO is activated.
	[0]	ENA	0x0	W	Enable the direct transfer between the TX security FIFO and the TX FIFO.

Table 16. RX Security FIFO control registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
0x080	[7:0]	SRFCPOP		R	Through this register, data in RX security FIFO is read. The RX security FIFO data is read with either the single register access (this register), the burst mode of the SPI, or direct transfer between the RX security FIFO and the RX FIFO.
0x081	[7:0]	SRFCWP	0x00	R/W	RX security FIFO write pointer Total size of the write pointer is 9-bit with SRFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the RX security FIFO.
0x082	[7:0]	SRFCRP	0x00	R/W	RX security FIFO read pointer Total size of the read pointer is 9-bit with SRFCRP8 in 0x004 register. It is increased by '1' whenever data is read from the RX security FIFO.
0x083	[7:2]	(Reserved)		R	
	[1]	ENA	0x1	R/W	When this field is set to '1', RX security FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to '1', SRFCWP, SRFCRP, 0x004, SRFCSIZE registers are initialized.
0x084	[7]	SRFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with SRFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	SRFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with SRFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	RX security FIFO full This field is set to '1' when data size in RX security FIFO is 256 byte.
	[0]	EMPTY	0x0	R	RX security FIFO empty This field is set to '1' when data size in RX security FIFO is '0'.
0x085	[7:0]	SRFCSIZE	0x00	R/W	This field represents the number of valid data bytes of RX security FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between SRFCWP and SRFCRP.
0x086	[7:0]	SRFCROOM	0x00	R/W	Threshold control for RX security FIFO full and empty
0x087	[7:0]	SRFCSECBASE	0x00	R/W	Frame base address for decryption
0x088	[7:0]	SRFCSECLEN	0x00	R/W	Frame length for decryption
0x089	[7:0]	SRFDMALEN	0x00	R/W	Data size of direct transfer between the RX security FIFO and the RX FIFO.
0x08A	[7:3]	(Reserved)		R	
	[2]	DONE	0x0	R	This field is set to '1', when direct transfer between the RX security FIFO and the RX FIFO is done.
	[1]	BUSY	0x0	R	When this field is set to '1', data transfer between the RX security FIFO and the RX FIFO is activated.
	[0]	ENA	0x0	W	Enable the direct transfer between the RX security FIFO and the RX FIFO.

6.9. Frequency Synthesizer(PLL)

According to the IEEE 802.15.4 specification, there are 16 channels in the 2.4-GHz band. And they are numbered by 11 through 26. The channel frequency is given by [1].

$$Fc = 2405 + 5*(k - 11)\ (MHz)$$

where k is channel number of IEEE 802.15.4-2.4GHz. Thus, to use k, PLLFREQ register shall be set to PLLFREQ[6:0] = 11 + 5*(k-11).
The center frequency for the channel number k of IEEE 802.15.4 is listed in [Table 17].

Table 17. Center Frequency Assignment

Register	Value	Channel Number k	Center Frequency [MHz]
PLLFREQ (0x286)	0x0B	11	2405
	0x10	12	2410
	0x15	13	2415
	0x1A	14	2420
	0x1F	15	2425
	0x24	16	2430
	0x29	17	2435
	0x2E	18	2440
	0x33	19	2445
	0x38	20	2450
	0x3D	21	2455
	0x42	22	2460
	0x47	23	2465
	0x4C	24	2470
	0x51	25	2475
	0x56	26	2480

The PLL locking time including frequency calibration period is less than 80usec. A lock status of the PLL is indicated with PLL_LOCK=1 in PLLMON(0x28C[0]) register.

6.10. Crystal Oscillator (XOSC)

The crystal oscillator generates the reference clock for the RF and digital blocks. As shown in [Figure 12], a 32MHz crystal unit is directly connected to XOSCI and XSOCO with external load capacitors.

OSCOK(0x2CF[0])=1 indicates that the reference clock is stabilized.

The total load capacitance, C_L is calculated by

$$C_L = \frac{C_{11}C_{12}}{C_{11}+C_{12}} + \frac{1}{2}\cdot C_p$$

where C_P represents all parasitic capacitances such as PCB stray capacitances and the package pin capacitance.

MG2420 provides the external clock to external circuits(refer to Sec 7.5.).

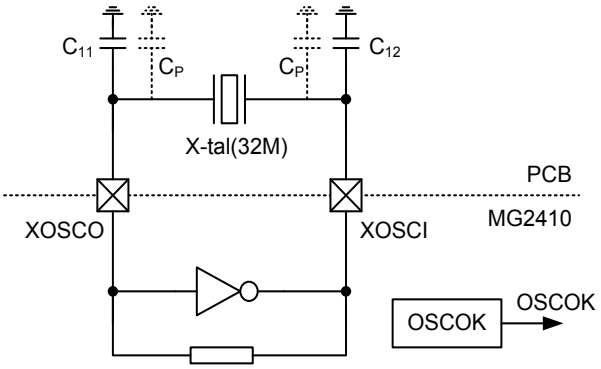


Figure 12. Simplified Crystal Oscillator schematic.

6.11. Voltage Regulator

There are several analog regulators (AVREGs) and one digital regulator(DVREG) in MG2420. Analog regulators provide the regulated internal voltage for the RF and analog blocks. Digital regulator supplies a regulated voltage to digital blocks. These regulators should be used only to supply internal blocks of MG2420 itself. Using the regulated outputs to supply external circuits is prohibited.

The DVREG is enabled by the DVREGEN, pin 22. To operate the DVREG, the DVREGEN should be connected to 3.0V.

The AVREGs are configured by the 0x2CF(AVREG) register.

The timing diagram for turning the digital regulator on and off can be seen in Sec.7.2.

6.12. Temperature Sensor

The on-chip analog temperature sensor output is accessed via the ATEST0 pin. The output voltages and characteristics are summarized in [**Table 18**] and the typical output voltage is shown in [**Figure 13**].

Table 18. Temperature Sensor Characteristics

Parameter	MIN	TYP	MAX	UNIT
Output voltage at -40°C		0.8276		V
Output voltage at 0°C		0.7709		V
Output voltage at +27°C		0.7322		V
Output voltage at +85°C		0.6463		V
Temperature coefficient		-1.4526		mV/°C

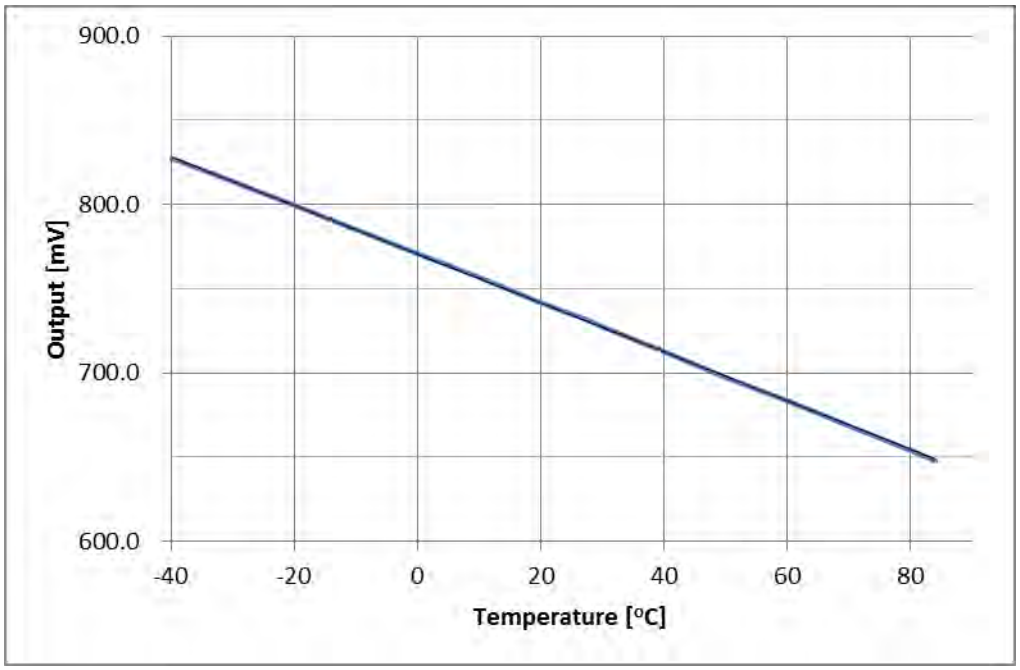


Figure 13. Temperature sensor output voltage.

6.13. Clock Control

Each block in MG2420 is controlled to enable or disable its operating clock. Clock control registers are located at addresses 0x2C0, 0x2C1, 0x2C2[7:4]. 0x2C3, and 0x2C5. The recommended clock setting is reset value(refer to [Table 19]). In the reset status, all Clock Control Registers (0x22C0 ~ 0x22CF) are activated except for test clock. If 0x2C1[7:6] is set to 0x0, other registers are not accessible. Clock Control State Machine automatically controls all clocks according to a modem status, data rate setting and so on. So there is no need to control the clock register by manual setting. It is recommended to use reset values.

Table 19. Operating clock setting

Mode / Status	Register Setting	Description
Reset Status	0x2C0=0xFF, 0x2C1=0xCC 0x2C2=0xB0	If 0x2C1[7:6] is set to 0x0, Only Clock Control registers are accessible. It is impossible to access Other Registers.
Normal Operation Mode	0x2C0=0xFF, 0x2C1=0xCC 0x2C2=0xB0	Enables all of clocks
TX Test Mode	0x2C0=0xFF, 0x2C1=0xDC 0x2C2=B0	Only for TX test mode. Enables TSTCLK

7. MICROCONTROLLER INTERFACE

MG2420 uses 4-wire SPI for external interface. External MCU controls MG2420, writes data in internal register, or reads the values through it. During the procedure above, MCU becomes a master and MG2420 becomes a slave.

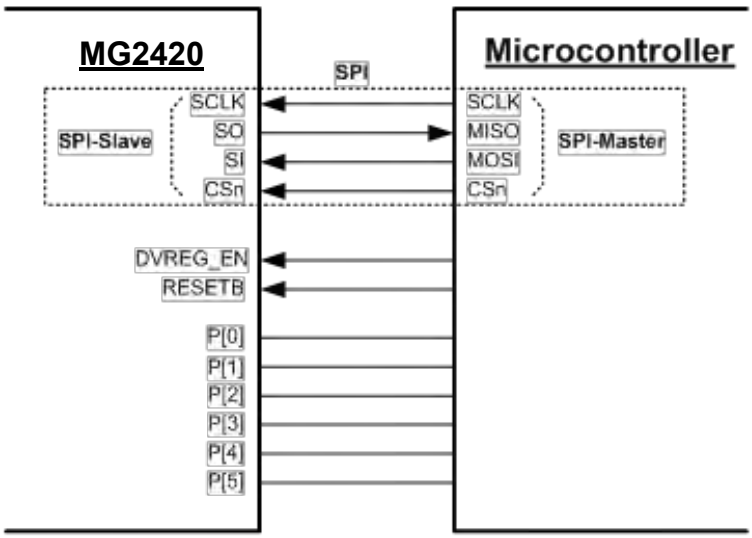


Figure 14. Microcontroller to MG2420 interfaces.

7.1. SPI Protocol

An SPI serial interface is used for radio configuration and packet handling.

7.1.1. SPI Timing Description

[Figure 15] illustrates the SPI timing diagram. SI is sampled at the falling edge of the SCLK and SO is set at the falling edge of the SCLK. The corresponding timing parameter definitions t_6 - t_{13} are summarized in [Table 20].

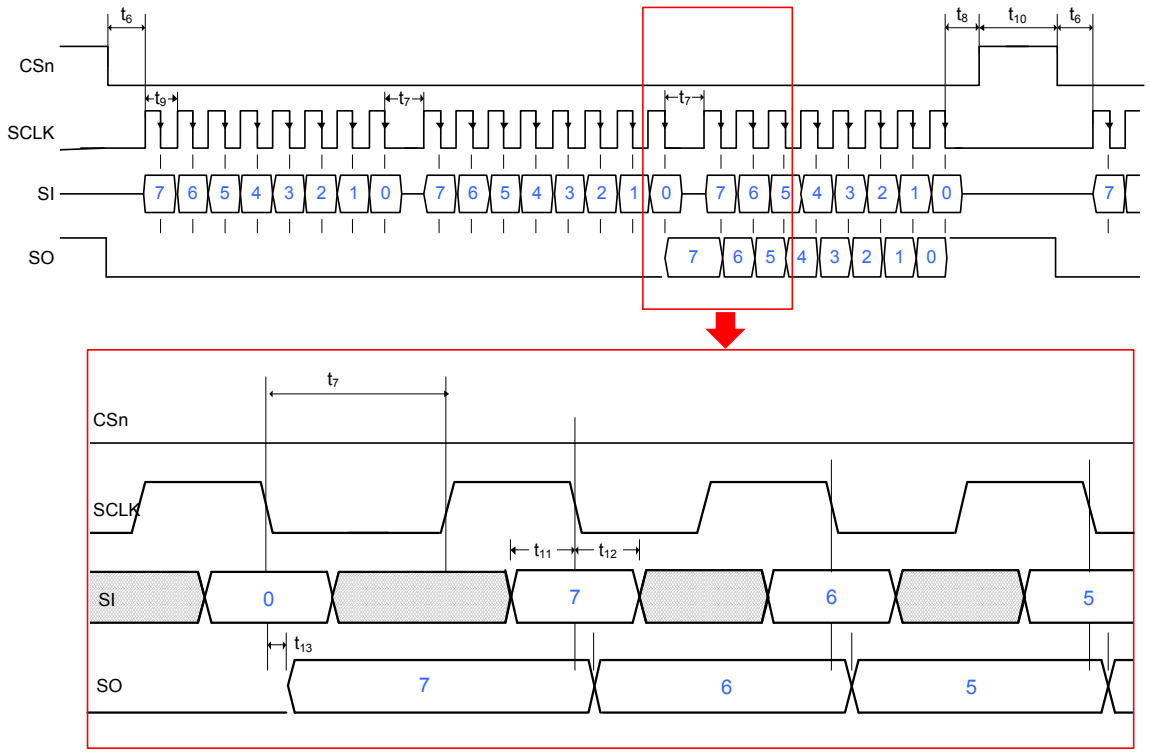


Figure 15. SPI timing diagram.

Table 20. SPI Timing Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
t_6	CSn low to first SCLK	50			ns
t_7	Last SCLK to following SCLK	50			ns
t_8	Last SCLK to CSn high	50			ns
t_9	SCLK frequency			12	MHz
t_{10}	SPI idle time	50			ns
t_{11}	SI setup time	20			ns
t_{12}	SI hold time	20			ns
t_{13}	SCLK to SO output	10			ns

7.1.2. Register Access

A register access mode is 3-byte write and read operation started by CSn=0. [**Table 21**] illustrates the SPI protocol format for the register access. The first byte consists of SPI_CMD and 4-bit high-address. The second bytes include 8-bit address. The third byte is data.

Table 21. SPI Format – Register Access

Byte1								Byte2								Byte3							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
SPI_CMD				Addr[11:8]				Addr[7:0]								Data[7:0]							

Each operation, which is configured by SPI_CMD, summarized in [Table 22]. SPI operation and timing are shown in [Figure 16] and [Figure 17]. For accessing *n* successive addresses, one can make the access format with the first address and *n* successive data. Note that the SCLK timing margin before the following low-address must be larger than 50ns (t_7 in [Figure 15] above).

Table 22. SPI Command – Register Access

Byte 1				Operation
SPI_CMD				
b7	b6	b5	b4	
0	0	0	0	Register write
1	0	0	0	Register read

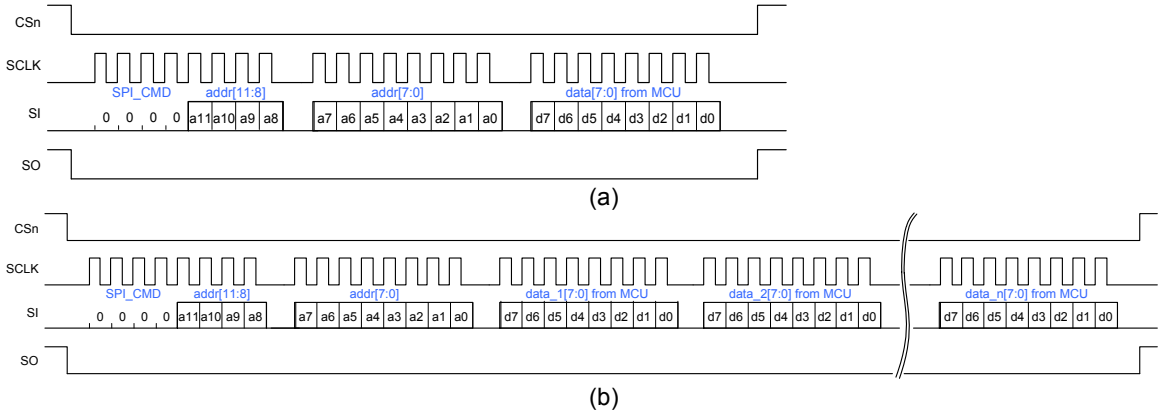


Figure 16. Register write sequence for (a) a single and (b) n successive data.

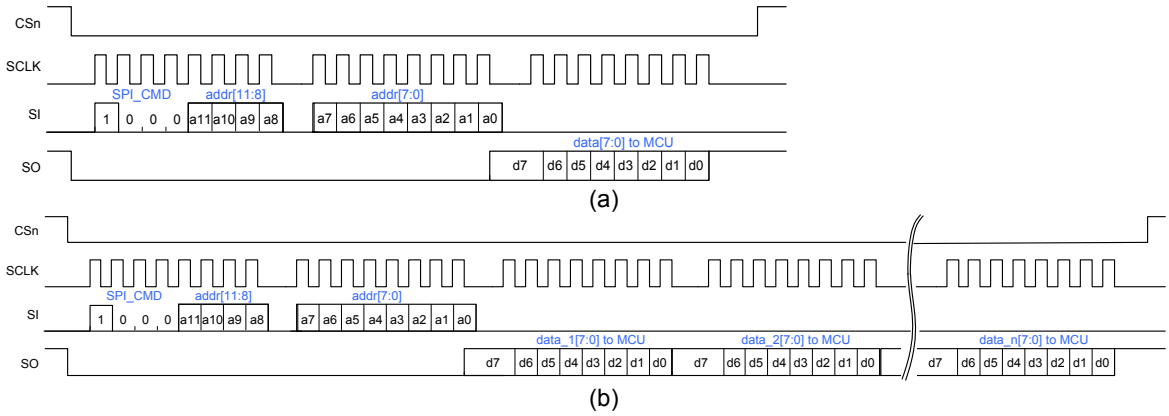


Figure 17. Register read sequence for (a) a single and (b) *n* successive data.

7.1.3. FIFO Access

The FIFO uses the address spaces 0x300~0x3FF and 0x400~0x4FF for TX and RX operations, respectively.

The FIFO access mode is 3-byte operation as described in [Table 23]. Basically, the format is same as register access. The first and second byte consists of SPI_CMD and Reserved.

The following bytes are the data.

Table 23. SPI Format – FIFO Access

Byte 1								Byte 2								Byte3							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
SPI_CMD				Reserved												data[7:0]							

Each FIFO operation is configured by SPI_CMD as summarized in [Table 24]. FIFO operation and timing are shown in [Figure 18] and [Figure 19]. Note that the SCLK timing margin before the following SCLK should be larger than 50ns (t_7 in [Figure 15] above).

Table 24. SPI Command – FIFO Access

Byte 1				Operation
SPI_CMD				
b7	b6	b5	b4	
0	1	0	0	TX FIFO Push (Write)
1	1	0	0	RX FIFO Pop (Read)

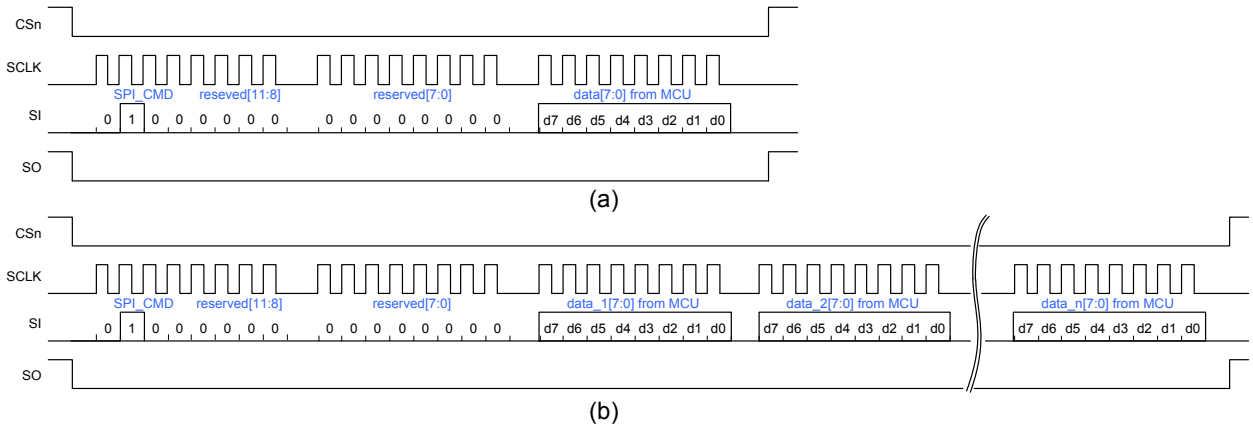


Figure 18. TX FIFO write sequence. (a) Single and (b) Multiple data access.

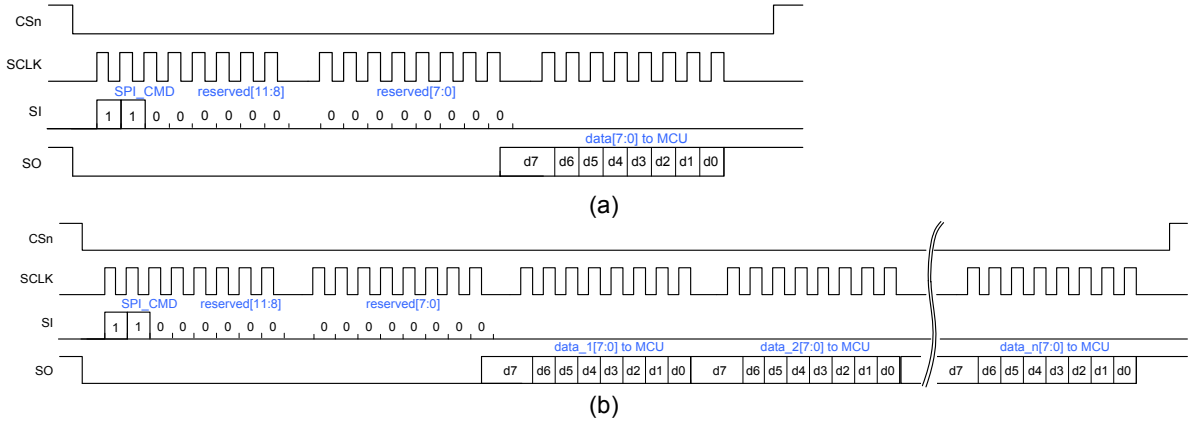


Figure 19. RX FIFO read sequence. (a) Single and (b) Multiple data access.

7.2. RESETB and DVREGEN

MG2420 reset and digital regulation enable signal diagram is shown in [Figure 20]. And the required timing characteristics are summarized in [Table 25].
As shown in [Figure 20], when DVREGEN is low state, the digital regulator is off and MG2420 is in the deep sleep state. To operate the digital regulator, the DVREGEN should be high(3V). The DVREGEN=H leads to turn on the digital regulator. At the same time, the crystal oscillator (XOSC) is enabled and its output stabilizes during t_{12}. In general, t_{12} mainly depends on the load capacitance of the crystal. When the DVREGEN goes to low, the digital voltage regulator(DVREG) will turn off and its output will goes to GND within t_9. t_9 is related to the output decoupling capacitance (C_{DVREG} in [Figure 2]).
The reset signal is active-low and therefore RESETB=L sets all registers to their default values. The reset signal width (t_{10} in [Figure 20]) should be larger than 4us. During 3.25us after releasing the reset(t_{11} in [Figure 20]), any access to the chip cannot be made.

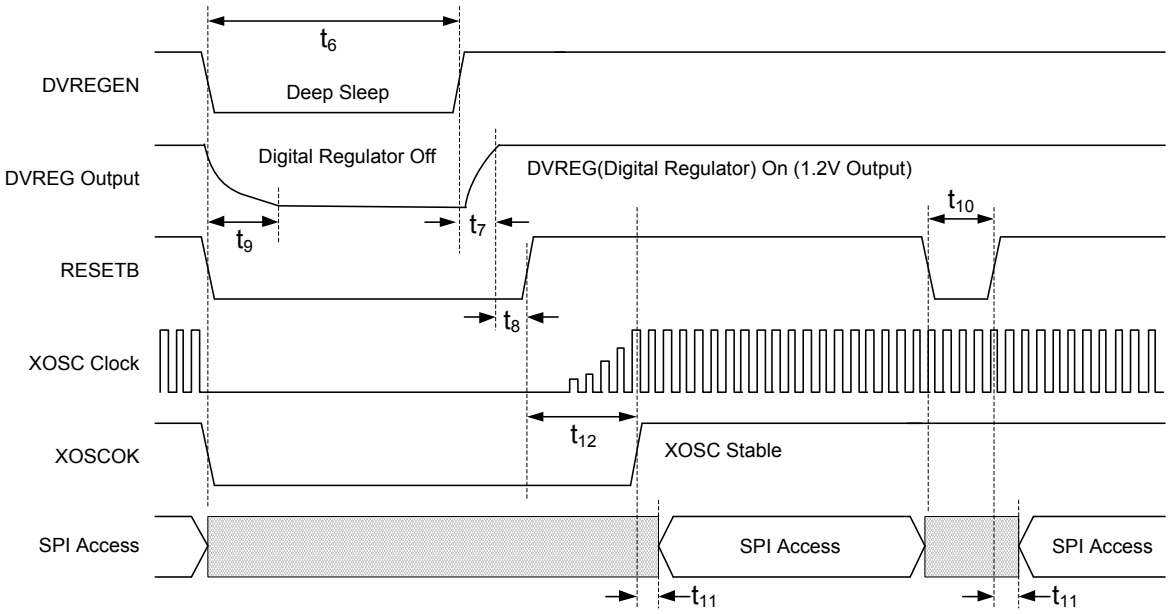


Figure 20. RESETB and DVREGEN signal diagram

Table 25. RESETB and DVREGEN Timing Characteristics

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_6	DVREGEN signal width	C_{D0}=1uF	3.3			ms
t_7	DVREG settling time	C_{D0}=1uF			97.0	us
t_8	RESETB signal width after DVREG on		2.9			us
t_9	DVREG discharge time	C_{D0}=1uF			3.3	ms
t_{10}	RESETB signal width		2.9			us
t_{11}	SPI access latency after reset	≥ 64 clock cycles at 32MHz	2.0			us
t_{12}	XOSC stabilized time				1.3	ms

7.3. Interrupt

For interface between MCU and MG2420, there is an interrrupt for notifying the modem status. MG2420 generates interrupt in case of modem-turned-on, the end of the packet transmission, and the end/start of the packet reception.

7.3.1. Signaling

The interrupt of MG2420 is detected in the signal level: When the interrrupt occurs, IRQ pin (refer to address 0x2F6) goes to the low.

7.3.2. Interrupt Source & Masking

The interrupt is generated when either (i) the modem is turned on, (ii) the packet tranmission is ended in the TX mode, (iii) the packet is detected and its reception is started, and (iv) the packet reception is ended, (v) the modem on is failed, (vi) the packet transmission is failed, (vii) the packet transmission is ended. Therefore, there are 7 interrupt sources listed in [Table 26]. When the interrupt occurs, the source of the interrupt is identified by reading the bit field [2:0] of 0x27E. The interrupt is masked by configuring the masking register(0x27D[6:0], 0 = masked).

Table 26. Interrupt Summary

Interrupt Source	Clear Register (0x27E[2:0])	Masking Register (0x27D[6:0]	Priority
Modem ON	0	xxx_xxx1	Highest
TX End	1	xxx_xx1x	
RX Start (Sync Detect)	2	xxx_x1xx	
RX End	3	xxx_1xxx	
Modem On Fail	4	xx1_xxxx	
TX Fail	5	x1x_xxxx	
TX Start	6	1xx_xxxx	Lowest

By default, all interrupts are to be masked(0x27D[6:0] = 0x0). The interrupt is unmasked by configuring the corresponding bit field as 1. For example, the interrupt for “Modem ON” is unmasked by setting the value of 0x27D[0] as 1.

When an interrupt occurs, the corresponding bit field of the source indication register (0x27F[6:0]) is set to 1 if the interrupt is not cleared. The interrupt sources have priority by Modem ON (0) > TX end (1) > RX start (2) > RX end (3) > Modem On Fail(4), TX Fail(5), TX Start(6). In order to clear the interrupt, it is sufficient to just read the clear register (0x27E[2:0]) and the interrupt is cleared (one by one) in a priority order. Therefore, the register of 0x27E[2:0] means which interrupt source would be cleared.

7.4. Other Digital Interface

MG2420 has 6 GPIO pins. Each GPIO is individually configured as monitor signal pin or register in/out pin by SEL_COMBMON (0x279[5:0]). Also each GPIO has programmable pull-up/down and driving strength control.

Driving strength (DS) The output driving strength of each GPIO is individually configured by GPIO_DS (0x21E ~ 0x21F). When each GPIO_DS is configured as 0~3, the driving strength is 4~16mA. A default driving strength value of a SO pad is a 16mA.

Table 27. GPIO Driving Strength

DS1	DS0	Driving Strength (mA)
0	0	4
0	1	8 (default)
1	0	12
1	1	16

Register I/O mode The register I/O mode is individually selected by SEL_COMBMON (0x279[5:0]). When selected as register I/O mode, each pin can be configured as output by GPIO_OEN (0x21A[5:0]) or input by GPIO_IE (0x21B[5:0]). When configured as output, each pin can be driven by GPIO_I (0x219[5:0]). Similarly, when configured as input, each pin can be read by GPIO_Z (0x218[5:0]). Additionally, the input pull-up/pull-down/strong pull-up of each GPIO is configured by GPIO_PS (0x21D[5:0]) and GPIO_SPU (0x2BE). By default, the input pull-up mode is set. The configuration table for GPIO_PS and GPIO_SPU is listed in [Table 28].

Table 28. GPIO Configuration Table for PS and SPU

PS	SPU	Status
0	x	Pull-down
1	0	Pull-up
1	1	Strong Pull-up

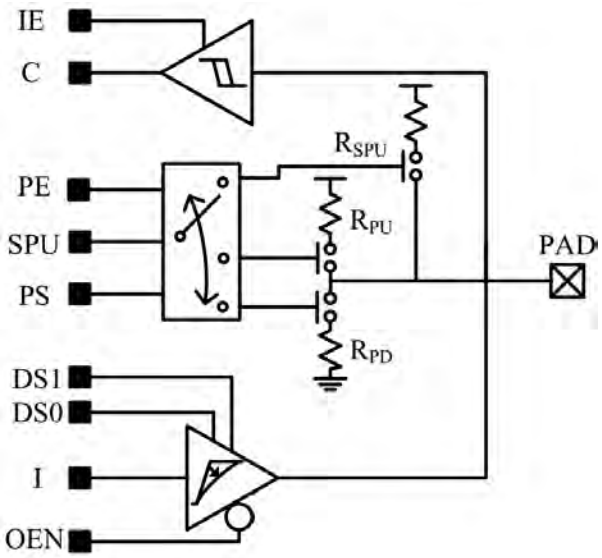


Figure 21. GPIO PAD Block Diagram

Reset Status When GPIO configuration is set as reset state, P[5] is set as a output mode and others are Input mode. [Table 29] shows GPIO Reset Status.

Monitor Signal Mode. Monitoring signal sets are available according to the value of SIGNAL_OUT register (0x2F6[6:4]).

Table 29. GPIO Reset State

GPIO	Reset Status		
	Direction	Pull-Up/Down	Strong Pull Up
P[0]	Input	Pull-Up	Disable
P[1]	Input	Pull-Up	Disable
P[2]	Input	Pull-Up	Disable
P[3]	Input	Pull-Up	Disable
P[4]	Input	Pull-Up	Disable
P[5]	Output (EXTCLK)	Pull-Up	Disable

7.5. External Clock Output

MG2420 provides the external clock output through P[5] (pin 15). The external clock frequencies of 32MHz, 16MHz, 8MHz, 4MHz, 2MHz, 1MHz, 500kHz, 250KHz, 125KHz, 62KHz, and 31KHz are generated and configured by EXTCLK(0x2C8) register. [**Table 30**] summarizes the external clock configuration. The reset value is 1MHz. The duty cycle of the external clock is maintained as 50:50.

The EXTCLK is available at P[5] after t_{12} in [Figure 20].

Table 30. External clock configuration

Register	Value	Description
EXTCLK (0x2C8)	0x0	32 MHz
	0x1	16 MHz
	0x2	8 MHz
	0x3	4 MHz
	0x4	2 MHz
	0x5	1 MHz (default)
	0x6	500 KHz
	0x7	250 KHz
	0x8	125 KHz
	0x9	62 KHz
	0xA	31 KHz
	0xF	No clock at P[5] (pin 15), output level of logic low

8. OPERATING DESCRIPTION

8.1. Basic Operating Mode

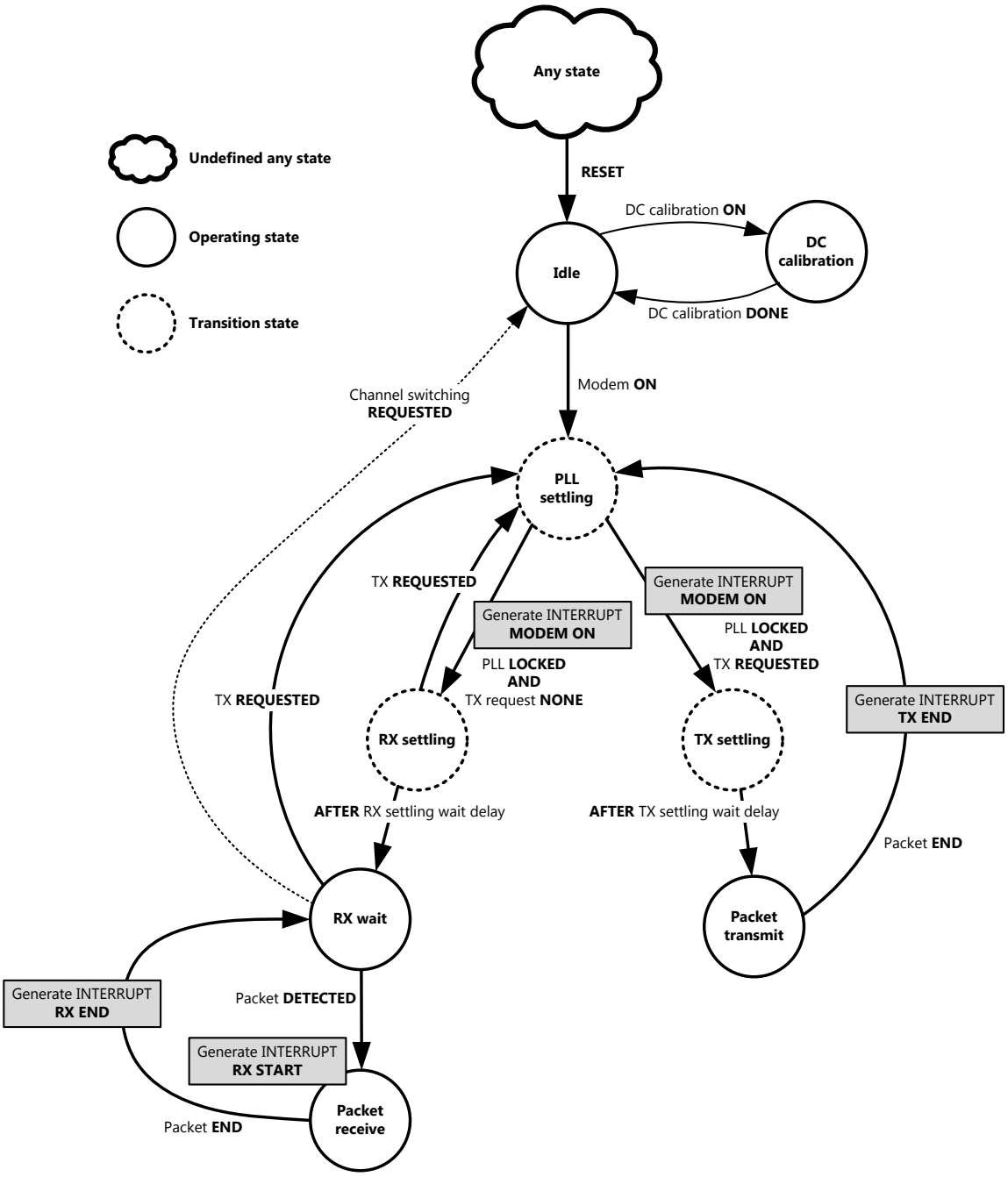


Figure 22. Basic MG2420 State Transition Diagram

MG2420 is controlled by the modem FSM shown in [Figure 22]. MG2420 is initialized by the external reset. Depending on the control of the modem FSM, MG2420 operates in either packet transmitting or packet receiving mode. When the packet to be transmitted is prepared by MAC TX FIFO, MG2420 operates in the packet transmit mode only. Besides, it operates in the packet receiving mode and waits for the packet.

Idle state: MG2420 is initialized by the external reset and the state of the modem FSM is moved to the *idle* state. In this state, the modem executes no operation.

DC calibration state: In order to receive the packet correctly, the DC offset of the RF receiver should be calibrated before use. Before *MODEM ON* is set, the DC offset of the RF receiver is preferred to be calibrated. When the DC calibration is initiated, the state is transited to *DC calibration* state. When the DC calibration has completed, the state is automatically transited to *idle* state. After the initial DC calibration is performed, the DC calibration tracker should be enabled.

PLL settling state: When the DC calibration is done, the RF synthesizer for channel selection is configured and then the PLL (RF synthesizer) is started. Additionally, the PLL may be restarted in order to change the RX or TX channel. In the *PLL settling* state, the modem waits for the PLL to be locked. This state is also called a transition state. If the PLL is already locked (it can be clearly identified from the PLL lock detection flag), this state can be skipped.

TX settling state: When the PLL is locked and the packet transmission is requested (from MAC layer), the state of the modem FSM is changed from the *PLL settling* to the *TX settling*. In this state, the modem waits for the RF transmitter to be stable. The DM calibration shall be performed if needed. The modem FSM stays at this state during the *TX (settling) wait delay* which can be configured.

Packet transmit state: After *TX (settling) wait delay*, the state of the modem FSM is transited to the *packet transmit* state when the DM calibraton is completed. In this state, the modem transmits the packet in accordance to the PHY specification. When the packet transmission is completed, the state is moved to the *PLL settling* state along with generating the interrupt for *TX END*.

RX settling state: When the PLL is locked and no packet transmission is requested, the state of the modem FSM is changed from the *PLL settling* to the *RX settling* state in order to wait for packet coming from other transmitting units. In this state, the modem waits for the RF receiver to be stable. The modem FSM stays at this state during the *RX (settling) wait delay* which can be configured. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the *RX settling* to the *PLL settling* state.

RX wait state: After *RX (settling) wait delay*, the state of the modem FSM is transited to the *RX wait* state. In this state, the modem waits for the packet reception. When the packet is detected, the state is moved to the *packet receive* state along with generating the interrupt for *RX START*. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the *RX wait* to the *PLL settling* state. If the channel is reselected, the state moves to *idle* state.

Packet receive state: When the packet is detected at the *RX wait* state, the state of the modem FSM is moved to the *packet receive* state. In this state, the modem receives the packet and puts its payload to MAC RX FIFO. At the end of the packet, the state is transited to the *RX wait* state along with generating the interrupt for *RX END*.

RF test mode state: The *RF test mode* state is entered by setting the register as the *RF test mode*. When the PLL is locked and the *RF test mode* is set, the modem FSM changes its

state from the *PLL settling* to the *RF test mode* state. Basically, in this state, the modem operates as the transmitter only. Therefore, the DM calibration shall be performed if needed. The modem FSM leaves this state to the *idle* state when the *RF test mode* becomes disabled.

9. REGISTER MAP

MG2420 is configured and controlled by accessing the register map through the SPI. [Figure 23] shows overall register address space.

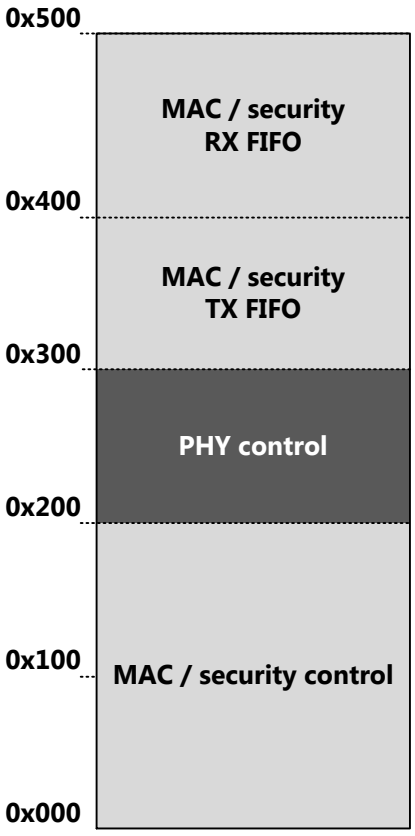


Figure 23. Overall register address space

9.1. Modem Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
PCMD0 0x200	[7:6]	(Reserved)	00	R/W	Only '00' allowed.
	[5]	MODEM_OFF	1	R/W	When this field is set to '0', the modem block status is changed to OFF. In the OFF state, the RF block is in a power-down state and the modem block is in the reset state. In this state, MG2420 cannot receive or transmit packets. For the transmission or the reception of a packet, the modem block needs to be changed to ON state. When the modem block goes to OFF state, this field is automatically set to '1' by the hardware.
	[4]	MODEM_ON	1	R/W	When this field is set to '0', a modem block status is changed to ON. In ON state,the RF and modem blocks are in the TX or RX ready state. In this state, the modem block controls power-down or power-up for the transmitter or the receiver without an active user application program. When the modem block goes to ON status, this field is automatically set to '1' by the hardware.

	[3]	(Reserved)	1	R/W	Only '1' allowed.
	[2]	TX_REQ	1	R/W	When this field is set to '0', the modem block transmits a packet. When a packet transmission is requested, the modem block changes to the TX ready state. Only when a communication channel is in idle state(CCA= '1'), the packet will be transmitted. When the channel is in busy state(CCA= '0'), the transmission is deferred until the channel state goes to idle. This field is automatically set to '1' by hardware after completing the transmission. When the packet transmission is completed successfully, a TXEND_INT interrupt is sent. If the packet transmission is abnormal, the interrupt is not sent and the TXREQ field is set to '1'.
	[1]	TX_ON	0	R/W	When this field is set to '1', the baseband digital transmitter is always activated regardless of the control of the state machine. When this field is set to '0', the digital transmitter is under the control of the state machine or TX_OFF register.
	[0]	RX_ON	0	R/W	When this field is set to '1', the baseband digital receiver is always activated regardless of the control of the state machine. When this field is set to '0', the digital receiver is under the control of the state machine or RX_OFF register.
PCMD1 0x201	[7:2]	(Reserved)	0x00	R/W	Only 0x00 allowed.
	[1]	TX_OFF	0	R/W	When this field is set to '1' and TX_ON is set to '0', the baseband digital transmitter is always deactivated regardless of the control of the state machine. When this field is set to '0' or TX_ON is set to '1', the digital transmitter is under the control of the state machine or TX_ON register.
	[0]	RX_OFF	0	R/W	When this field is set to '1' and RX_ON is set to '0', the baseband digital receiver is always deactivated regardless of the control of the state machine. When this field is set to '0' or RX_ON is set to '1', the digital receiver is under the control of the state machine or RX_ON register.
PLLPD[4] 0x202	[7]	BIAS power-down	1	R/W	BIAS power-down control 0=forced-power-down 1=automatically-controlled
	[6]	RFBIAS power-down	1	R/W	RFBIAS power-down control 0=forced-power-down 1=automatically-controlled
	[5:4]	(Reserved)	00	R	
	[3]	PLL Reset	1	R/W	PLL reset control. 0=forced-reset asserted 1=automatically-controlled
	[2]	VCO_Buffer power-down	1	R/W	VCO Buffer power-down control. 0=forced-power-down 1=automatically-controlled
	[1]	VCO power-down	1	R/W	VCO power-down control. 0=forced-power-down 1=automatically-controlled
	[0]	CP power-down	1	R/W	PLL Charge-Pump power-down control. 0=forced-power-down

[4] The priority of PLLPU is higher than that of PLLPD. When both of PLLPD and PLLPU are set to '0,' the corresponding block is ON.

					1=automatically-controlled
PLLPU 0x203	[7]	BIAS power-up	1	R/W	BIAS power-up control 0=forced-power-up 1=automatically-controlled
	[6]	RFBIAS power-up	1	R/W	RFBIAS power-up-control 0=forced-power-up 1=automatically-controlled
	[5:4]	(Reserved)	00	R	
	[3]	PLL Reset Clear	1	R/W	PLL reset clear control. 0=forced-reset cleared 1=automatically-controlled
	[2]	VCO_Buffer power-up	1	R/W	VCO Buffer power-up control. 0=forced-power-up 1= automatically-controlled
	[1]	VCO power-up	1	R/W	VCO power-up control. 0=forced-power-up 1=automatically-controlled
	[0]	CP power-up	1	R/W	PLL Charge-Pump power-up control. 0=forced-power-up 1=automatically-controlled
RXRFPD[5] 0x204	[7]	PA power-down	1	R/W	Power-Amplifier power-down control. 0=forced-power-down 1=automatically-controlled
	[6]	PLL_DMC power-down	1	R/W	PLL Direct-Modulation Conveter power-down control. 0=forced-power-down 1=automatically-controlled
	[5]	(Reserved)	0	R	
	[4]	LNA power-down	1	R/W	LNA power-down control. 0=forced-power-down 1=automatically-controlled
	[3]	RMIX power-down	1	R/W	RX Mixer power-down control. 0=forced-power-down 1=automatically-controlled
	[2]	LOGEN power-down	1	R/W	LO Generator power-down control. 0=forced-power-up 1=automatically-controlled
	[1]	LPF/VGA power-down	1	R/W	Low-Pass Filter and Variable-Gain Amplifier power-down control. 0=forced-power-down 1=automatically-controlled
	[0]	ADC power-down	1	R/W	RX ADC power-down control. 0=forced-power-down 1=automatically-controlled
RXRFPU 0x205	[7]	PA power-up	1	R/W	Power-Amplifier power-up control. 0=forced-power-up 1=automatically-controlled
	[6]	PLL_DMC power-up	1	R/W	PLL Direct-Modulation Conveter power-up control.

[5] The priority of RXRFPU is higher than that of RXRFPD. When both of RXRFPD and RXRFPU are set to '0,' the corresponding block is ON.

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td></td><td>[5]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td></td><td>[4]</td><td>LNA power-up</td><td>1</td><td>R/W</td><td>LNA power-up control.
0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td></td><td>[3]</td><td>RMIX power-up</td><td>1</td><td>R/W</td><td>RX Mixer power-up control.
0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td></td><td>[2]</td><td>LOGEN power-up</td><td>1</td><td>R/W</td><td>LO Generator power-up control.
0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td></td><td>[1]</td><td>LPF/VGA power-up</td><td>1</td><td>R/W</td><td>Low-Pass Filter and Variable-Gain Amplifier power-up control.
0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td></td><td>[0]</td><td>ADC power-up</td><td>1</td><td>R/W</td><td>RX ADC power-up control.
0=forced-power-up
1=automatically-controlled</td></tr>
<tr><td>MDMCNF3
0x211</td><td>[7:4]</td><td>(Reserved)</td><td>0100</td><td>R/W</td><td>Only ‘0100’ allowed.</td></tr>
<tr><td></td><td>[3:0]</td><td>SEL_TXDR</td><td>0x6</td><td>R/W</td><td>
<table>
<tr><th colspan="2">CLK_SEL=1
(RF BW=2MHz)</th><th colspan="2">CLK_SEL=0
(RF BW=4MHz)</th></tr>
<tr><th>SEL_TXDR</th><th>Data Rate</th><th>SEL_TXDR</th><th>Data Rate</th></tr>
<tr><td>0x0</td><td>2Mbps x Coding rate</td><td>0x0</td><td>4Mbps x Coding rate</td></tr>
<tr><td>0x2</td><td>250Kbps</td><td></td><td></td></tr>
<tr><td>0x3</td><td>125Kbps</td><td colspan="2" rowspan="4"><Notes>
CLK_SEL: 0x2C6[1]</td></tr>
<tr><td>0x5</td><td>62.5Kbps</td></tr>
<tr><td>0x9</td><td>31.25Kbps</td></tr>
</table>
Coding rate is controlled by CDRATE Register.</td></tr>
<tr><td>MDMCNF6
0x214</td><td>[7:4]</td><td>(Reserved)</td><td>0x4</td><td>R/W</td><td>Only 0x4 allowd.</td></tr>
<tr><td></td><td>[3:0]</td><td>AACK_WAIT_TIME</td><td>0xF</td><td>R/W</td><td>This determines the interval between the received packet and its ACK packet. The interval is 16*AACK_WAIT_TIME usec.</td></tr>
<tr><td>MDMCNF7
0x215</td><td>[7:2]</td><td>(Reserved)</td><td>0x00</td><td>R/W</td><td>Only 0x00 allowd</td></tr>
<tr><td></td><td>[1:0]</td><td>CDRATE</td><td>0x0</td><td>R/W</td><td>Convolutional encoder code rate
00: Used in DSS
01: 1/2 code rate
10: Reserved
11: 3/4 code rate</td></tr>
<tr><td>AGCCNF
0x220-
0x23F</td><td></td><td>AGCCNF</td><td></td><td>R/W</td><td>The several registers are prepared to control AGC block. The receiver performance is very sensitive to the setting. These registers are not recommended to be modified. The required configuration of these registers is referred to MG2420 EVK.</td></tr>
<tr><td>CORCNF
0x240-
0x248</td><td></td><td>CORCNF</td><td></td><td>R/W</td><td>The several registers are prepared to control receiver core block. The receiver performance is very sensitive to the setting. These registers are not recommended to be modified. The required configuration of these registers is referred to MG2420 EVK.</td></tr>
<tr><td>CCA0</td><td>[7:6]</td><td>(Reserved)</td><td>00</td><td>R/W</td><td>Only ‘00’ allowed.</td></tr>
</table>

<table>
<tr><td rowspan="3">0x24C</td><td>[5]</td><td>CCA_FIX</td><td>0</td><td>R/W</td><td>It fixes the communication channel state to idle. A communication channel state is determined by the CCA circuit in MG2420. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to ‘1’, the channel is always in idle state.</td></tr>
<tr><td>[4:2]</td><td>(Reserved)</td><td>000</td><td>R/W</td><td>Only ‘000’ allowed.</td></tr>
<tr><td>[1:0]</td><td>CCAMD</td><td>00</td><td>R/W</td><td>This field sets the method to determine the communication channel state. The following describes the three methods to detect the channel state.

ED (Energy Detection): This method determines the channel state as ‘busy’ when the energy of received signal is higher than the defined level.

CD (Carrier Detection): This method determines the channel state as ‘busy’ when an IEEE802.15.4 carrier is detected.

FD (Frame Detection): This method determines the channel state as ‘busy’ when the normal IEEE802.15.4 packet is detected.

<table><tr><th>CCAMD</th><th>Method</th></tr><tr><td>00</td><td>ED</td></tr><tr><td>01</td><td>CD</td></tr><tr><td>10</td><td>FD</td></tr></table></td></tr>
<tr><td>CA1
0x24D</td><td>[7:0]</td><td>CCA_TH</td><td>0xB2</td><td>R/W</td><td>The threshold value of CCA (in dBm)</td></tr>
<tr><td rowspan="4">LQICNF0
0x26E</td><td>[7]</td><td>LQI_VALID</td><td>0</td><td>R</td><td>LQI valid indicator :</td></tr>
<tr><td>[6:4]</td><td>(Reserved)</td><td>000</td><td>R/W</td><td>Only ‘000’ allowed.</td></tr>
<tr><td>[3]</td><td>LQI_EN</td><td>0</td><td>R/W</td><td>LQI enable register (0: Disable, 1: Enable)</td></tr>
<tr><td>[2:0]</td><td>(Reserved)</td><td>000</td><td>R/W</td><td>Only ‘000’ allowed</td></tr>
<tr><td>LQICNF1
0x26F</td><td>[7:0]</td><td>LQI</td><td>0x00</td><td>R</td><td>LQI value (0~255)</td></tr>
<tr><td rowspan="4">CLKCFG
0x2C6</td><td>[7:4]</td><td>(Reserved)</td><td>0x2</td><td>R/W</td><td>Only ‘0x2’ allowed.</td></tr>
<tr><td>[3:2]</td><td>(Reserved)</td><td>00</td><td>R/W</td><td>Only ‘00’ allowed.</td></tr>
<tr><td>[1]</td><td>CLK_SEL</td><td>0</td><td>R/W</td><td>Sets the chip rate.
0: 4Mcps mode
1: 2Mcps mode</td></tr>
<tr><td>[0]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td rowspan="4">SCRM0
0x2FA</td><td>[7:5]</td><td>(Reserved)</td><td></td><td></td><td>Only ‘0x010’ allowed</td></tr>
<tr><td>[4]</td><td>SCRM_EN</td><td></td><td></td><td>Scrambler enable
0: Disable
1: Enable</td></tr>
<tr><td>[3:2]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td>[1:0]</td><td>SCRM_SEED</td><td>00</td><td>R/W</td><td>Scrambler seed</td></tr>
</table>

9.2. Clock Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
CLKON0 0x2C0	[7:2]	(Reserved)	0x00	R	
	[1]	RXCLK	1	R/W	AGC clock enable register 0 : Disable 1 : Enable
	[0]	ADCCLK	1	R/W	RX ADC clock enable register 0 : Disable 1 : Enable
CLKON1 0x2C1	[7]	REG_PRB_CLK	1	R/W	PHY Register clock enable register 0: Disable 1: Enable
	[6]	REG_RF_CLK	1	R/W	RF Register clock enable register 0: Disable 1 :Enable
	[5]	(Reserved)			
	[4]	TSTCLK	0	R/W	TX clock enable register for TX test mode 0 : Disable 1 : Enable
	[3]	TXCLK	1	R/W	TX clock enable register 0 : Disable 1 : Enable
	[2]	MPICLK	1	R/W	Modem state machine clock enable register 0 : Disable 1 : Enable
	[1:0]	(Reserved)	00	R	
CLKON2 0x2C2	[7]	CLKON_DCC	0	R/W	DCC clock enable register 0: Disable 1: Enable
	[6]	(Reserved)	0	R/W	Only ‘0’ allowed
	[5]	REG_READ_CLK	1	R/W	Register Read Latch clock 0: Disable 1: Enable
	[4]	CLKON_AGC	1	R/W	AGC clock enable register 0: Disable 1: Enable
	[3:0]	(Reserved)	0x0	R/W	Only ‘0’ allowed.
	[0]	(Reserved)	0	R	
CLKON3 0x2C3	[7]	AESCLK	1	R/W	MAC AES clock enable register 0: Disable 1: Enable
	[6]	MTCLK	1	R/W	TX-MAC clock enable register 0: Disable 1: Enable
	[5]	MRCLK	1	R/W	RX-MAC clock enable register 0: Disable 1: Enable

	[4:0]	(Reserved)	0x00	R	

It is recommended to set CLKON-register as Enable status except for CLKON_TSTCLK. If CLKON registers are activated, The Clock Control State Machine automatically controls the clock enable status internally.

9.3. Digital Interface Pin Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
GPCNF0 0x218	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_Z	0x00	R	When Digital Interface Pins are configured as register input mode, Pin signal value is read by GPIO_Z.
GPCNF1 0x219	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_I	0x00	R/W	When Digital Interface Pins are configured as register output mode, corresponding pin is driven by GPIO_I.
GPCNF2 0x21A	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_OEN	0x3F	R/W	Register output mode enable control 0: Enable 1: Disable (default) GPIO_OEN[n] → GPIO[n] Out Enable Control (n: 0~5)
GPCNF3 0x21B	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_IE	0x1F	R/W	Register input mode enable control 0: Disable 1: Enable (default) GPIO_IE[n] → GPIO[n] Input Enable Control (n: 0~5)
GPCNF4 0x21C	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_PE	0x00	R/W	Input pull-up/down enable control 0: High-Z 1: Pull-up/down (default / controlled by GPIO_PS) GPIO_PE[n] → GPIO[n] Pull up Enable Control (n: 0~5)
GPCNF5 0x21D	[7:6]	(Reserved)	00	R	
	[5:0]	GPIO_PS	0x3F	R/W	Input pull-up/down control 0: Pull-down 1: Pull-up (default) GPIO_PS[n] → GPIO[n] Pull Up Selection Control (n: 0~5)
GPCNF6 0x21E	[7:6]	GPIO_DS3	0 0	R/W	GPIO[3] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA

					3: 16mA
	[5:4]	GPIO_DS2	0 0	R/W	GPIO[2] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA 3: 16mA
	[3:2]	GPIO_DS1	0 0	R/W	GPIO[1] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA 3: 16mA
	[1:0]	GPIO_DS0	0 0	R/W	GPIO[0] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA 3: 16mA
GPCNF7 0x21F	[7:6]	(Reserved)	00	R	
	[5:4]	SO_DS	0 1	R/W	SPI SO Pin Output driving strength 0: 4mA 1: 8mA (default) 2: 12mA 3: 16mA
	[3:2]	GPIO_DS5	0 0	R/W	GPIO[5] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA 3: 16mA
	[1:0]	GPIO_DS4	0 0	R/W	GPIO[4] Output driving strength 0: 4mA (default) 1: 8mA 2: 12mA 3: 16mA
GPCNF9 0x2BE	[7]	(Reserved)	0	R	
	[6]	SO_SPU	0	R/W	Controls SO pad strong pull-up. 0: disable 1: enable
	[5:0]	GPIO_SPU	0x00	R/W	Controls GPIO strong pull-up. 0: disable 1: enable GPIO_SPU[n] → GPIO[n] Strong Pull up Control (n: 0~5)
EXTCLK	[7:4]	(Reserved)	0000	R	

<table>
<tr><td>0x2C8</td><td>[3:0]</td><td>EXTCLK</td><td>0101</td><td>R/W</td><td>Controls the external clock frequency.
<table>
<tr><th>Value</th><th>Output Clock Freq.</th></tr>
<tr><td>0x0</td><td>32 MHz</td></tr>
<tr><td>0x1</td><td>16 MHz</td></tr>
<tr><td>0x2</td><td>8 MHz</td></tr>
<tr><td>0x3</td><td>4 MHz</td></tr>
<tr><td>0x4</td><td>2 MHz</td></tr>
<tr><td>0x5</td><td>1 MHz (default)</td></tr>
<tr><td>0x6</td><td>500 KHz</td></tr>
<tr><td>0x7</td><td>250 KHz</td></tr>
<tr><td>0x8</td><td>125 KHz</td></tr>
<tr><td>0x9</td><td>62 KHz</td></tr>
<tr><td>0xA</td><td>31 KHz</td></tr>
<tr><td>0xF</td><td>No output, P[5]=L</td></tr>
</table></td></tr>
<tr><td rowspan="2">MONCON0
0x279</td><td>[7:6]</td><td>(Reserved)</td><td>00</td><td>R</td><td></td></tr>
<tr><td>[5:0]</td><td>SEL_COMBMON</td><td>0x1F</td><td>R/W</td><td>Some Digital Interface pins are assigned as monitoring, others are used as input.

SEL_COMBMON[n]
0 : Monitor Signal Output Mode
1 : GPIO Direction is determined by GPIO Register, (Reset value is a input mode. Except for P[5])
<table>
<tr><th rowspan="2">GPIO</th><th colspan="2">SEL_COMBMON[n] → GPIO_P[n]</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td>P[0]</td><td>Monitor</td><td rowspan="6">Register I/O
(0x21A~0x21B)</td></tr>
<tr><td>P[1]</td><td>Monitor</td></tr>
<tr><td>P[2]</td><td>Monitor</td></tr>
<tr><td>P[3]</td><td>Monitor</td></tr>
<tr><td>P[4]</td><td>Monitor</td></tr>
<tr><td>P[5]</td><td>Monitor
(EXTCLK)</td></tr>
</table></td></tr>
<tr><td rowspan="3">MONCON3
0x2F6</td><td>[7]</td><td>(Reserved)</td><td>0</td><td>R/W</td><td>Only ‘0’ allowed.</td></tr>
<tr><td>[6:4]</td><td>SIGNAL_OUT</td><td>000</td><td>R/W</td><td>Output Signal Selection Register
<table>
<tr><th rowspan="2">GPIO</th><th colspan="3">Digital interface Monitor Control Value (output mode)</th></tr>
<tr><th>0x0</th><th>0x1</th><th>0x2</th></tr>
<tr><td>P[0]</td><td>IRQ</td><td>TRSW</td><td>TRSW</td></tr>
<tr><td>P[1]</td><td>TRSW</td><td>nTRSW</td><td>nTRSW</td></tr>
<tr><td>P[2]</td><td>nTRSW</td><td>IRQ</td><td>IRQ</td></tr>
<tr><td>P[3]</td><td>CRCOK</td><td>CRCOK</td><td>CRCOK</td></tr>
<tr><td>P[4]</td><td>PLL_LOCK</td><td>MAC_SEC_DONE</td><td>PLL_LOCK</td></tr>
<tr><td>P[5]</td><td>EXTCLK</td><td>EXTCLK</td><td>EXTCLK</td></tr>
</table></td></tr>
<tr><td>[3:0]</td><td>(Reserved)</td><td>1111</td><td>R/W</td><td>Only ‘1111’ allowed.</td></tr>
</table>

9.4. PLL Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
PLLCTRL 0x280	[7:5]	(Reserved)	001	R/W	Only '001' allowed.
	[4]	VCVALEN	0	R/W	'0': Closed loop. '1': Open loop. The control voltage of the VCO is applied from VC_DAC_VAL[3:0].
	[3:1]	(Reserved)	000	R/W	Only '000' allowed.
	[0]	PLLSTART	0	R/W	When this bit is set to high, at first, a course frequency calibration performs to find appropriate capacitor array values in the VCO. Soon after that, through a fine frequency tuning process, the PLL is locked finally. PLLSTART bit is automatically cleared to '0.'
PLLFREQ 0x286	[7]	(Reserved)	0	R	
	[6:0]	PLL_FREQ[6:0]	0x38	R/W	Sets the RF channel frequency. To set the IEEE802.15.4 channel frequency, PLLFREQ shall be set to PLLFREQ[6:0] = 11 + 5*(k-11). k is channel number of IEEE 802.15.4-2.4GHz.
PLLVCO2 0x288	[7]	(Reserved)	1	R/W	Only '1' allowed.
	[6:4]	VCO_CUR1[2:0]	101	R/W	Adjusts VCO current. '100' is recommended.
	[3:2]	VCO_CUR2[1:0]	00	R/W	Adjusts VCO current. '00' is recommended.
	[1:0]	VCOBUF_CUR[1:0]	11	R/W	Adjusts VCO Buffer current. '11' is recommended.
PLLVCDAC 0x28A	[7:4]	(Reserved)	1000	R/W	Only '1000' allowed.
	[3:0]	VC_DAC_VAL[3:0]	1000	R/W	When the VCVALEN sets to '1,' the control voltage (VC) of the VCO is controlled by VC_DAC_VAL[3:0]. The VC value is : VC = 0.08*VC_DAC_VAL[3:0] [V]. At VCVALEN=0, it is allowed to set to '0101.'
PLLAFC 0x28B	[7:0]	(Reserved)	0x0A	R/W	Only '0x0A' allowed.
PLLMON 0x28C	[7:4]	(Reserved)	1010	R/W	Only '1010' allowed.
	[3:1]	(Reserved)	000	R	
	[0]	PLL_LOCK	0	R	The locking status of the PLL. When the PLL is in locked status, this bit is automatically set high.

9.5. RF Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
RXCUR 0x298	[7:6]	LNA_CUR1[1:0]	01	R/W	Adjusts LNA current. '01' is recommended.
	[5:4]	LNA_CUR2[1:0]	01	R/W	Adjusts LNA current. '01' is recommended.
	[3:2]	RMIX_CUR[1:0]	01	R/W	Adjusts RX Mixer current. '01' is recommended.
	[1:0]	LOGEN_CUR[1:0]	01	R/W	Adjusts LO Generator current. '01' is recommended.
RXBW0 0x29A	[7:0]	(Reserved)	0x91	R/W	Only '0x91' allowed.
RXBW1 0x29B	[7:0]	(Reserved)	0xDD	R/W	Only '0xDD' allowed.
RXBW2	[7:0]	(Reserved)	0x70	R/W	Only '0x75' allowed.

<table>
<tr><td>0x29C</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="3">RFBIAS
0x29D</td><td>[7:4]</td><td>(Reserved)</td><td>0000</td><td>R/W</td><td>Only ‘0000’ allowed.</td></tr>
<tr><td>[3:2]</td><td>LPF_CUR[1:0]</td><td>01</td><td>R/W</td><td>Adjusts LPF current. ‘01’ is recommended.</td></tr>
<tr><td>[1:0]</td><td>RFBIAS_CUR</td><td>01</td><td>R/W</td><td>Only ‘01’ allowed.</td></tr>
<tr><td rowspan="3">TXPA
0x29E</td><td>[7:5]</td><td>(Reserved)</td><td>000</td><td>R</td><td rowspan="6">Configures the TX output power level.
<table><tr><th rowspan="2">TX Output (dBm)</th><th colspan="2">Setting Value (hex)</th></tr><tr><th>TXPA (0x29E)</th><th>TXDA (0x29F)</th></tr><tr><td>+9</td><td>0x1F</td><td>0x1A</td></tr><tr><td>+8</td><td>0x1E</td><td>0x1A</td></tr><tr><td>+7</td><td>0x1C</td><td>0x1B</td></tr><tr><td>+6</td><td>0x19</td><td>0x1F</td></tr><tr><td>+5</td><td>0x1A</td><td>0x19</td></tr><tr><td>+4</td><td>0x16</td><td>0x19</td></tr><tr><td>+3</td><td>0x13</td><td>0x1F</td></tr><tr><td>+2</td><td>0x12</td><td>0x1D</td></tr><tr><td>+1</td><td>0x11</td><td>0x1B</td></tr><tr><td>0</td><td>0x13</td><td>0x17</td></tr><tr><td>-1</td><td>0x14</td><td>0x0F</td></tr><tr><td>-2</td><td>0x06</td><td>0x1C</td></tr><tr><td>-3</td><td>0x07</td><td>0x12</td></tr><tr><td>-4</td><td>0x04</td><td>0x1C</td></tr><tr><td>-5</td><td>0x02</td><td>0x1E</td></tr><tr><td>-6</td><td>0x0A</td><td>0x13</td></tr><tr><td>-7</td><td>0x02</td><td>0x19</td></tr><tr><td>-8</td><td>0x04</td><td>0x12</td></tr><tr><td>-9</td><td>0x03</td><td>0x12</td></tr><tr><td>-10</td><td>0x02</td><td>0x12</td></tr><tr><td>-20</td><td>0x0B</td><td>0x10</td></tr><tr><td>-30</td><td>0x10</td><td>0x1C</td></tr><tr><td>-40</td><td>0x10</td><td>0x15</td></tr><tr><td>-50</td><td>0x08</td><td>0x01</td></tr></table></td></tr>
<tr><td>[7:4]</td><td>(Reserved)</td><td>0000</td><td>R/W</td></tr>
<tr><td>[3:2]</td><td>PA_PC[1:0]</td><td>11</td><td>R/W</td></tr>
<tr><td rowspan="3">TXDA
0x29F</td><td>[2:0]</td><td>PA_GC[2:0]</td><td>111</td><td>R/W</td></tr>
<tr><td>[7:5]</td><td>(Reserved)</td><td>000</td><td>R</td></tr>
<tr><td>[4:3]</td><td>DA_DC[1:0]</td><td>11</td><td>R/W</td></tr>
<tr><td>[2:0]</td><td>DA_CC[2:0]</td><td>111</td><td>R/W</td></tr>
<tr><td>DMEQ01
0x290</td><td>[7:0]</td><td>(Reserved)</td><td>0x82</td><td>R/W</td><td>TX direct-modulation parameter for 4Mcps mode
Only ‘0x52’ allowed.</td></tr>
<tr><td>DMEQ02
0x291</td><td>[7:0]</td><td>(Reserved)</td><td>0xA4</td><td>R/W</td><td>TX direct-modulation parameter for 4Mcps mode
Only ‘0xF3’ allowed.</td></tr>
<tr><td>DMEQ03
0x292</td><td>[7:0]</td><td>(Reserved)</td><td>0x3F</td><td>R/W</td><td>TX direct-modulation parameter for 4Mcps mode
Only ‘0xCB’ allowed.</td></tr>
<tr><td>DMEQ04
0x293</td><td>[7:0]</td><td>(Reserved)</td><td>0x44</td><td>R/W</td><td>TX direct-modulation parameter for 4Mcps mode
Only ‘0x7F’ allowed.</td></tr>
<tr><td>DMEQ11
0x294</td><td>[7:0]</td><td>(Reserved)</td><td>0x28</td><td>R/W</td><td>TX direct-modulation parameter for 2Mcps mode
Only ‘0x28’ allowed.</td></tr>
<tr><td>DMEQ12
0x295</td><td>[7:0]</td><td>(Reserved)</td><td>0xD2</td><td>R/W</td><td>TX direct-modulation parameter for 2Mcps mode
Only ‘0xF2’ allowed.</td></tr>
</table>

DMEQ13 0x296	[7:0]	(Reserved)	0x1C	R/W	TX direct-modulation parameter for 2Mcps mode Only '0x03' allowed.
DMEQ14 0x297	[7:0]	(Reserved)	0x71	R/W	TX direct-modulation parameter for 2Mcps mode Only '0x7F' allowed.

9.6. Miscellaneous Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
TST0 0x260	[7]	TSTEN	1	R/W	Test mode enable. 1: Disable 0: Enable
	[6]	(Reserved)	0	R/W	Only '0' allowed.
	[5]	TX_TST	0	R/W	In order to enable TX test mode, TS_TST is set to '1' along with setting TSTEN as '0'.
	[4:2]	(Reserved)	000	R/W	Only '000' allowed.
	[1]	TSTMD	0	R/W	When this field is set to '1', the O-QPSK modulation signal can be generated. When this field is set to '0', the single-tone signal is generated.
	[0]	(Reserved)	0	R/W	Only '0' allowed.
TST2 0x262	[7:6]	(Reserved)	00	R/W	Only '00' allowed.
	[5]	(Reserved)	1	R/W	Only '1' allowed.
	[4:0]	IFS	0x05	R/W	Inter-frame space for test mode. This can be configured in the unit of symbol duration (=16usec).
TST8 0x268	[7:0]	TSTPKTNUM	0x01	R/W	The number of the packet to be generated at test mode. For generating the packet infinitely, TSTPKTNUM is set to 0x00.
TSEN 0x2AB	[7]	TSEN	0	R/W	Enables(1) or disables(0) the temperature sensor output.
	[6:4]	(Reserved)	000	R/W	Only '000' allowed.
	[3:0]	(Reserved)	0000	R/W	Only '0000' allowed.
AVREG 0x2CF	[7]	(Reserved)	0	R	
	[6:5]	(Reserved)	0	R/W	Only '0' allowed.
	[4:2]	(Reserved)	100	R/W	Only '010' allowed.
	[1]	AVREGEN	0	R/W	Enables(1) or disables(0) analog voltage regulators When this bit sets, all analog regulators are turned on.
	[0]	OSC_OK	0	R	The stabilization status of the Crystal Oscillator. When the Crystal Oscillator is stabilized, this bit is automatically set high.

9.7. Status and Monitoring Registers

Address (hex)	Bit	Name	Reset Value	R/W	Description
AGCSTS2 0x272	[7:0]	RXENRG		R	Average energy level of the received RF signal at antenna.
AGCSTS3 0x275	[7:0]	PKTENRG		R	Average energy level of the received packet.
INTCON 0x27D	[6]	TXS intmsk	0	R/W	Enables(1) or disables(0) the TX Start interrupt mask.
	[5]	TXFAIL intmsk	0	R/W	Enables(1) or disables(0) the TX Fail interrupt mask.
	[4]	MDONFAIL_intmsk	0	R/W	Enables(1) or disables(0) the Modem On Fail interrupt mask.
	[3]	RXEND_intmsk	0	R/W	Enables(1) or disables(0) the RXEND interrupt mask.
	[2]	RXSTART_intmsk	0	R/W	Enables(1) or disables(0) the RXSTART interrupt mask.
	[1]	TXEND_intmsk	0	R/W	Enables(1) or disables(0) the TXEND interrupt mask.
	[0]	MDON_intmsk	0	R/W	Enables(1) or disables(0) the MDON(Modem On) interrupt mask.
INTIDX 0x27E	[1:0]	INTIDX		R	Stores the highest-priority interrupt source among the present interrupts. 0: MDON interrupt 1: TXEND interrupt 2: RXSTART interrupt 3: RXEND interrupt 4: MDONFAIL interrupt 5: TXFAIL interrupt 6: TXSTART interrupt
INTSTS 0x27F	[3:0]	INTSTS		R	Represents the interrupt source. '0' at each bit field means 'interrupt occur,' and '1' means 'interrupt not occur.' INTSTS[6]: TXSTART interrupt status. INTSTS[5]: TXFAIL interrupt status. INTSTS[4]: MDONFAIL interrupt status. INTSTS[3]: RXEND interrupt status INTSTS[2]: RXSTART interrupt status INTSTS[1]: TXEND interrupt status INTSTS[0]: MDON interrupt status
MACSTS 0x180	[0]	CRC_OK		R	When the CRC comparison matched, the CRC_OK is set to 1.

9.8. MAC Registers

9.8.1. MAC/Security Address FIFO Map

Address (hex)	Name	R/W	Description
0x300 ~ 0x3FF	MTXFIFO or STXFIFO	R/W	Random access space for MAC TX FIFO (MTXFIFO; SECMAP = 0) or TX security FIFO (STXFIFO; SECMAP = 1)
0x400 ~ 0x4FF	MRXFIFO or SRXFIFO	R/W	Random access space for MAC RX FIFO (MRXFIFO; SECMAP = 0) or RX security FIFO (SRXFIFO; SECMAP = 1)

9.8.2. Common Control Register Description

Address (hex)	Bit	Name	Reset Value	R/W	Description
KEY0 0x100 ~ 0x10F	[127:0]	KEY0		R/W	16-byte key (KEY0) for AES-128 0x10F: Most significant byte
RXNONCE 0x110 ~ 0x11C	[103:0]	RXNONCE		R/W	Used for decryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x11C: Most significant byte of source address 0x114: Most significant byte of frame counter 0x110: Key sequence counter
SAESBUF 0x120 ~ 0x12F	[127:0]	SAESBUF		R/W	Standalone encrypt/decrypt data buffer: After the AES-128 operation, the result is stored in this register. 0x12F: Most significant byte of plain-text and cipher-text
KEY1 0x130 ~ 0x13F	[127:0]	KEY1		R/W	16-byte key (KEY0) for AES-128 0x13F: Most significant byte
TXNONCE 0x140 ~ 0x14C	[103:0]	TXNONCE		R/W	Used for encryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x14C: Most significant byte of source address 0x144: Most significant byte of frame counter 0x140: Key sequence counter
IEEEADDR 0x150 ~ 0x157	[63:0]	IEEE_ADDR		R/W	64-bit IEEE address 0x157: Most significant byte
PANID 0x158 ~ 0x159	[15:0]	PAN_ID		R/W	16-bit PAN ID. 0x159: Most significant byte
SHORTADDR 0x15A ~ 0x15B	[15:0]	SHORT_ADDR		R/W	16-bit short (network) address 0x15B: Most significant byte
MACSTS 0x180	[7]	ENCDEC_STS	0	R	When this field is set to ‘1’, there is data in the encryption or decryption.
	[6]	TX_BUSY	0	R	When this field is set to ‘1’, data in the TX FIFO is transmitted to a modem.
	[5]	RX_BUSY	0	R	When this field is set to ‘1’, data is transmitted from a modem to the RX FIFO.
	[4]	SAES_DONE	0	R/W	When standalone AES operation is finished, this field is set to ‘1’.
	[3]	DECODE_OK	0	R	This field checks the validity of data according to the type of data received or the address mode. If there is no problem, this field is set to ‘1’.

<table>
<tr><td></td><td>[2]</td><td>ENC_DONE</td><td>0</td><td>R/W</td><td>When encryption operation is finished, this field is set to ‘1’.</td></tr>
<tr><td></td><td>[1]</td><td>DEC_DONE</td><td>0</td><td>R/W</td><td>When decryption operation is finished, this field is set to ‘1’.</td></tr>
<tr><td></td><td>[0]</td><td>CRC_OK</td><td>0</td><td>R/W</td><td>If there is no problem for checking CRC of received packet, this field is set to ‘1’.</td></tr>
<tr><td>SAES
0x18E</td><td>[7:1]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td></td><td>[0]</td><td>SAES</td><td>0</td><td>W</td><td>When this field is set to ‘1’, the AES operation is done by data in SAESBUF and KEY selected by the SA_KEYSEL. This field is cleared automatically.</td></tr>
<tr><td>RST
0x190</td><td>[7]</td><td>RST_FIFO</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the MAC FIFO is initialized.</td></tr>
<tr><td></td><td>[6]</td><td>RST_TSM</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the MAC TX state machine is initialized.</td></tr>
<tr><td></td><td>[5]</td><td>RST_RSM</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the MAC RX state machine is initialized.</td></tr>
<tr><td></td><td>[4]</td><td>RST_AES</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the AES engine is initialized.</td></tr>
<tr><td></td><td>[3:0]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td>CTRL
0x191</td><td>[7:5]</td><td>(Reserved)</td><td>0</td><td>R</td><td></td></tr>
<tr><td></td><td>[4]</td><td>PREVENT_ACK</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the RX interrupt doesn’t occur when the DSN field of received ACK packet is different from the value in MACDSN register during packet reception.</td></tr>
<tr><td></td><td>[3]</td><td>PAN_COORDINATOR</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, function for PAN coordinator is enabled.</td></tr>
<tr><td></td><td>[2]</td><td>ADR_DECODE</td><td>1</td><td>R/W</td><td>When this field is set to ‘1’, the RX interrupt doesn’t occur when address information of the received packet is not matched with device itself.</td></tr>
<tr><td></td><td>[1]</td><td>AUTO_CRC</td><td>1</td><td>R/W</td><td>When this field is set to ‘1’, the RX interrupt doesn’t occur when the CRC of the received packet is not valid.</td></tr>
<tr><td></td><td>[0]</td><td>AUTO_ACK</td><td>0</td><td>R/W</td><td>When this field is set to ‘1’, the ACK packet is automatically sent when the designated packet is correctly received.</td></tr>
<tr><td>DSN
0x192</td><td>[7:0]</td><td>MACDSN</td><td>0x00</td><td>R/W</td><td>If the DSN field of the received ACK packet is not equal to MACDSN, the RX interrupt does not occurred.</td></tr>
<tr><td>SEC
0x193</td><td>[7]</td><td>SA_KEYSEL</td><td>0</td><td>R/W</td><td>Selects the KEY value for standalone SAES operation. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td></tr>
<tr><td></td><td>[6]</td><td>TX_KEYSEL</td><td>0</td><td>R/W</td><td>Selects the KEY value for AES operation during packet transmission. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td></tr>
<tr><td></td><td>[5]</td><td>RX_KEYSEL</td><td>0</td><td>R/W</td><td>Selects the KEY value for AES operation when packet reception. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td></tr>
<tr><td></td><td>[4:2]</td><td>SEC_M</td><td>000</td><td>R/W</td><td>In CBC-MAC operation, it represents the data length used in the authentication field in byte.
<table><tr><th>SEC_M</th><th>Authentication field length</th></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>10</td></tr><tr><td>5</td><td>12</td></tr><tr><td>6</td><td>14</td></tr><tr><td>7</td><td>16</td></tr></table></td></tr>
<tr><td></td><td>[1:0]</td><td>SEC_MODE</td><td>00</td><td>R/W</td><td>Security mode.
00: No security
01: CBC-MAC mode
10: CTR mode
11: CCM mode</td></tr>
</table>

TXL 0x194	[7]	(Reserved)	0	R	
	[6:0]	TXL	0x00	R/W	This field represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows. Security mode: CTR It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO. Security mode: CBC-MAC It represents the number of byte between length byte and the data to be authenticated. Security mode: CCM It represents the length of data which is used not in encoding or decoding but in authentication.
RXL 0x195	[7]	(Reserved)	0	R	
	[6:0]	RXL	0x00	R/W	This field represents the length used in the AES operation for the received packet and it has a different meaning for each security mode as follows. Security mode: CTR It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO. Security mode: CBC-MAC It represents the number of bytes between length byte and the data to be authenticated. Security mode: CCM It represents the length of data which is used not in encoding or decoding but in authentication.
SECMAP 0x19F	[7:1]	(Reserved)	0x0	R	
	[0]	SECMAP	0	R/W	Security control/FIFO selection 0: MAC control / MAC FIFO selected 1: Security control / security FIFO selected

9.8.3. RX FIFO control Register Description

Address (hex)	Bit	Name	Reset Value	R/W	Description
MRFCPOP 0x080	[7:0]	MRFCPOP		R	Through this register, data in RX FIFO is read. The RX FIFO data is read with either the single register access (this register) or the burst mode of the SPI
MRFCWP 0x081	[7:0]	MRFCWP	0x00	R/W	RX FIFO write pointer Total size of the write pointer is 9-bit with MRFCWP8 in 0x084 register. It is increased by ’1’ whenever data is written to the RX FIFO.
MRFCRP 0x082	[7:0]	MRFCRP	0x00	R/W	RX FIFO read pointer Total size of the read pointer is 9-bit with MRFCRP8 in 0x084 register. It is increased by ’1’ whenever data is read from the RX FIFO.
MRFCCTL 0x083	[7:3]	(Reserved)		R	
	[2]	ASA	0x1	R/W	When this field is set to ‘1’, it automatically sets the starting address of a packet and the length of a packet decrypted by the AES engine to the information of the received packet.
	[1]	ENA	0x1	R/W	When this field is set to ‘1’, RX FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to ‘1’, MRFCWP, MRFCRP, 0x084, MRFCSIZE registers are initialized.

MRFCSTATUS 0x084	[7]	MRFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with MRFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	MRFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with MRFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	RX FIFO full This field is set to '1' when data size in RX FIFO is 256 byte.
	[0]	EMPTY	0x0	R	RX FIFO empty This field is set to '1' when data size in RX FIFO is '0'.
MRFCSIZE 0x085	[7:0]	MRFCSIZE	0x00	R/W	This field represents the number of valid data bytes of RX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MRFCWP and MRFCRP.
MRFCROOM 0x086	[7:0]	MRFCROOM	0x00	R/W	Threshold control for RX FIFO empty and full

9.8.4. TX FIFO Control Register Description

Address (hex)	Bit	Name	Reset Value	R/W	Description
MTFCPUSH 0x000	[7:0]	MTFCPUSH		W	When data is written to this register, it is stored in TX FIFO. The TX FIFO data is written with either the single register access (this register) or the burst mode of the SPI
MTFCWP 0x001	[7:0]	MTFCWP	0x00	R/W	TX FIFO write pointer Total size of the write pointer is 9-bit with MTFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the TX FIFO.
MTFCRP 0x002	[7:0]	MTFCRP	0x00	R/W	TX FIFO read pointer Total size of the read pointer is 9-bit with MTFCRP8 in 0x004 register. It is increased by '1' whenever data is read from the TX FIFO.
MTFCCTL 0x003	[7:3]	(Reserved)		R	
	[2]	ASA	0x1	R/W	When this field is set to '1', it automatically sets the starting address of a packet and the length of a packet encrypted by the AES engine to the information of the packet which is to be transmitted.
	[1]	ENA	0x1	R/W	When this field is set to '1', TX FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to '1', MTFCWP, MTFCRP, 0x004, MTFCSIZE registers are initialized.
MTFCSTATUS 0x004	[7]	MTFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with MTFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	MTFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with MTFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	TX FIFO full This field is set to '1' when data size in TX FIFO is 256 byte.
	[0]	EMPTY	0x0	R	TX FIFO empty This field is set to '1' when data size in TX FIFO is '0'.
MTFCSIZE 0x005	[7:0]	MTFCSIZE	0x00	R/W	This field represents the number of valid data bytes of TX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between

					MTFCWP and MTFCRP.
MTFCROOM 0x006	[7:0]	MTFCROOM	0x00	R/W	Threshold control for TX FIFO empty and full
AACKFC 0x009-0x00A	[15:0]	AACKFC	0x00	R/W	Frame control field for transmitted auto-ACK packet. Most significant byte is 0x00A.
AACKDSN 0x00B	[7:0]	AACKDSN	0x00	R/W	DSN value for transmitted auto-ACK packet
AACKSTA 0x00C	[7:1]	(Reserved)	0x00	R	
	[0]	PENDING	0	R/W	Frame-pending subfield for transmitted auto-ACK packet

9.8.5. RX Security FIFO Control Register Description

Address (hex)	Bit	Name	Reset Value	R/W	Description
SRFCPOP 0x080	[7:0]	SRFCPOP		R	Through this register, data in RX security FIFO is read. The RX security FIFO data is read with either the single register access (this register), the burst mode of the SPI, or direct transfer between the RX security FIFO and the RX FIFO.
SRFCWP 0x081	[7:0]	SRFCWP	0x00	R/W	RX security FIFO write pointer Total size of the write pointer is 9-bit with SRFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the RX security FIFO.
SRFCRP 0x082	[7:0]	SRFCRP	0x00	R/W	RX security FIFO read pointer Total size of the read pointer is 9-bit with SRFCRP8 in 0x004 register. It is increased by '1' whenever data is read from the RX security FIFO.
SRFCCTL 0x083	[7:2]	(Reserved)		R	
	[1]	ENA	0x1	R/W	When this field is set to '1', RX security FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to '1', SRFCWP, SRFCRP, 0x004, SRFCSIZE registers are initialized.
SRFCSTATUS 0x084	[7]	SRFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with SRFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	SRFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with SRFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	RX security FIFO full This field is set to '1' when data size in RX security FIFO is 256 byte.
	[0]	EMPTY	0x0	R	RX security FIFO empty This field is set to '1' when data size in RX security FIFO is '0'.
SRFCSIZE 0x085	[7:0]	SRFCSIZE	0x00	R/W	This field represents the number of valid data bytes of RX security FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between SRFCWP and SRFCRP.
SRFCROOM 0x086	[7:0]	SRFCROOM	0x00	R/W	Threshold control for RX security FIFO full and empty
SRFCSECBASE	[7:0]	SRFCSECBASE	0x00	R/W	Frame base address for decryption

0x087					
SRFCSECLEN 0x088	[7:0]	SRFCSECLEN	0x00	R/W	Frame length for decryption
SRFDMALEN 0x089	[7:0]	SRFDMALEN	0x00	R/W	Data size of direct transfer between the RX security FIFO and the RX FIFO.
SRFDMACTL 0x08A	[7:3]	(Reserved)		R	
	[2]	DONE	0x0	R	This field is set to '1', when direct transfer between the RX security FIFO and the RX FIFO is done
	[1]	BUSY	0x0	R	When this field is set to '1', data transfer between the RX security FIFO and the RX FIFO is activated.
	[0]	ENA	0x0	W	Enable the direct transfer between the RX security FIFO and the RX FIFO

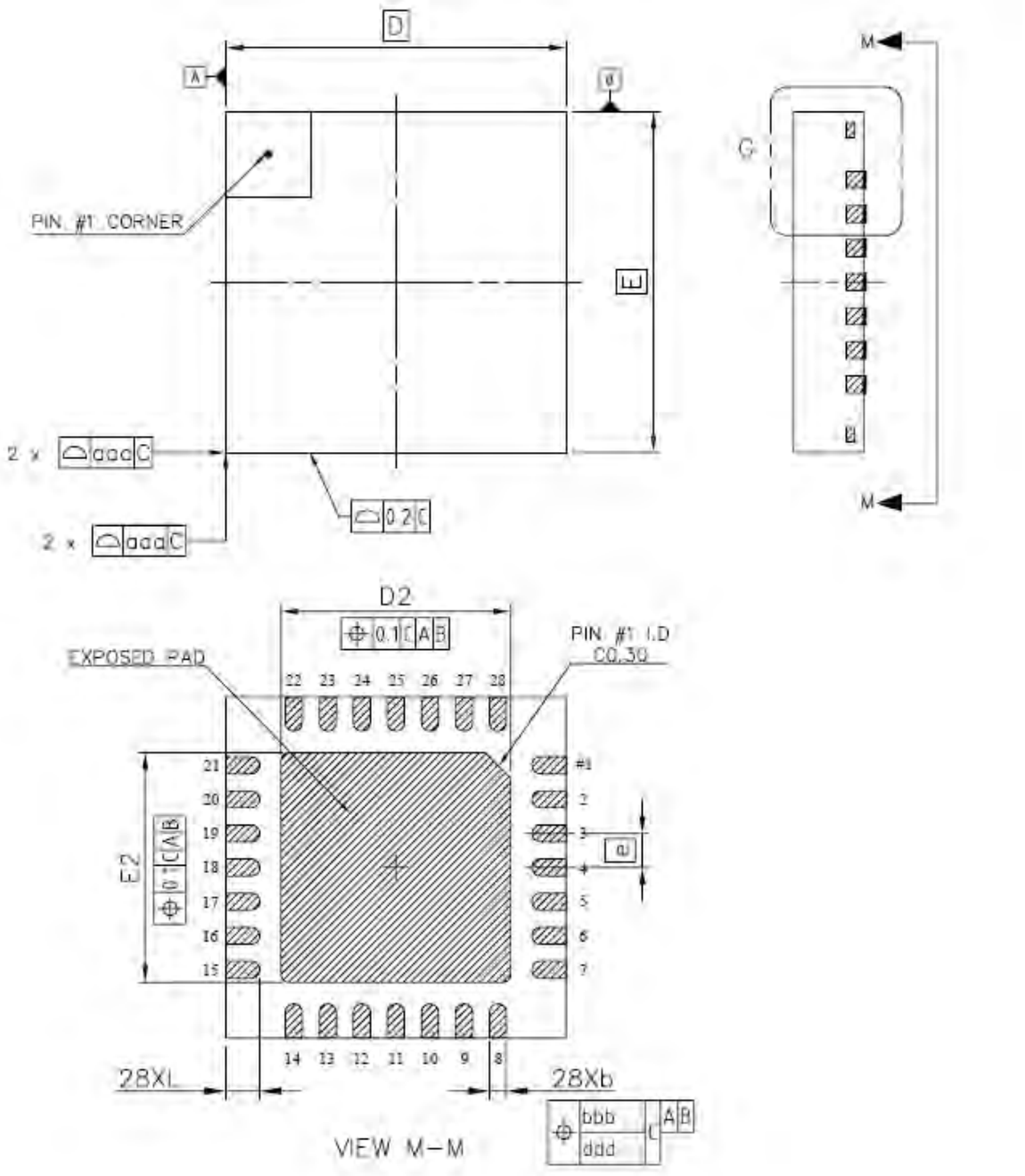
9.8.6. TX Security FIFO Control Register Description

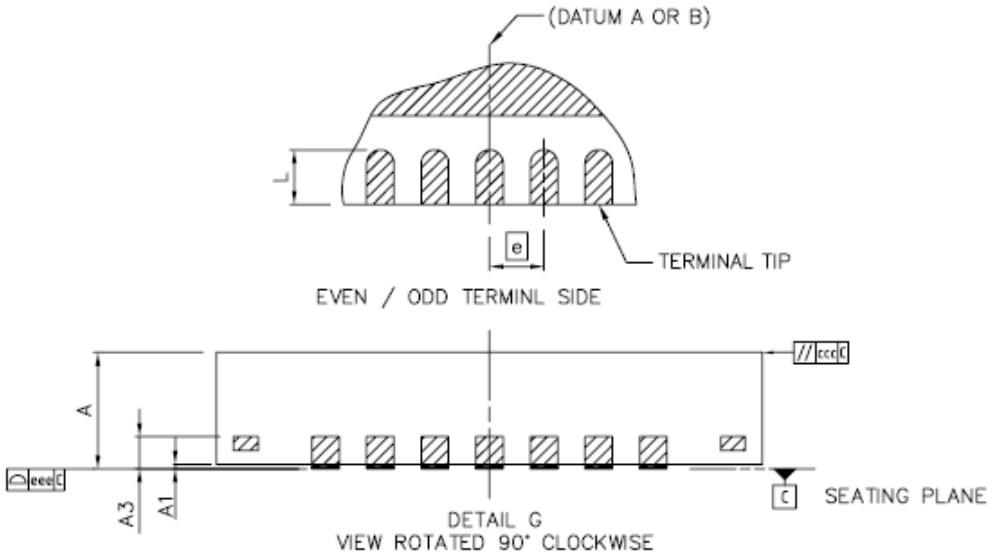
Address (hex)	Bit	Name	Reset Value	R/W	Description
STFCPUSH 0x000	[7:0]	STFCPUSH		W	When data is written to this register, it is stored in TX security FIFO. The TX security FIFO data is written with the single register access (this register), the burst mode of the SPI, or direct transfer between the TX security FIFO and the TX FIFO.
STFCWP 0x001	[7:0]	STFCWP	0x00	R/W	TX security FIFO write pointer Total size of the write pointer is 9-bit with STFCWP8 in 0x004 register. It is increased by '1' whenever data is written to the TX security FIFO.
STFCRP 0x002	[7:0]	STFCRP	0x00	R/W	TX security FIFO read pointer Total size of the read pointer is 9-bit with STFCRP8 in 0x004 register. It is increased by '1' whenever data is read from the TX security FIFO.
STFCCTL 0x003	[7:2]	(Reserved)		R	
	[1]	ENA	0x1	R/W	When this field is set to '1', TX security FIFO is enabled.
	[0]	CLR	0x0	R/W	When this field is set to '1', STFCWP, STFCRP, 0x004, STFCSIZE registers are initialized.
STFCSTATUS 0x004	[7]	STFCWP8	0x0	R/W	Total size of the write pointer is 9-bit address with STFCWP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[6]	STFCRP8	0x0	R/W	Total size of the read pointer is 9-bit address with STFCRP. This field is MSB, and is used to detect wrap-around of a circular FIFO.
	[5:2]	(Reserved)		R	
	[1]	FULL	0x0	R	TX security FIFO full This field is set to '1' when data size in TX security FIFO is 256 byte.
	[0]	EMPTY	0x0	R	TX security FIFO empty This field is set to '1' when data size in TX security FIFO is '0'.
STFCSIZE 0x005	[7:0]	STFCSIZE	0x00	R/W	This field represents the number of valid data bytes of TX security FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between STFCWP and STFCRP.
STFCROOM 0x006	[7:0]	STFCROOM	0x00	R/W	Threshold control for TX security FIFO full and empty
STFCSECBASE 0x007	[7:0]	STFCSECBASE	0x00	R/W	Frame base address for encryption

MTFCSECLEN 0x008	[7:0]	STFCSECLEN	0x00	R/W	Frame length for encryption
STFDMALEN 0x009	[7:0]	STFDMALEN	0x00	R/W	Data size of direct transfer between the TX security FIFO and the TX FIFO.
STFDMACTL 0x00A	[7:3]	(Reserved)		R	
	[2]	DONE	0x0	R	This field is set to ‘1’, when direct transfer between the TX security FIFO and the TX FIFO is done
	[1]	BUSY	0x0	R	When this field is set to ‘1’, data transfer between the TX security FIFO and the TX FIFO is activated.
	[0]	ENA	0x0	W	Enable the direct transfer between the TX security FIFO and the TX FIFO

10. PACKAGE INFORMATION

10.1. Dimensions





DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

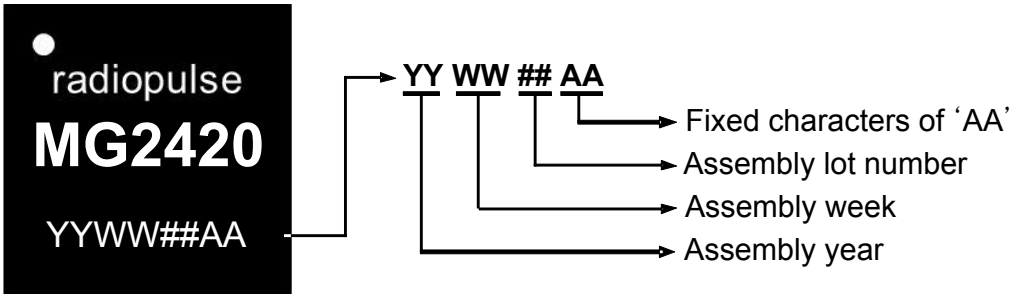
3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220

10.2. Marking



11. ABBREVIATIONS

ACK	-	Acknowledgement
ADC	-	Analog-to-digital converter
AES	-	Advanced encryption standard
AGC	-	Automatic gain controller
AVREG	-	Voltage regulator for analog blocks
CBC-MAC	-	Cipher block chaining message authentication code
CCA	-	Clear channel assessment
CRC	-	Cyclic redundancy check
DVREG	-	Voltage regulator for digital blocks
EVM	-	Error vector magnitude
FEC	-	Forward error correction
FIFO	-	First in first out
FSM	-	Finite state machine
GPIO	-	General purpose input output
IRQ	-	Interrupt request
ISM	-	Industrial, scientific, and medical
LNA	-	Low-noise amplifier
LO	-	Local oscillator
LPF	-	Low-pass filter
LQI	-	Link quality indicator
MAC	-	Medium access control
MSK	-	Minimum shift keying
O-QPSK	-	Offset quadrature phase shift keying
PA	-	Power amplifier
PER	-	Packet error rate
PHY	-	Physical layer
PLL	-	Phase locked loop
PSDU	-	PHY service data unit
QFN	-	Quad flat no-lead package
RF	-	Radio frequency
RSSI	-	Received signal strength indicator
RX	-	Receiver
SFD	-	Start-of-frame delimiter
SPI	-	Serial peripheral interface
TRSW	-	Transmit/receive switch
TX	-	Transmitter
VCO	-	Voltage-controlled oscillator
VGA	-	Variable gain amplifier
XOSC	-	Crystal oscillator

12. REFERENCES

[1] IEEE Standard 802.15.4™ – 2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs).

[2] ETSI EN 300 440-1 (2010-04) : Electromagnetic compatibility and Radio spectrum Matters (ERM); Short range devices; Radio equipment to be used in the 1 GHz to 40 GHz frequency range; Part 1: Technical characteristics and test methods.

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About RadioPulse Inc.

RadioPulse is a Being Wireless solution provider offering wireless communication & network technologies and developing next generation wireless networking technologies.

The new wireless networking solutions envisioned by RadioPulse will enable user to enjoy wireless technologies with easy interface.

Founded in April of 2003, the company maintains it headquarters and R&D center in Seoul, Korea.