DATA SHEET

TDA8783

40 Msps, 10-bit analog-to-digital interface for CCD cameras

Product specification
Supersedes data of 1999 Jun 25

2002 Oct 23

Philips
Semiconductors

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40 Msps, 10-bit analog-to-digital interface for CCD cameras

TDA8783

FEATURES

- Correlated Double Sampling (CDS), AGC, 10-bit ADC and reference regulator included, adjustable bandwidth (CDS and AGC)
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 40 MHz
- AGC gain from 4.5 to 34.5 dB (in 0.1 dB steps)
- CDS programmable bandwidth from 4 to 120 MHz
- AGC programmable bandwidth from 4 to 54 MHz
- Standby mode available for each block for power saving applications 20 mW (typ.)
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 483 mW (typ.)
- 5 V operation and 2.5 to 5.25 V operation for the digital outputs
- TTL compatible inputs, TTL and CMOS compatible outputs.

APPLICATIONS

- CCD camera systems.

GENERAL DESCRIPTION

The TDA8783 is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC and a low-power 10-bit Analog-to-Digital Converter (ADC) together with its reference voltage regulator.

The AGC and CDS have a bandwidth circuit controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

An additional 8-bit DAC is provided for additional system controls; its output voltage range is 1.4 V (p-p) which is available at pin OFDOUT.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8783HL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital outputs supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current		–	78	95	mA
I_{CCD}	digital supply current		–	18	20	mA
I_{CCO}	digital outputs supply current	f_{CLK} = 27 MHz; C_L = 20 pF; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	CDS input voltage (peak-to-peak value)		–	400	1200	mV
G_{CDS}	CDS output amplifier gain		–	6	–	dB
$f_{CLK(max)}$	maximum clock frequency	$f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 54 MHz	40	–	–	MHz
AGC_{dyn}	AGC dynamic range		–	30	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output (RMS value)	gain = 4.5 dB; $f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 40 MHz	–	0.125	–	LSB
P_{tot}	total power consumption		–	483	–	mW

BLOCK DIAGRAM

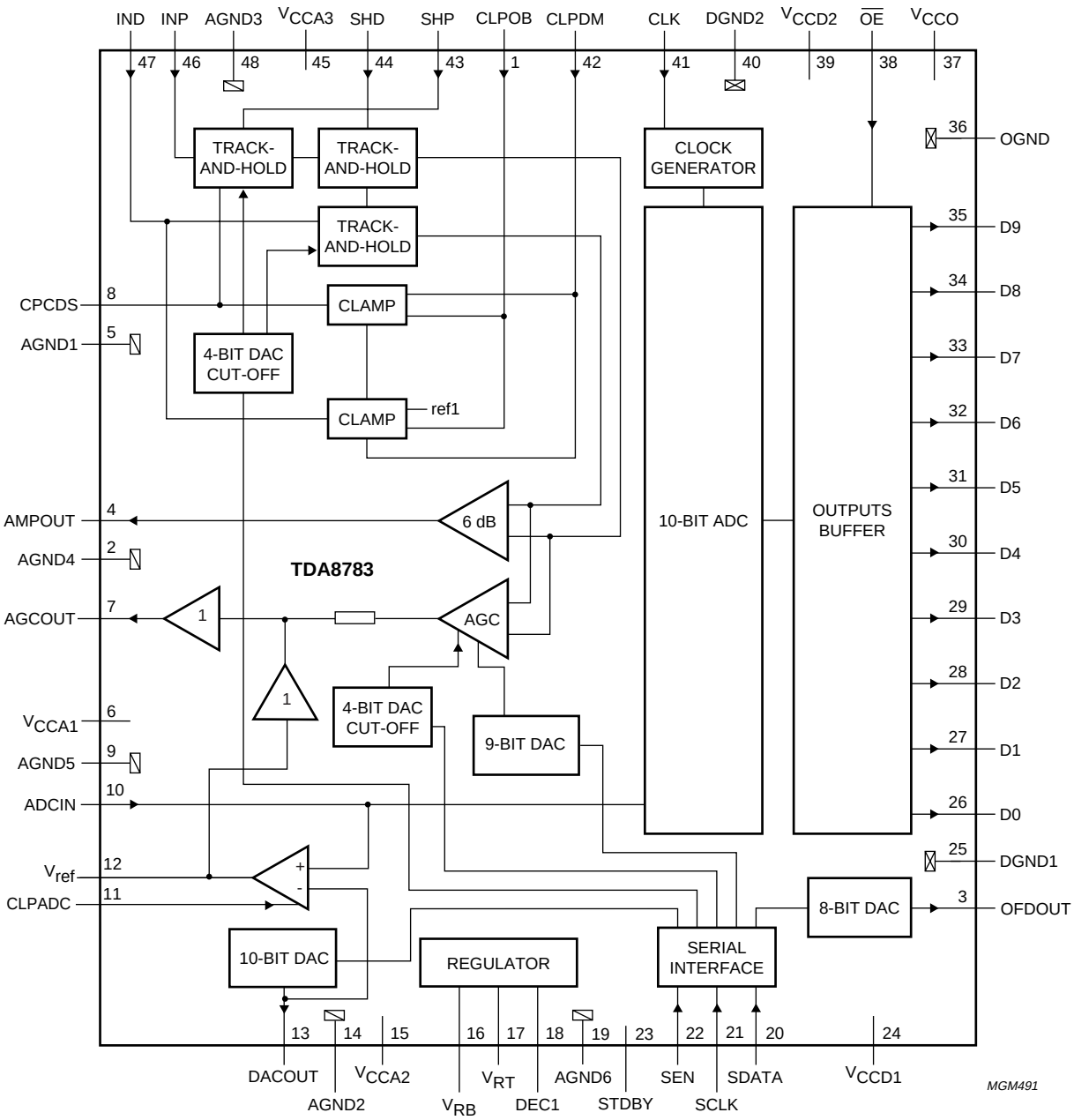


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLPOB	1	clamp pulse input at optical black
AGND4	2	analog ground 4
OFDOUT	3	analog output of the additional 8-bit control DAC (controlled via the serial interface)
AMPOUT	4	CDS amplifier output (fixed gain = 6 dB)
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGCOUT	7	AGC amplifier signal output
CPCDS	8	clamp storage capacitor pin
AGND5	9	analog ground 5
ADCIN	10	ADC analog signal input from AGCOUT via a short circuit
CLPADC	11	clamp control input for ADC analog input signal clamp (used with a capacitor from V_{ref} to ground)
V_{ref}	12	ADC input clamp reference voltage (normally connected to pin V_{RB} or DACOUT, or connected to ground via a capacitor)
DACOUT	13	DAC output for ADC clamp level
AGND2	14	analog ground 2
V_{CCA2}	15	analog supply voltage 2
V_{RB}	16	ADC reference voltage (BOTTOM) code 0
V_{RT}	17	ADC reference voltage (TOP) code 1023
DEC1	18	decoupling 1 (decoupled to ground via a capacitor)
AGND6	19	analog ground 6
SDATA	20	serial data input for the 4 control DACs (9-bit DAC for AGC gain, 8-bit DAC for frequency cut-off; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the standby mode per block and edge pulse control); see Fig.3, Fig.4 and Table 1
SCLK	21	serial clock input for the control DACs and their serial interface; see Fig.3, Fig.4 and Table 1
SEN	22	enable input for the serial interface shift register (active when SEN = logic 0); see Fig.3, Fig.4 and Table 1
STDBY	23	standby control (active HIGH); all the output bits are logic 0 when standby is enabled
V_{CCD1}	24	digital supply voltage 1
DGND1	25	digital ground 1
D0	26	ADC digital output 0 (LSB)
D1	27	ADC digital output 1
D2	28	ADC digital output 2
D3	29	ADC digital output 3
D4	30	ADC digital output 4
D5	31	ADC digital output 5
D6	32	ADC digital output 6
D7	33	ADC digital output 7
D8	34	ADC digital output 8
D9	35	ADC digital output 9 (MSB)
OGND	36	digital output ground

SYMBOL	PIN	DESCRIPTION
V_{CCO}	37	digital output supply voltage
$\overline{OE}$	38	output enable (active LOW: digital outputs active; active HIGH: digital outputs high impedance)
V_{CCD2}	39	digital supply voltage 2
DGND2	40	digital ground 2
CLK	41	ADC clock input
CLPDM	42	clamp pulse input at dummy pixel
SHP	43	pre-set sample-and-hold pulse input
SHD	44	data sample-and-hold pulse input
V_{CCA3}	45	analog supply voltage 3
INP	46	pre-set input signal from CCD
IND	47	data input signal from CCD
AGND3	48	analog ground 3

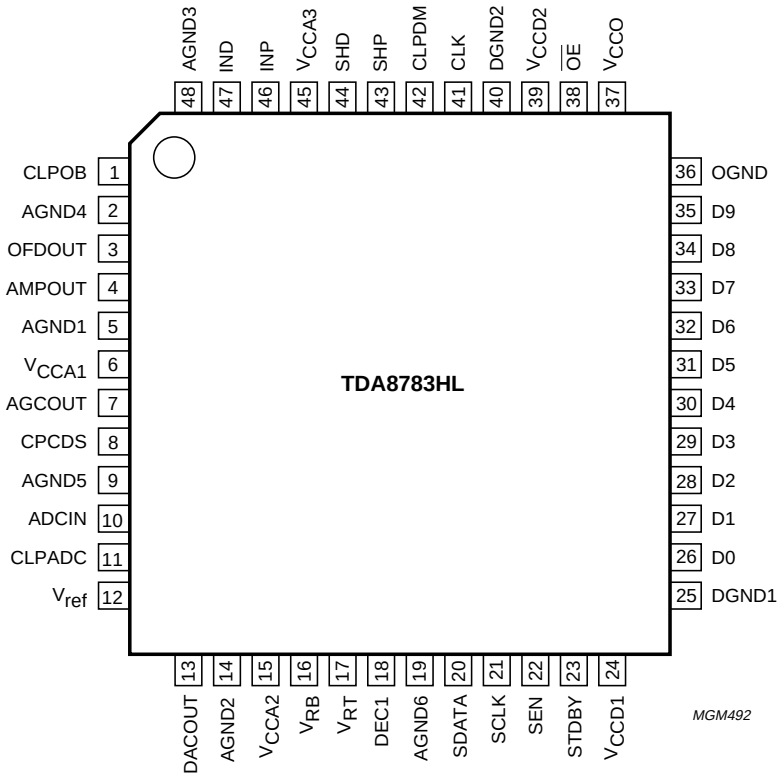


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		–1.0	+1.0	V
	between V_{CCA} and V_{CCO}		–1.0	+4.0	V
	between V_{CCD} and V_{CCO}		–1.0	+4.0	V
V_i	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_o	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

CHARACTERISTICS

V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3 V; f_{CLK} = 27 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5	5.25	V
V_{CCD}	digital supply voltage		4.75	5	5.25	V
V_{CCO}	digital outputs supply voltage		2.5	3	5.25	V
I_{CCA}	analog supply current		–	78	95	mA
I_{CCD}	digital supply current		–	18	20	mA
I_{CCO}	digital outputs supply current	C_L = 20 pF on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: CLK (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} = 0.8 V	–1	–	+1	µA
I_{IH}	HIGH-level input current	V_{CLK} = 2.0 V	–	–	20	µA
Z_i	input impedance	f_{CLK} = 27 MHz	–	46	–	kΩ
C_i	input capacitance	f_{CLK} = 27 MHz	–	1	–	pF
INPUTS: SHP AND SHD						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	–	–6	–	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	–	0	–	µA
INPUTS: SEN, SCLK, SDATA, $\overline{OE}$, STDBY, CLPDM, CLPOB AND CLPADC						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_i	input current		–2	–	+2	µA
Correlated Double Sampling (CDS); note 1						
$V_{i(CDS)(p-p)}$	CDS input amplitude pin 47 (peak-to-peak value)		–	400	1200	mV
I_{CPCDS}, I_{INP}, I_{IND}	input current pins 8, 46 and 47		–2	–	+2	µA
$t_{CDS(min)}$	CDS control pulses minimum active time	$f_{i(CDS1,2)}$ = $f_{CLK(pix)}$; $V_{i(CDS)(p-p)}$ = 600 mV black-to-white transition in 1 pixel (±1 LSB typ.); $f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 54 MHz	8	–	–	ns
t_{hd1}	hold time INP compared to control pulse SHP	see Fig.5	–	1	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{hd2}	hold time of IND compared to control pulse SHD	see Fig.5	–	1	–	ns
$t_{set(CDS)}$	CDS settling time	see Fig.12; control DAC 4 bits input code; AGC gain = 0 dB; $f_{cut(AGC)}$ = 54 MHz; $V_{i(CDS)}$ = 600 mV (p-p) black-to-white transition in 1 pixel (±1 LSB typ.)				
		0000	–	8	–	ns
		0001	–	21	–	ns
		0010	–	42	–	ns
		0011	–	52	–	ns
		0100	–	82	–	ns
		0111	–	94	–	ns
		1000	–	195	–	ns
		1011	–	219	–	ns
		1111	–	280	–	ns
Amplifier outputs						
G_{AMPOUT}	output amplifier gain		–	6	–	dB
Z_{AMPOUT}	output amplifier impedance		–	300	–	Ω
$V_{AMPOUT(p-p)}$	output amplifier dynamic voltage (peak-to-peak value)		–	2.4	–	V
$V_{AMPOUT(bl)}$	output amplifier black level voltage		–	1.5	–	V
$V_{AGCOUT(p-p)}$	AGC output amplifier dynamic voltage level (peak-to-peak value)		–	2000	–	mV
$V_{AGCOUT(bl)}$	AGC output amplifier black level voltage	V_{ref} connected to DACOUT	–	V_{ref}	–	V
Z_{AGCOUT}	AGC output amplifier output impedance	at 10 kHz	–	5	–	Ω
I_{AGCOUT}	AGC output static drive current	static	–	–	1	mA
$G_{AGC(min)}$	minimum gain of AGC circuit	AGC DAC input code = 00 (9-bit control); see Fig.7	–	4.5	–	dB
$G_{AGC(max)}$	maximum gain of AGC circuit	AGC DAC input code ≥ 319 (9-bit control); see Fig.7	–	34.5	–	dB
$f_{cut(AGC)}$	cut-off frequency AGC	4-bit control DAC				
		input code = 00	–	54	–	MHz
		input code = 15	–	4	–	MHz
		other codes see Fig.13				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamps						
$g_{m(ADC)}$	ADC clamp transconductance	at clamp level	–	7	–	mS
$g_{m(CDS)}$	CDS clamp transconductance	at clamp level	–	1.5	–	mS
Analog-to-Digital Converter (ADC)						
$f_{CLK(max)}$	maximum clock frequency		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		12	–	–	ns
t_{CPL}	clock pulse width LOW		12	–	–	ns
SR_{CLK}	clock input slew rate (rising and falling edge)	10% to 90%	0.5	–	–	V/ns
$V_{i(ADC)(p-p)}$	ADC input voltage level (peak-to-peak value)		–	2	–	V
V_{RB}	ADC reference voltage output code 0		–	1.5	–	V
V_{RT}	ADC reference voltage output code 1023		–	3.5	–	V
I_{ADCIN}	ADC input current		–2	–	+120	µA
INL	integral non-linearity	ramp input	–	±0.6	±1.5	LSB
DNL	differential non-linearity	ramp input	–	±0.2	±0.75	LSB
$t_{d(s)}$	sampling delay time		–	–	5	ns
Total chain characteristics (CDS + AGC + ADC)						
t_d	delay between SHD and CLK	50% at rising edges CLK and SHD: transition full scale code 0 to 1023; $f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 54 MHz; $V_{i(CDS)}$ = 600 mV	–	30	–	ns
$N_{tot(rms)}$	total output noise (RMS value)	$f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 40 MHz; note 2				
		G_{AGC} = 4.5 dB	–	0.125	–	LSB
		G_{AGC} = 34.5 dB	–	1.6	–	LSB
$V_{offset(fl-d)}$	maximum offset between CCD floating level and CCD dark pixel level		–200	–	+200	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	AGC gain = 34.5 dB	–	125	–	µV
		AGC gain = 4.5 dB	–	150	–	µV
Digital-to-Analog Converter (OFDOUT)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)		–	1.4	–	V
$V_{OFDOUT(0)}$	DC output voltage for code 0		–	2.3	–	V
$V_{OFDOUT(255)}$	DC output voltage for code 255		–	3.7	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_{OFDOUT}	additional 8-bit control DAC (OFD) output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output current drive	static	–	–	50	µA
ADC clamp control DAC (see Fig.8)						
$V_{DACOUT(p-p)}$	ADC clamp 10-bit control DAC output voltage (peak-to-peak value)		–	1	–	V
V_{DACOUT}	DC output voltage	code 0	–	1.5	–	V
		code 1023	–	2.5	–	V
Z_{DACOUT}	ADC clamp control DAC output impedance		–	–	250	Ω
I_{DACOUT}	DAC output current drive	static	–	–	50	µA
OFE_{LOOP}	maximum offset error of DAC + ADC clamp loop	code 0	–	±5	–	LSB
		code 1023	–	±5	–	LSB
Digital outputs (f_{CLK} = 40 MHz; C_L = 20 pF); note 3						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
I_{OZ}	output current in 3-state mode	0 V < V_o < V_{CCO}	–20	–	+20	µA
$t_{o(h)}$	output hold time		8	–	–	ns
$t_{o(d)}$	output delay time	C_L = 20 pF; V_{CCO} = 5 V	–	17	23	ns
		C_L = 10 pF; V_{CCO} = 5 V	–	15	21	ns
		C_L = 20 pF; V_{CCO} = 3 V	–	20	29	ns
		C_L = 10 pF; V_{CCO} = 3 V	–	17	25	ns
		C_L = 20 pF; V_{CCO} = 2.5 V	–	22	33	ns
		C_L = 10 pF; V_{CCO} = 2.5 V	–	18	28	ns
Serial interface						
$f_{SCLK(max)}$	maximum frequency of serial interface		5	–	–	MHz

Notes

1. More information about CDS related signals is available in the following figures: The clamp current for pin CPCDS is given in Fig. 9, clamp current for pins IND and INP in Fig 10 and for clamp current for pin V_{ref} in Fig 11. The CDS output amplitude is shown in Fig. 14
2. Noise measurement at ADC outputs: the coupling capacitor at the input is connected to ground, so that only the noise contribution of the front-end is evaluated. The front-end operates at 18 Mpix with a line of 1024 pixels. The first 40 are used to run CLPOB and the last 40 to run CLPDM. Data at the ADC outputs is measured during the other pixels. The differences between the types of codes statistic is then computed; the result is the noise. No quantization noise is taken into account as no signal is input. Figure15 gives noise figure graphs with signal input.
3. Depending on operating pixel frequency, the output voltage and capacitance must be determined according to the output delay timings ($t_{o(d)}$), see Fig.5.

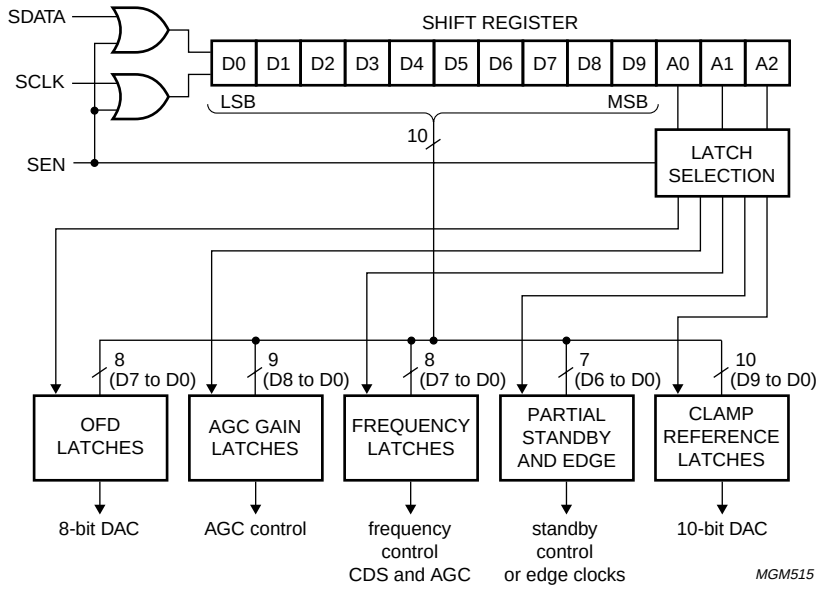
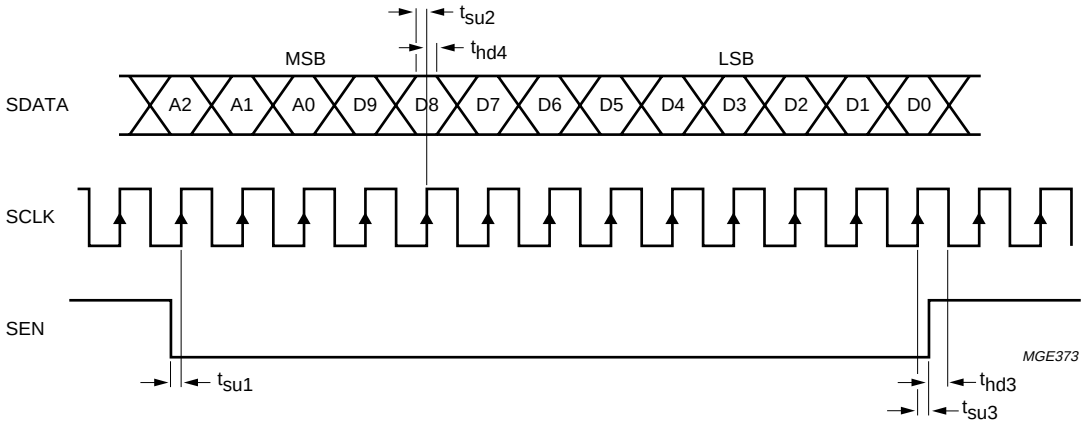


Fig.3 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 4$ ns (min.); $t_{hd3} = t_{hd4} = 4$ ns (min.).

Fig.4 Loading sequence of control DACs input data via the serial interface.

Table 1 Serial interface programming

ADDRESS BITS			DATA BITS D9 to D0
A2	A1	A0	
0	0	0	OFD output control (D7 to D0).
0	0	1	Cut-off frequency of CDS and AGC. Only the 4 LSBs (D3 to D0) are used for CDS. D4 to D7 are used for AGC. D8 and D9 should be set to logic 0.
0	1	0	AGC gain control (D8 to D0).
0	1	1	Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Edge control for pulses SHP, SHD, CLAMP and clock ADC: D0 = 1: CDS + AGC in standby; $I_{CCA} + I_{CCD}$ = 35 mA D1 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD}$ = 95 mA D2 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD}$ = 95.5 mA D3 = 1: SHP and SHD activated with falling edge (for positive pulse) D4 = 1: CLPDM, CLPOB and CLPADC activated on HIGH level; note 1 D5 = 0: CLKADC activated with falling edge D6 must be set to logic 0.
1	0	0	Clamp reference DAC (D9 to D0).

Note

1. When CLPADC is HIGH (D4 = 1: serial interface), the ADC input is clamped to voltage level V_{ref}. V_{ref} is connected to ground via a capacitor.

Table 2 Standby selection

STDBY	DATA BITS D9 to D0	$I_{CCA} + I_{CCD}$ (TYP.)
1	LOW	4 mA
0	active	96 mA

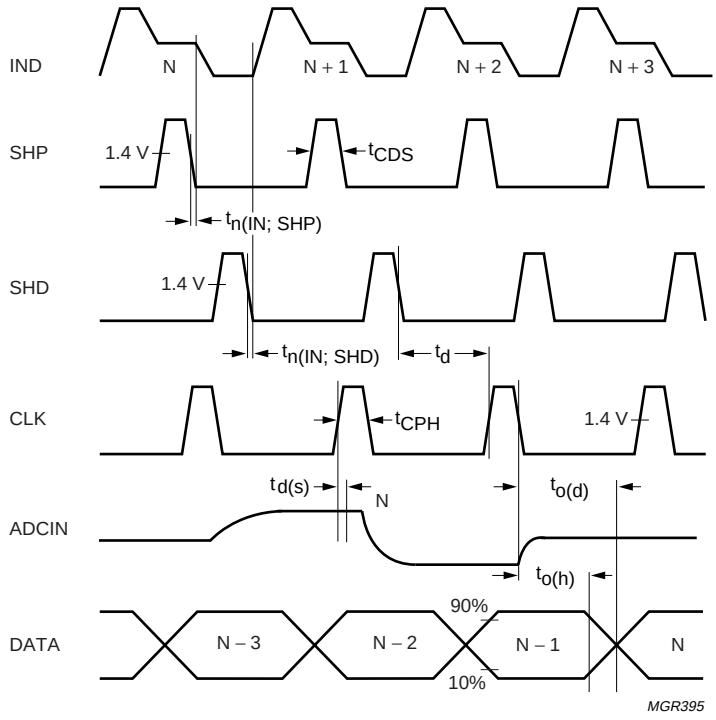
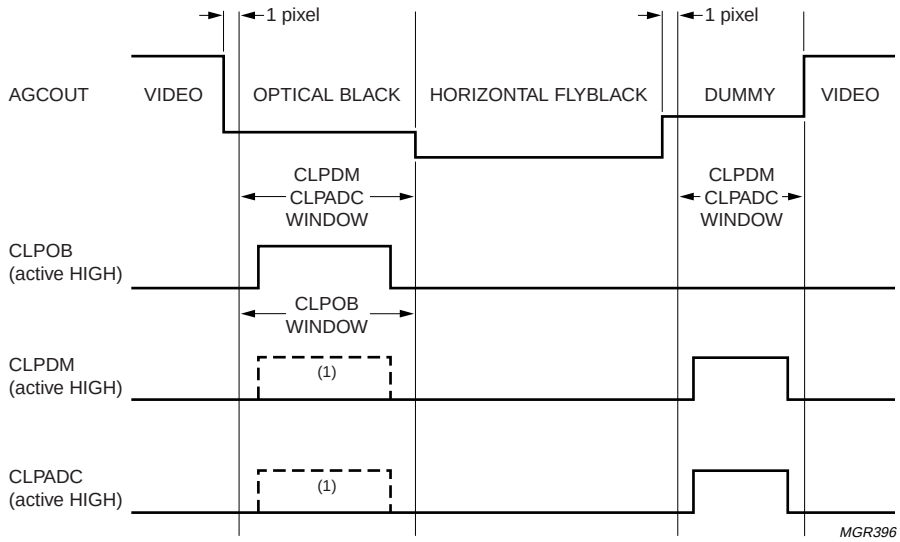


Fig.5 Pixel frequency timing diagram.



(1) When dummy pixels are not available.

Fig.6 Line frequency timing diagram.

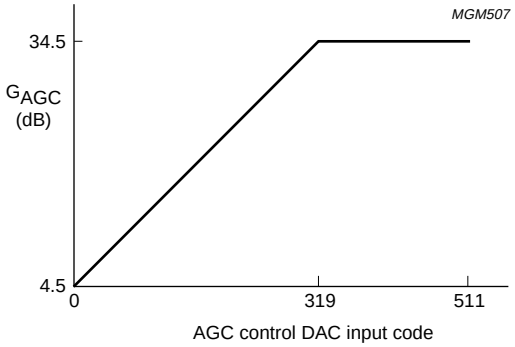


Fig.7 AGC gain as a function of DAC input code.

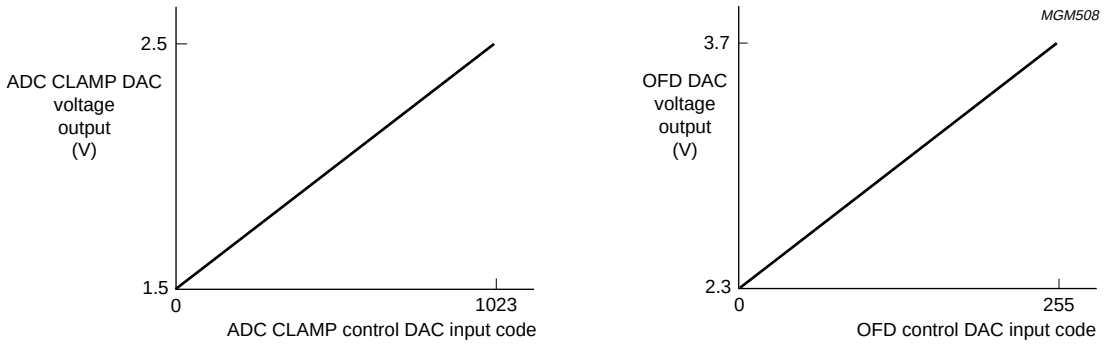


Fig.8 DAC voltage output as a function of DAC input code.

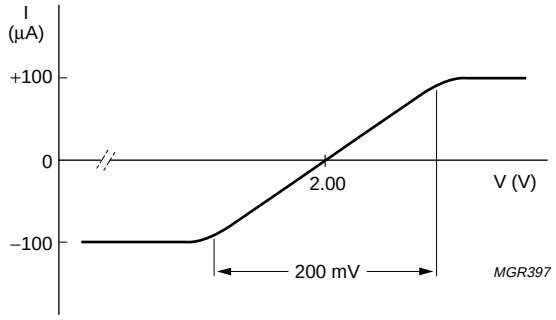


Fig.9 Typical clamp current for pin CPCDS.

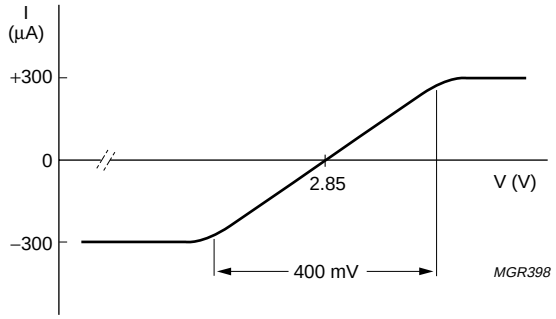


Fig.10 Typical clamp current for pins IND and INP.

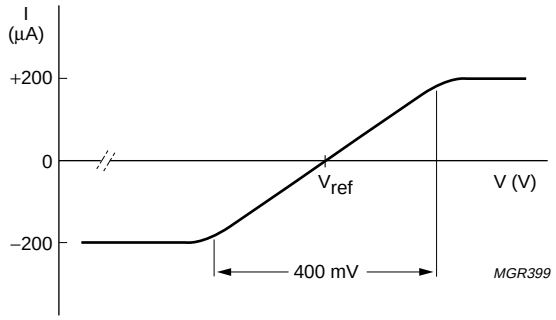
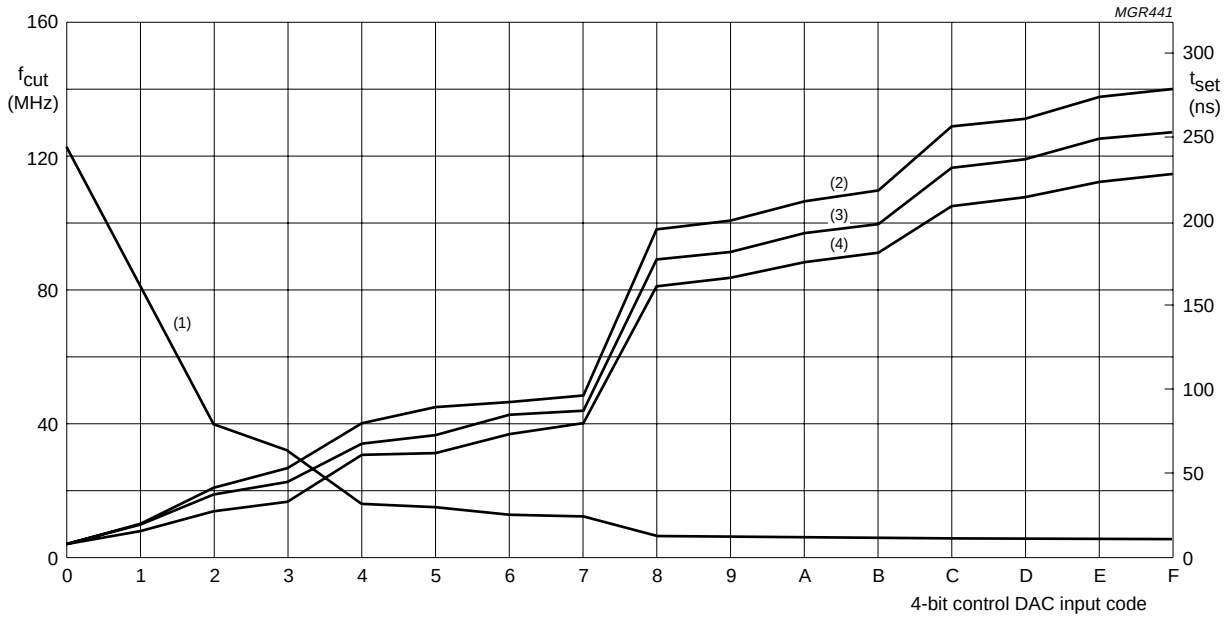


Fig.11 Typical clamp current for pin V_{ref}.



(1) f_{cut}.
(2) t_{set} (10 bits accuracy).
(3) t_{set} (9 bits accuracy).
(4) t_{set} (8 bits accuracy).

Fig.12 CDS settling time and bandwidth.

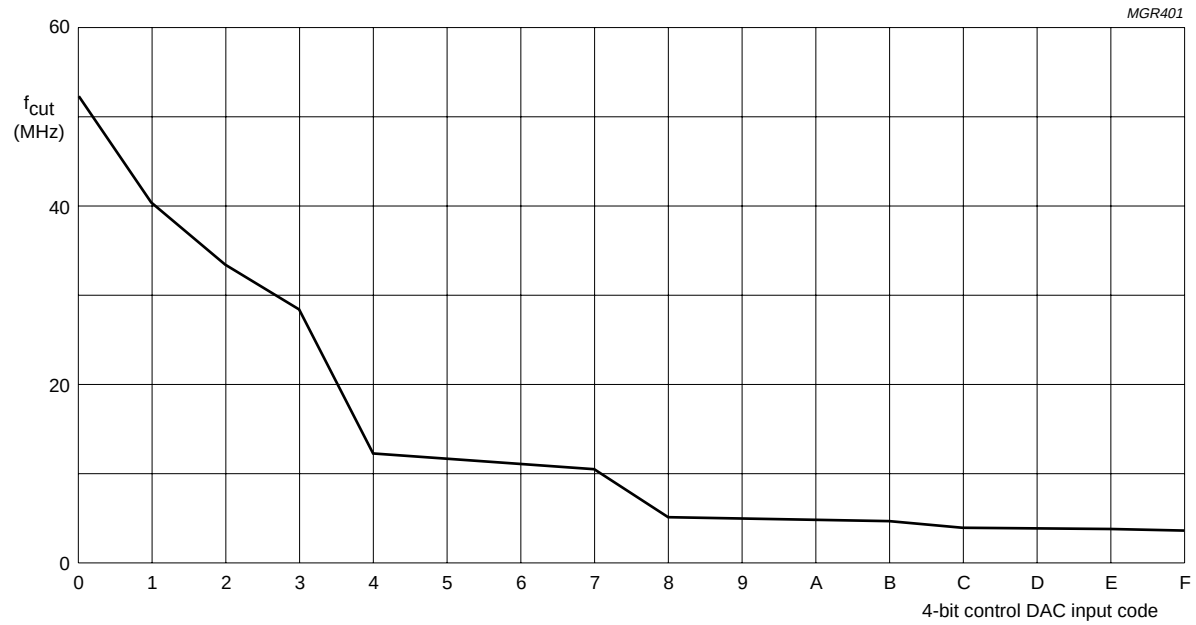
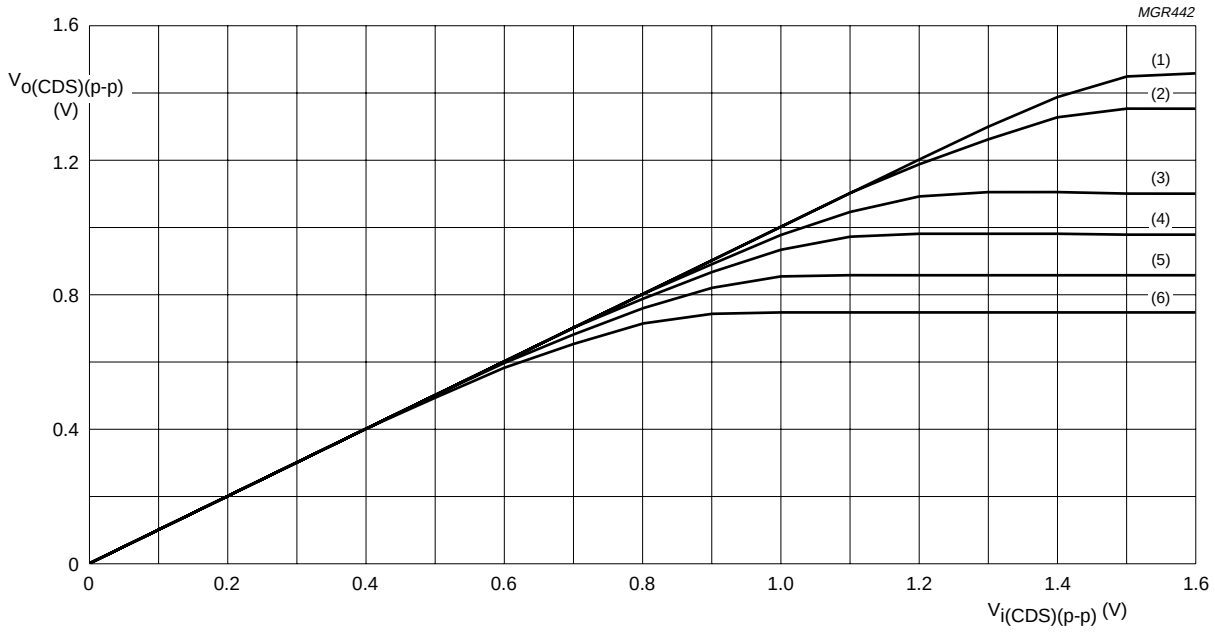
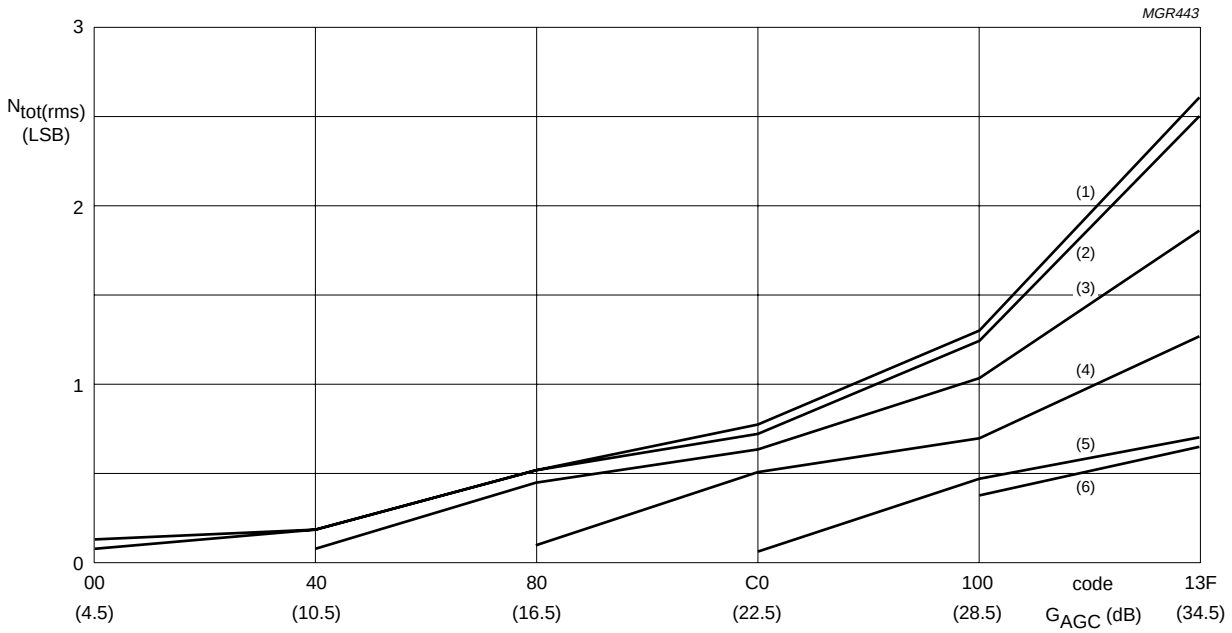


Fig.13 AGC bandwidth.



(1) $t_{set(CDS)}$ = 12 ns (3) $t_{set(CDS)}$ = 8 ns (5) $t_{set(CDS)}$ = 6 ns
(2) $t_{set(CDS)}$ = 10 ns (4) $t_{set(CDS)}$ = 7 ns (6) $t_{set(CDS)}$ = 5 ns

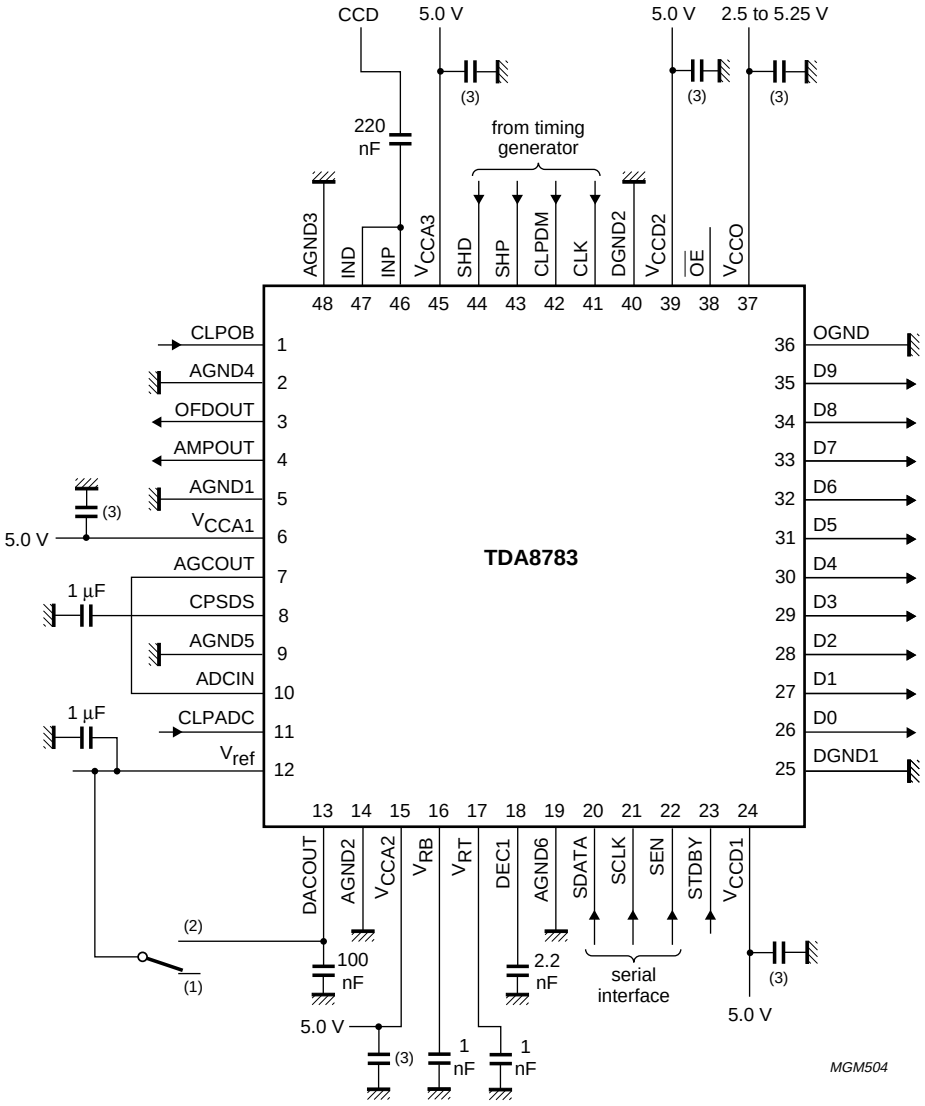
Fig.14 CDS output.



(1) f_{pix} = 27 MHz; control DAC = 00H; $f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 54 MHz.
(2) f_{pix} = 18 MHz; control DAC = 10H; $f_{cut(CDS)}$ = 120 MHz; $f_{cut(AGC)}$ = 40 MHz.
(3) f_{pix} = 10 MHz; control DAC = 31H; $f_{cut(CDS)}$ = 80 MHz; $f_{cut(AGC)}$ = 30 MHz.
(4) f_{pix} = 5 MHz; control DAC = 43H; $f_{cut(CDS)}$ = 35 MHz; $f_{cut(AGC)}$ = 12 MHz.
(5) f_{pix} = 1 MHz; control DAC = F8H; $f_{cut(CDS)}$ = 6 MHz; $f_{cut(AGC)}$ = 4 MHz.
(6) f_{pix} = 375 kHz; control DAC = FFH; $f_{cut(CDS)}$ = 4 MHz; $f_{cut(AGC)}$ = 4 MHz.

Fig.15 Output noise (RMS value).

APPLICATION INFORMATION



Depending on the application, the following connections must be made:

(1) The clamp level of the signal input at ADCIN can be tuned from code 00 to code 511 in 0.5 LSB steps of ADC via the serial interface (clamp ADC activated).

(2) Clamp ADC not activated, direct connection from DACOUT to V_{ref}.

(3) All supply pins must be decoupled with 100 nF capacitors as close as possible to the device.

Fig.16 Application diagram.

Power and grounding recommendations

Care must be taken to minimize noise when designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.

The connections between CCD interface and CDS input should be as short as possible and a ground ring protection around these connections can be beneficial.

Decoupling capacitors are necessary on all supply pins as shown in Fig.16.

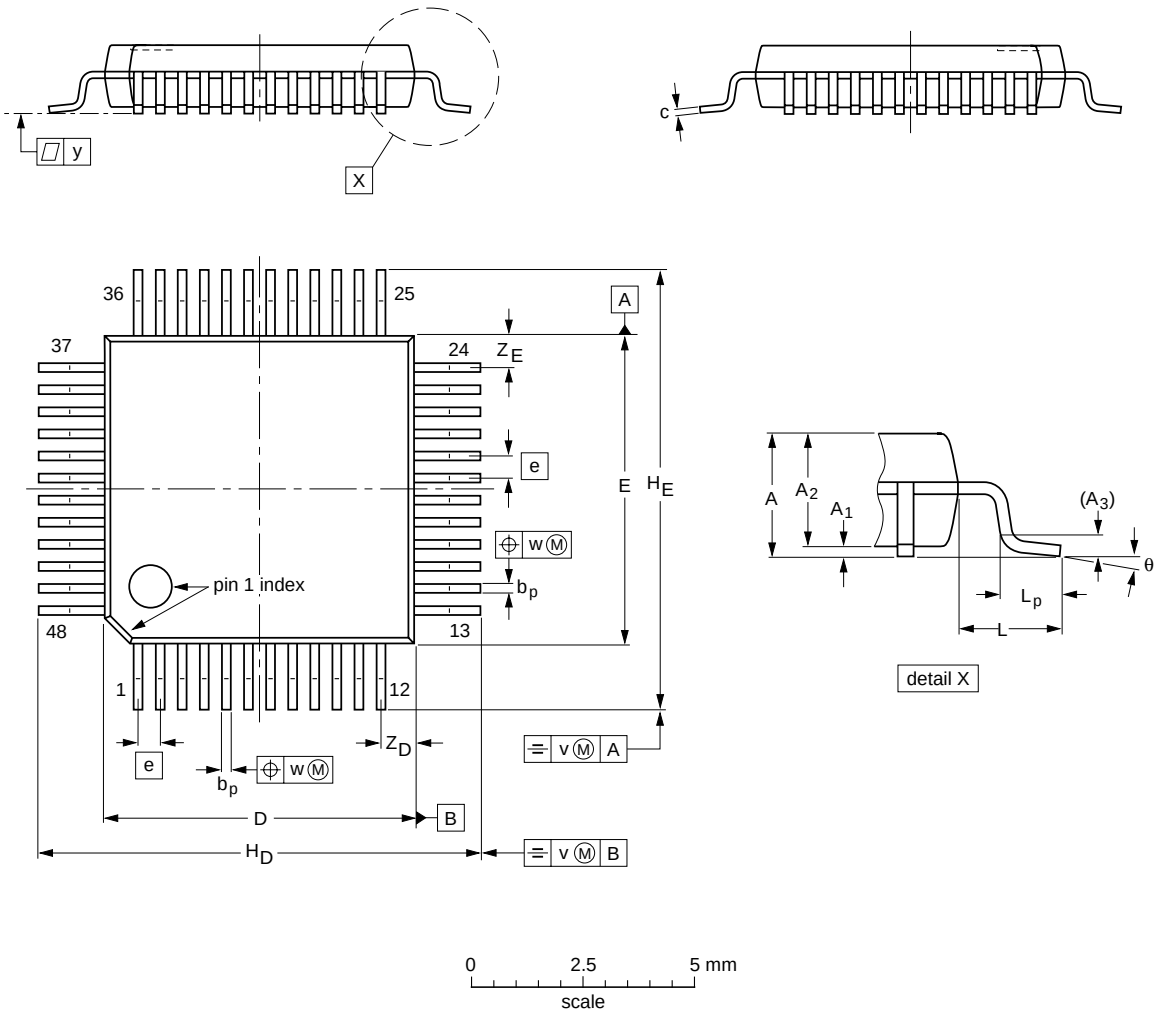
Separate analog and digital supplies provide the best performance. If it is not possible to do this on the board, then decouple the analog supply pins effectively from the digital supply pins. The decoupling capacitors must be placed as close as possible to the IC package.

In a two-ground system, in order to minimize the noise from package and die parasitics, the following recommendations must be implemented:

- The ground pin associated with the digital outputs must be connected to the digital ground plane and special care should be taken to avoid feedthrough in the analog ground plane. The analog and digital ground planes must be connected with an inductor as close as possible to the IC package, in order to have the same DC voltage on the ground planes.
- The digital output pins and their associated lines should be shielded by the digital ground plane, which can be used as return path for the digital signals.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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