Dual-Channel Digital Isolators, Enhanced System-Level ESD Reliability

Enhanced Product

ADuM3210-EP/ADuM3211-EP

FEATURES

- **Enhanced system-level ESD performance per IEC 61000-4-x**
- **High temperature operation: 125°C**
- **Narrow body, RoHS-compliant, 8-lead SOIC**
- **Low power operation**
  - **5 V operation**
    - **1.7 mA per channel maximum at 0 Mbps to 1 Mbps**
    - **4.1 mA per channel maximum at 10 Mbps**
    - **8.4 mA per channel maximum at 25 Mbps**
  - **3.3 V operation**
    - **1.5 mA per channel maximum at 0 Mbps to 1 Mbps**
    - **2.6 mA per channel maximum at 10 Mbps**
    - **5.2 mA per channel maximum at 25 Mbps**
- **Precise timing characteristics**
- **High common-mode transient immunity: >25 kV/µs**
- **Safety and regulatory approvals (pending)**
  - **UL recognition: 2500 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A**
  - **VDE certificate of conformity**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 560 V peak**

ENHANCED FEATURES

- **Supports defense and aerospace applications (AQEC standard)**
- **Military temperature range: −55°C to +125°C**
- **Controlled manufacturing baseline**
- **Enhanced product change notification**
- **Qualification data available on request**

APPLICATIONS

- **Size-critical multichannel isolation**
- **SPI interface/data converter isolation**
- **RS-232/RS-422/RS-485 transceiver isolation**
- **Digital field bus isolation**
- **Gate drive interfaces**

GENERAL DESCRIPTION

The ADuM3210-EP/ADuM3211-EP[1] are dual-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

The ADuM3210-EP/ADuM3211-EP isolators provide two independent isolation channels in two channel configurations with data rates up to 25 Mbps (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems, as well as enabling voltage translation functionality across the isolation barrier. The ADuM3210-EP/ADuM3211-EP isolators have a default output low characteristic in comparison to the ADuM3200/ADuM3201 models, which have a default output high characteristic.

In comparison to the ADuM1200-EP isolator, the ADuM3210-EP/ADuM3211-EP isolators contain various circuit and layout changes providing increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM1200-EP or ADuM3210-EP/ADuM3211-EP products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with* i*Coupler Isolation Products*.

Refer to the ADuM3210/ADuM3211 data sheet for additional application and technical information.

FUNCTIONAL BLOCK DIAGRAMS

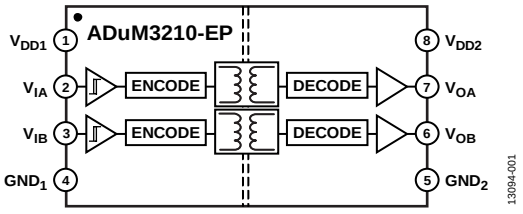

Figure 1. ADuM3210-EP Functional Block Diagram

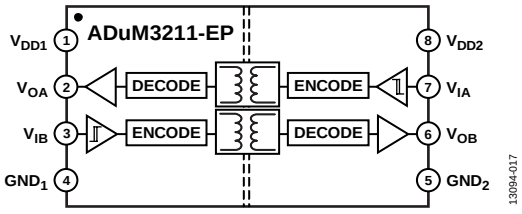

Figure 2. ADuM3211-EP Functional Block Diagram

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,239.

Rev. A Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			18	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Directional	t_{PSKOD}			18	ns	
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%

Table 2.

		1 Mbps			10 Mbps			25 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM3210-EP	I_{DD1}		1.3	1.7		3.5	4.8		7.6	9.9	mA
	I_{DD2}		1.0	1.6		2.0	2.8		3.8	5.1	mA
ADuM3211-EP	I_{DD1}		1.1	1.5		3.0	4.0		6.4	8.7	mA
	I_{DD2}		1.3	1.8		3.1	4.1		6.1	8.0	mA

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.4	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD			4	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Directional	t_{PSKOD}			20	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 5.

		1 Mbps			10 Mbps			25 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM3210-EP	I_{DD1}		0.8	1.3		2.1	3.2		4.6	6.1	mA
	I_{DD2}		0.7	1.0		1.3	1.9		2.4	3.4	mA
ADuM3211-EP	I_{DD1}		0.7	1.3		1.8	2.6		3.8	5.4	mA
	I_{DD2}		0.8	1.6		1.9	2.5		3.7	5.0	mA

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Directional	t_{PSKOD}			20	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 8.

		1 Mbps			10 Mbps			25 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM3210-EP	I_{DD1}		1.3	1.7		3.5	4.8		7.6	9.9	mA
	I_{DD2}		0.7	1.0		1.3	1.9		2.4	3.4	mA
ADuM3211-EP	I_{DD1}		1.1	1.5		2.9	4.0		6.4	8.7	mA
	I_{DD2}		0.8	1.6		1.9	2.5		3.7	5.0	mA

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			4	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			22	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Directional	t_{PSKOD}			20	ns	
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%

Table 11.

		1 Mbps			10 Mbps			25 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM3210-EP	I_{DD1}		0.8	1.3		2.1	3.2		4.6	6.1	mA
	I_{DD2}		1.0	1.6		2.0	2.8		3.7	5.1	mA
ADuM3211-EP	I_{DD1}		0.7	1.3		1.8	2.6		3.8	5.4	mA
	I_{DD2}		1.3	1.8		3.1	4.1		6.1	8.0	mA

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3210-EP/ADuM3211-EP are pending approval by the organizations listed in Table 14.

Table 14.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single/basic 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3210-EP/ADuM3211-EP is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM3210-EP/ADuM3211-EP is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air, in the plane of the PCB
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Distance (Internal Clearance)		0.017 min	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

INSULATION CHARACTERISTICS (DIN V VDE V 0884-10 (VDE V 0884-10):2006-12)

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for a 560 V peak working voltage.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.56	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

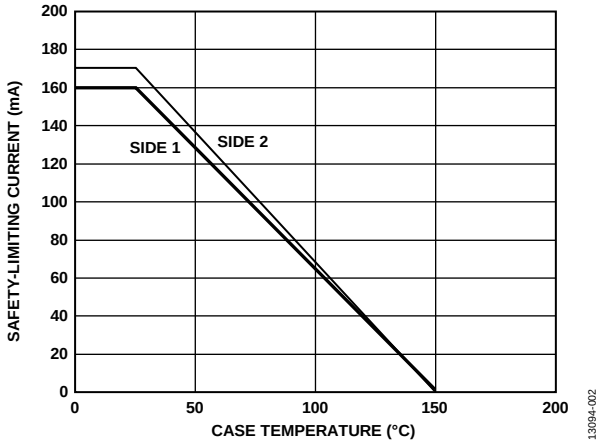

Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Rating
Operating Temperature	T_A	−55°C to +125°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3 V to 5.5 V
Maximum Input Signal Rise and Fall Times		1 ms
Start-Up Current	I_{DD1}, I_{DD2}	20 mA

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 18.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−55°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin (I_O)[3]	−22 mA to +22 mA
Common-Mode Transients (CM_H, CM_L)[4]	−100 kV/µs to +100 kV/µs

[1] Each voltage is relative to its respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 3 for maximum allowable current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 19. Maximum Continuous Working Voltage

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

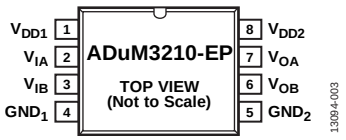

Figure 4. ADuM3210-EP Pin Configuration

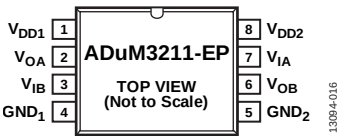

Figure 5. ADuM3211-EP Pin Configuration

Table 20. ADuM3210-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.

Table 21. ADuM3211-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.

TRUTH TABLES

Table 22. ADuM3210-EP Truth Table (Positive Logic)

V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DD2} State	V_{OA} Output[1]	V_{OB} Output[1]	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 µs of V_{DDI} power restoration
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration

[1] H is logic high, L is logic low, and X is don't care.

Table 23. ADuM3211-EP Truth Table (Positive Logic)

V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DD2} State	V_{OA} Output[1]	V_{OB} Output[1]	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1 µs of V_{DDI} power restoration
X	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration

[1] H is logic high, L is logic low, and X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

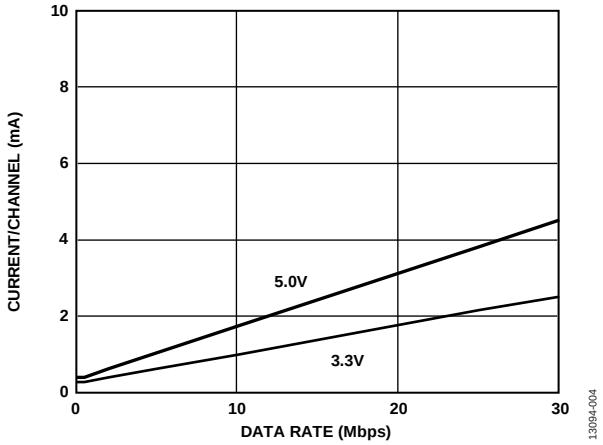

Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5.0 V and 3.3 V Operation

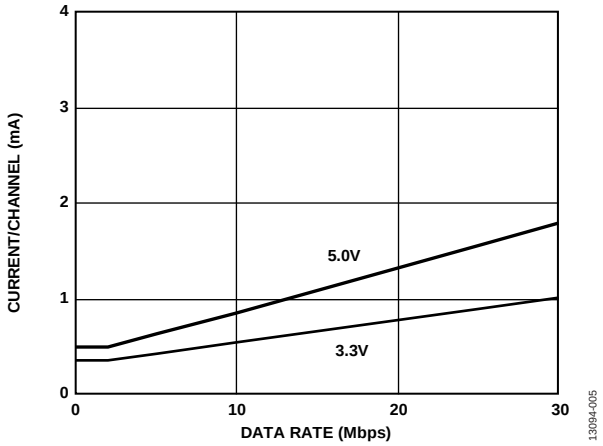

Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5.0 V and 3.3 V Operation (No Output Load)

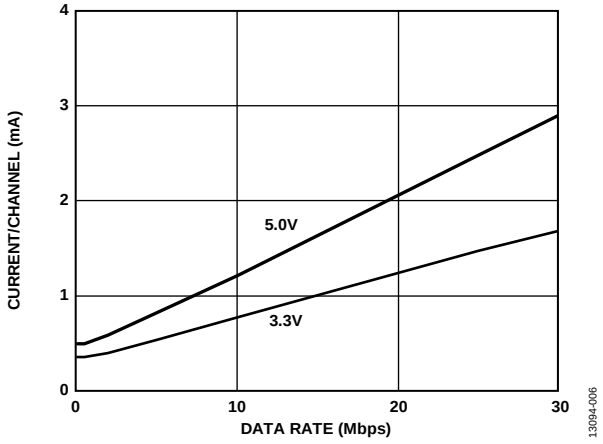

Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5.0 V and 3.3 V Operation (15 pF Output Load)

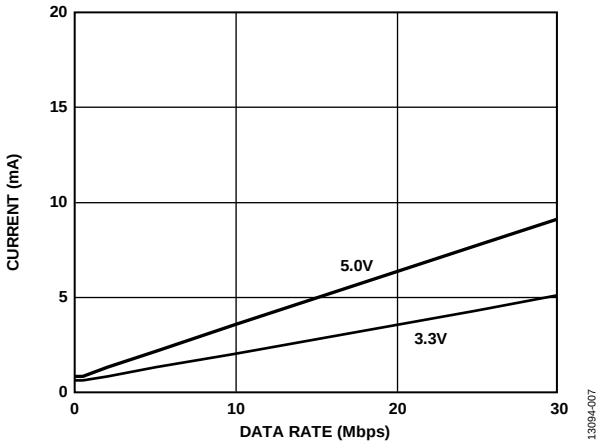

Figure 9. ADuM3210-EP Typical I_{DD1} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

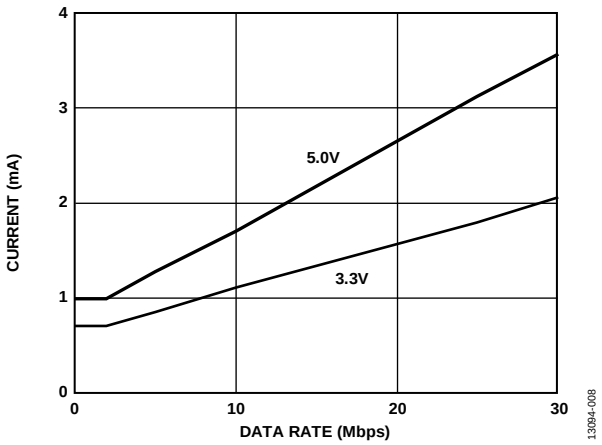

Figure 10. ADuM3210-EP Typical I_{DD2} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

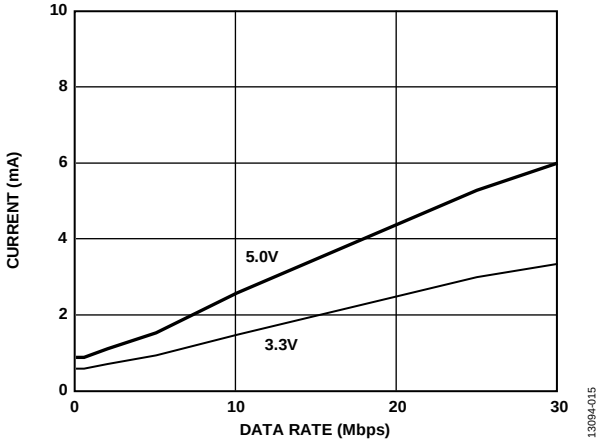

Figure 11. ADuM3211-EP Typical I_{DD1} or I_{DD2} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

OUTLINE DIMENSIONS

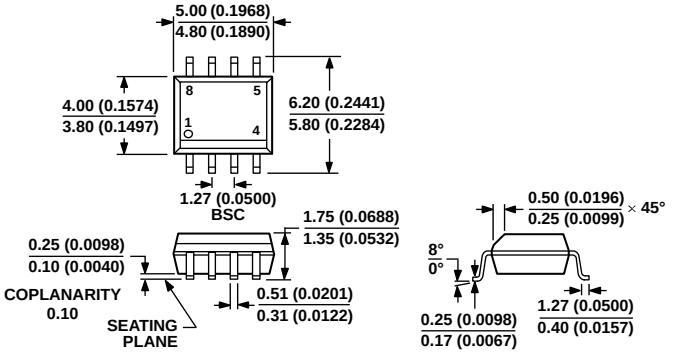

Figure 12. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option[2]
ADuM3210TRZ-EP	2	0	25	50	3	−55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3210TRZ-EP-RL7	2	0	25	50	3	−55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3211TRZ-EP	1	1	25	50	4	−55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3211TRZ-EP-RL7	1	1	25	50	4	−55°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.
[2] R-8 means 8-lead, narrow body SOIC_N.

D13094-0-10/15(A)