PIC18F2585/2680/4585/4680 Rev. A3 Silicon Errata

The PIC18F2585/2680/4585/4680 Rev. A3 parts you have received conform functionally to the Device Data Sheet (DS39625**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2585/2680/4585/4680 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F2585/2680/4585/4680 silicon.

The following silicon errata apply only to PIC18F2585/2680/4585/4680 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2585	0001 1010 100	0 0100
PIC18F2680	0001 1010 110	0 0100
PIC18F4585	0001 1010 101	0 0100
PIC18F4680	0001 1010 111	0 0100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>) or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the test or operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

EXAMPLE 1:

```
MOVF    ECCP1AS, W
BTFSC   WREG, ECCPASE
BRA     SHUTDOWN_ROUTINE
```

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: ECCP

When a shutdown condition occurs, the output port is made inactive for the duration of the event. After the event that caused the shutdown ends, the ECCP module immediately enables the PWM output and does not wait until the beginning of the next PWM cycle.

Work around

Disable the auto-restart feature in software, polling the Timer2 Interrupt Flag (TMR2IF) and do not clear the ECCPASE bit until TMR2IF is set.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not consistently synchronize the pulse to the beginning of the period, and the end of the pulse can occur at any time within the period.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: ECCP

The auto-shutdown event will cause the ECCP pins (P1A, P1B, P1C, P1D) to draw higher current than expected. This occurs when the ECCPAS1 or ECCPAS0 bits are set and an auto-shutdown event occurs.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: ECCP

The auto-shutdown source, FLT0, has inverse polarity from the description in **Section 16.4.7 "Enhanced PWM Auto-Shutdown"** of the Device Data Sheet. A logic high-voltage level on FLT0 will generate a shutdown on ECCP1.

Work around

Invert the logic in the program's source code.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: ECCP

If a Halt command is issued while debugging with the In-Circuit Debugger (MPLAB® ICD 2), the ECCP module may freeze completely. However, if a shutdown is enabled and triggered by the FLT0 pin, the ECCPASE bit is set and the outputs are driven to their shutdown state, as defined by the PSSAC1:PSSAC0 and PSSBD1:PSSBD0 bits, regardless of the debugging process being stopped.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: ECCP

In 10-Bit Addressing mode, when a Repeated Start is issued followed by the high address byte and a Write command, an ACK is not issued.

Work around

There are two work arounds available:

1. Single-Master Environment:
   In a single-master environment, the user must issue a Stop, then a Start, followed by a write to the address high, then the address low followed by the data.
2. Multi-Master Environment:
   In a multi-master environment, the user must issue a Repeated Start, send a dummy Write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will prevent loss of the bus.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F458, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter, after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4680 family as the PIC18F458 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F458, to achieve the same Reset period on the PIC18F4680 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 (depending on the T1CKPS1:T1CKPS0 bit values).

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: ECCP and CCP

When ECCP1 and CCP2 are configured for PWM mode with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, this may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

Work around

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The ECCP and CCP modules remain capable of 10-bit accuracy.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for an external clock source and the CCP1CON or ECCP1CON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

Work around

Modify firmware to reset the Timer registers upon detection of the compare match condition – TMRxL and TMRxH.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: Timer1/Timer3

When the Timer1/Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 TCY, interrupts may occasionally be skipped.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written. It does not change the actual prescale value.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected. The timer registers can also be written as expected.

Work around

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the $\overline{\text{T1SYNC}}$ bit (T1CON<2>).

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: MSSP

When the MSSP is configured for SPI Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

In Slave mode with Slave Select enabled, SSPM3:SSPM0 = 0010 (SSPCON<3:0>), the SDO pin can be disabled by placing a logic high level on the $\overline{\text{SS}}$ pin (RA5).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: MSSP

After an I²C™ transfer is initiated, the SSPBUF register may be written for up to 10 TCY before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set anytime an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: MSSP

In its current implementation, the I²C™ Master mode operates as follows:

1. The Baud Rate Generator for I²C in Master mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

   For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 17-3 of the Device Data Sheet. The differences are shown in **bold** text.

2. Use the following formula in place of the one shown in Register 17-4 (SSPCON1) of the Device Data Sheet for bit description, SSPM3:SSPM0 = 1000.

   SSPADD = INT((FCY/FSCL) – (FCY/1.111 MHz)) – 1

TABLE 1: I²C™ CLOCK RATE w/BRG

FOSC	FCY	FCY*2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I²C™ interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

17. Module: MSSP

RCEN becomes set when the system is idle. In normal operation, the setting of RCEN should be ignored by the module while the system is not idle.

Work around

Wait for the system to become idle. This requires a check for the following bits to be reset:

ACKEN, RCEN, PEN, RSEN and SEN.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: MSSP

In an I²C system with multiple slave nodes, an unaddressed slave may respond to bus activity when data on the bus matches its address. The first occurrence will set the BF bit. The second occurrence will set the BF and the SSPOV bits. In both situations, the SSPIF bit is not set and an interrupt will not occur. The device will vector to the Interrupt Service Routine only if the interrupt is enabled and an address match occurs.

Work around

The I²C slave must clear the SSPOV bit after each I²C event to maintain normal operation.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: MSSP

It has been observed that following a Power-on Reset, I^2C mode may not initialize properly by just configuring the SCL and SDA pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCL and SDA pins as outputs by clearing their corresponding TRIS bits.
2. Force SCL and SDA low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCL and SDA as inputs by setting their TRIS bits.

Once this is done, use the SSPCON1 and SSPCON2 registers to configure the proper I^2C mode as before.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: MSSP

When the MSSP is configured for SPI mode, the Buffer Full Status bit, BF (SSPSTAT<0>), should not be polled in software to determine when the transfer is complete.

Work around

Copy the SSPSTAT register into a variable and perform the bit test on the variable. In Example 2, SSPSTAT is copied into the working register where the bit test is performed.

EXAMPLE 2:

```
loop_MSB:
    MOVF    SSPSTAT, W
    BTFSS   WREG, BF
    BRA     loop_MSB
```

A second option is to poll the Master Synchronous Serial Port Interrupt Flag bit, SSPIF (PIR1<3>). This bit can be polled and will set when the transfer is complete.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: DC Characteristics (BOR)

The values for parameter D005 (V_{BOR}) in **Section 27.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet, when the trip point for BORV1:BORV0 = 11, are not applicable as the device may reset below the minimum operating voltage for the device.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: BOD/HLVD

Due to production tolerances, selecting the lowest setting for Brown-out Detect (BORV1:BORV0 = 11) or Low-Voltage Reset (LVV = 0000) is not recommended, since it may result in an actual Brown-out Reset or Low-Voltage Detect below the minimum allowable V_{DD} of 2.0V.

Work around

Use the next highest BOD or HLVD voltage threshold to ensure a low V_{DD} is detected before it drops below 2.0V.

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register. Upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction "`MOVFF TEMP, WREG`", the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming:
   a) If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 8-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead.

      For example, use:

      ```
      MOVF   TEMP, W
      MOVWF  BSR
      ```

      instead of `MOVFF TEMP, BSR`.

   b) As another alternative, the following work around shown in Example 3 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

EXAMPLE 3:

```
ISR @ 0x0008
   CALL     Foo, FAST      ; store current value of WREG, BSR, STATUS for a second time
Foo:
   POP                     ; clears return address of Foo call
   :                       ; insert high priority ISR code here
   :
   RETFIE   FAST
```

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as "low priority" by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The code segment, shown in Example 4 on the following page, demonstrates the work around using the C18 compiler.

EXAMPLE 4:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

An optimized C18 version is also provided in Example 5. This example illustrates how it reduces the instruction cycle count from 10 cycles to 3.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 5:

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
  _asm
    CALL high_vector_branch, 1
  _endasm
}

void high_vector_branch (void)
{
  _asm
    POP
    GOTO high_isr
  _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
  ...
}
```

25. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

26. Module: EUSART

The EUSART auto-baud feature may periodically measure the incoming baud rate incorrectly. The rate of incorrect baud rate measurements will depend on the frequency of the incoming synchronization byte and the system clock frequency.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

27. Module: EUSART

With the auto-wake-up option enabled by setting the WUE (BAUDCON<1>) bit, the RCIF (PIR1<5>) bit will become set on a high-to-low transition on the RX pin. However, the WUE bit may not clear within 1 TCY of a low-to-high transition on RX. While the WUE bit is set, reading the receive buffer, RCREG, will not clear the RCIF interrupt flag. Therefore, the first opportunity to automatically clear RCIF by reading RCREG may take longer than expected.

Note:	RCIF can only be cleared by reading RCREG.

Work around

There are two work arounds available:

1. After the wake-up event has occurred, clear the WUE bit in software before reading the receive buffer RCREG.
2. Poll the WUE bit and read RCREG after the WUE bit is automatically cleared.

Date Codes that pertain to this issue:

All engineering and production devices.

28. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted, only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer TXREG are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to,
- the baud rate counter overflows (at the end of the bit period), and
- a Stop bit is being transmitted (shifted out of TSR).

Work around

If possible, do not use the module's double buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREG immediately after TXIF is set or wait 1-bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted. Note that TXIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREG.
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of the Stop bit, then start the timer when you load the TXREG. Do not load the TXREG when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

29. Module: Reset

This version of silicon does not support the functionality described in Note 1 of parameter D002 in **Section 27.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet. The RAM content may be altered during a Reset event if the following conditions are met.

- Device is accessing RAM.
- Asynchronous Reset (i.e., WDT, BOR or $\overline{\text{MCLR}}$ occurs when a write operation is being executed (start of a Q4 cycle).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

30. Module: ECAN™ Technology

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the Transmit Buffer ID register, TXBnSIDH. The following conditions must exist for the corruption to occur:

1. A transmit message must be pending.
2. The ECAN module must detect a Start-Of-Frame (SOF) in the third bit of interframe space.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

31. Module: ECAN™ Technology

Following an error on the bus, the ECAN module is unable to switch from Listen Only mode directly to Configuration mode.

Work around

Use the REQOP (CANCON<7:5>) bits to select Normal mode as an intermediate step when switching from Listen Only mode to Configuration mode.

Date Codes that pertain to this issue:

All engineering and production devices.

32. Module: ECAN™ Technology

Under specific conditions, the TXBxSIDH register of the pending message for transmission may be corrupted. The following conditions must exist for this event to occur:

1. A transmit message must be pending.
2. All of the receive buffers must be full and a received message is in the Message Assembly Buffer (MAB).
3. A receiver buffer must be made available (RXBxCON<RXFUL> set to '0') when a Start-of-Frame (SOF) is recognized on the CAN bus, or on the instruction cycle prior to the SOF for the TXBxSIDH corruption event to occur. The timing of this event is crucial.

Work around

Ensure that a receive buffer overflow condition does not occur and/or ensure that a transmit request is not pending if a receive buffer overflow condition does exist.

The pseudo-code segment in Example 6 is an example of how to disable a pending transmission. This code is for illustration purposes only.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 6:

```
If (RXBnOVFL == 1)     // Has an overflow occurred?
       {   If (TXREQ == 1)// Is a transmission pending?
           {   TXREQ = 0; // Clear transmit request
               If (TXABT == 1)// Store transmission aborted status value
                   MyFlag = 1;
           }
       }
       Temp_RXREG = RXBx; // Read receive buffer
       If (MyFlag)        // Was previous transmission aborted?
       {   TXREQ = 1;     // Set transmit request
           MyFlag = 0;    // Reset stored transmission aborted status
       }
```

33. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (7/2006)

First revision of this document which includes silicon issues 1-9 (ECCP), 9 (ECCP and CCP), 10-12 (Timer1/ Timer3), 13 (Timer1), 14-20 (MSSP), 21 (A/D), 22 (DC Characteristics – BOR), 23 (BOD/HLVD), 24 (Interrupts), 25-28 (EUSART), 29 (Reset), and 30-32 (ECAN).

Rev B Document (12/2006)

Updated silicon issues 21 (MSSP) and 32-33 (ECAN™ Technology).

Rev C Document (2/2007)
Correct issue 31 ECAN™ Technology. Corrected code comment in Example 6 for silicon issue 33 (ECAN™ Technology).

Rev D Document (5/2007)
Added silicon issue 34 (10-Bit Analog-to-Digital Converter).

Rev E Document (10/2007)
Removed silicon issue 22 (A/D).

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