ADC0808S125/250

Single 8-bit ADC, up to 125 MHz or 250 MHz

Rev. 04 — 2 July 2012 Product data sheet

1. General description

The ADC0808S is a differential, high-speed, 8-bit Analog-to-Digital Converter (ADC) optimized for telecommunication transmission control systems and tape drive applications. It allows signal sampling frequencies up to 250 MHz.

The ADC0808S clock inputs are selectable between 1.8 V Complementary Metal Oxide Semiconductor (CMOS) or Low-Voltage Differential Signals (LVDS). The data output signal levels are 1.8 V CMOS.

All static digital inputs (CLKSEL, CCSSEL, CE_N, OTC, DEL0 and DEL1) are 1.8 V CMOS compatible.

The ADC0808S offers the most flexible acquisition control system possible due to its programmable Complete Conversion Signal (CCS) which allows the delay time of the acquisition clock and acquisition clock frequency to be adjusted.

The ADC0808S is supplied in an HTQFP48 package.

2. Features

- 8-bit resolution
- High-speed sampling rate up to 250 MHz
- Maximum analog input frequency up to 560 MHz
- Programmable acquisition output clock (complete conversion signal)
- Differential analog input
- Integrated voltage regulator or external control for analog input full-scale
- Integrated voltage regulator for input common-mode reference
- Selectable 1.8 V CMOS or LVDS clock input
- 1.8 V CMOS digital outputs
- 1.8 V CMOS compatible static digital inputs
- Binary or 2’s complement CMOS outputs
- Only 2 clock cycles latency
- Industrial temperature range from –40 °C to +85 °C
- HTQFP48 package

3. Applications

- 2.5G and 3G cellular base infrastructure radio transceivers
- Wireless access systems
- Fixed telecommunications

- Optical networking
- Wireless Local Area Network (WLAN) infrastructure
- Tape drive applications

4. Ordering information

Table 1. Ordering information

Type number	Sampling frequency (MHz)	Package		
		Name	**Description**	**Version**
ADC0808S125HW-C1	125	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-2
ADC0808S250HW-C1	250			

5. Block diagram

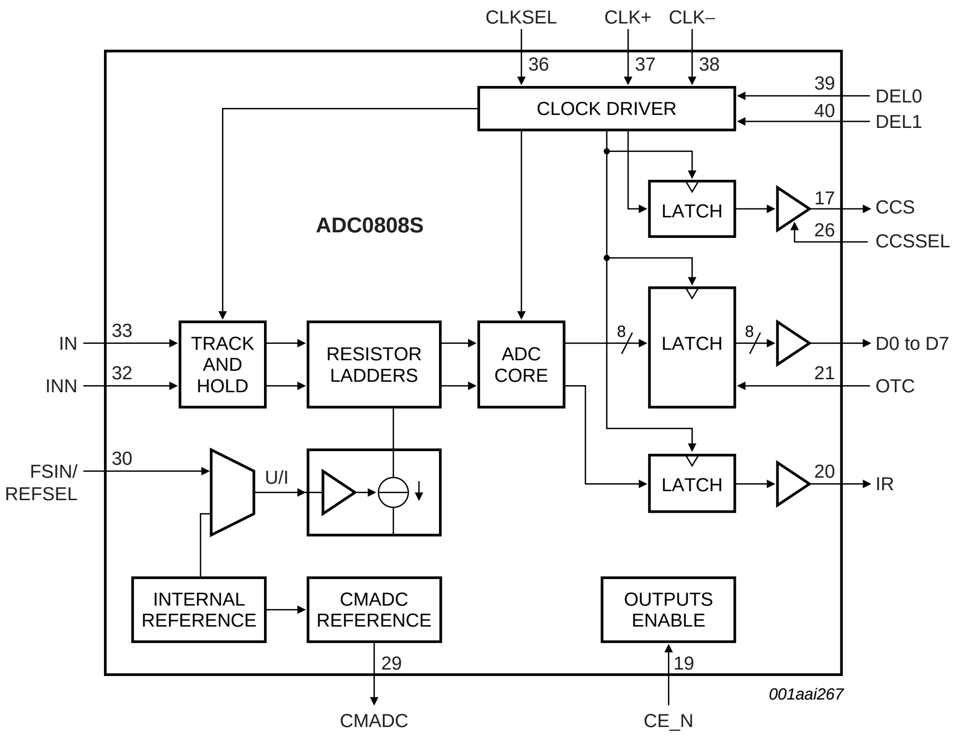


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

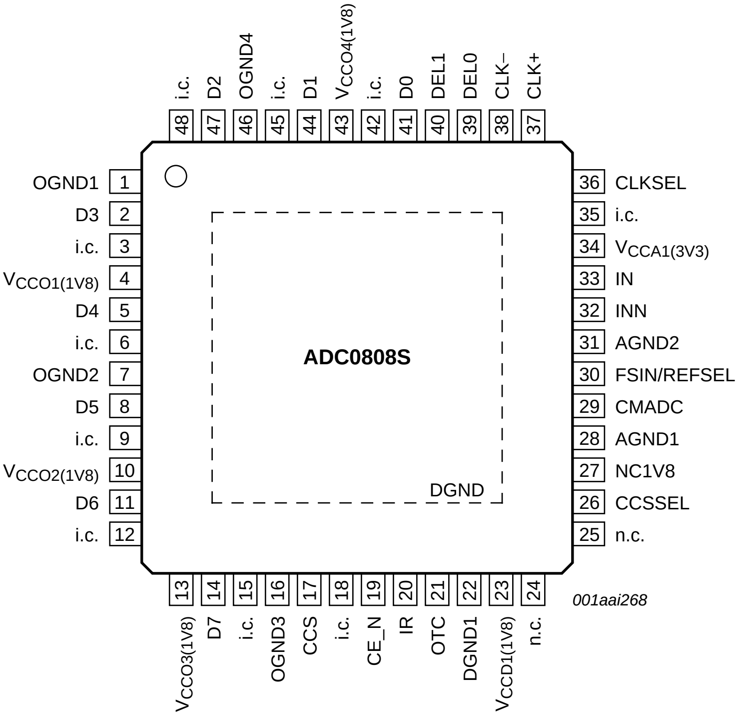


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
OGND1	1	G	data output ground 1
D3	2	O	data output bit 3
i.c.	3	-	internally connected; leave open
$V_{CCO1(1V8)}$	4	P	data output supply voltage 1 (1.8 V)
D4	5	O	data output bit 4
i.c.	6	-	internally connected; leave open
OGND2	7	G	data output ground 2
D5	8	O	data output bit 5
i.c.	9	-	internally connected; leave open
$V_{CCO2(1V8)}$	10	P	data output supply voltage 2 (1.8 V)
D6	11	O	data output bit 6
i.c.	12	-	internally connected; leave open
$V_{CCO3(1V8)}$	13	P	data output supply voltage 3 (1.8 V)
D7	14	O	data output bit 7

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
i.c.	15	-	internally connected; leave open
OGND3	16	G	data output ground 3
CCS	17	O	complete conversion signal output
i.c.	18	-	internally connected; leave open
CE_N	19	I(CMOS)	chip enable input (active LOW)
IR	20	O(CMOS)	in-range output
OTC	21	I(CMOS)	control input for 2’s complement output
DGND1	22	G	digital ground 1
$V_{CCD1(1V8)}$	23	P	digital supply voltage 1 (1.8 V)
n.c.	24	-	not connected
n.c.	25	-	not connected
CCSSEL	26	I(CMOS)	control input for CCS frequency selection
NC1V8	27	I	not connected or connected to $V_{CCD1(1V8)}$
AGND1	28	G	analog ground 1
CMADC	29	O	regulator common-mode ADC output
FSIN/REFSEL	30	I	full-scale reference voltage input/internal or external reference selection
AGND2	31	G	analog ground 2
INN	32	I	complementary analog input
IN	33	I	analog input
$V_{CCA1(3V3)}$	34	P	analog supply voltage 1 (3.3 V)
i.c.	35	-	internally connected; leave open
CLKSEL	36	I(CMOS)	control input for clock input selection
CLK+	37	I	clock input
CLK–	38	I	complementary clock input
DEL0	39	I(CMOS)	complete conversion signal delay input 0
DEL1	40	I(CMOS)	complete conversion signal delay input 1
D0	41	O	data output bit 0
i.c.	42	-	internally connected; leave open
$V_{CCO4(1V8)}$	43	P	data output supply voltage 4 (1.8 V)
D1	44	O	data output bit 1
i.c.	45	-	internally connected; leave open
OGND4	46	G	data output ground 4
D2	47	O	data output bit 2
i.c.	48	-	internally connected; leave open
DGND	-	G	digital ground; exposed die pad

[1] See Table 3.

Table 3. Pin type description

Type	Description
I	input
O	output
I(CMOS)	1.8 V CMOS level input
O(CMOS)	1.8 V CMOS level output
P	power supply
G	ground

7. Functional description

7.1 CMOS/LVDS clock input

The circuit has two clock inputs CLK+ and CLK–, with two modes of operation:

- LVDS mode: CLK+ and CLK– inputs are at differential LVDS levels. An external resistor of between 80 Ω and 120 Ω is required; see Figure 3.

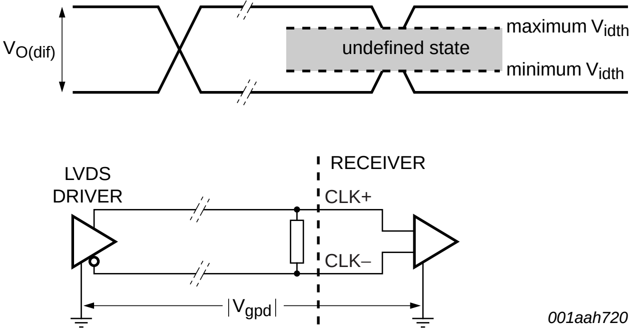


Fig 3. LVDS clock input

- 1.8 V CMOS mode: CLK+ input is at 1.8 V CMOS level and sampling is done on the rising edge of the clock input signal. In this case pin CLK– must be grounded; see Figure 4.

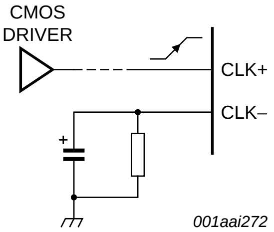


Fig 4. CMOS clock input

Table 4. Clock input format selection

Pin CLKSEL	Clock input signal
	Pins CLK+ and CLK−
HIGH or not connected	LVDS
LOW	1.8 V CMOS

7.2 Digital output coding

The digital outputs are 1.8 V CMOS compatible.

The data output format can be either binary or 2’s complement.

Table 5. Output coding with differential inputs

$V_{i(p-p)}$ = 2.0 V; $V_{ref(fs)}$ = 1.25 V; typical values to AGND.

Code	Inputs (V)		Output	Outputs D7 to D0	
	$V_{i(IN)}$	$V_{i(INN)}$	Pin IR	Binary	2’s complement
Underflow	< 0.45	> 1.45	LOW	0000 0000	1000 0000
0	0.45	1.45	HIGH	0000 0000	1000 0000
1	-	-	HIGH	0000 0001	1000 0001
:	:	:	:	:	:
127	0.95	0.95	HIGH	0111 1111	1111 1111
:	:	:	:	:	:
254	-	-	HIGH	1111 1110	0111 1110
255	1.45	0.45	HIGH	1111 1111	0111 1111
Overflow	> 1.45	< 0.45	LOW	1111 1111	0111 1111

The in-range CMOS output pin IR will be HIGH during normal operation. When the ADC input reaches either positive or negative full-scale, the IR output will be LOW.

Selection between output coding is controlled by pins OTC and CE_N.

Table 6. Output format selection

2’s complement outputs	Chip enable	Output data
Pin OTC	Pin CE_N	Pins D0 to D7, CCS and IR
LOW	LOW	active; binary
HIGH	LOW	active; 2’s complement
X[1]	HIGH	high-impedance

[1] X = don’t care.

7.3 Timing output

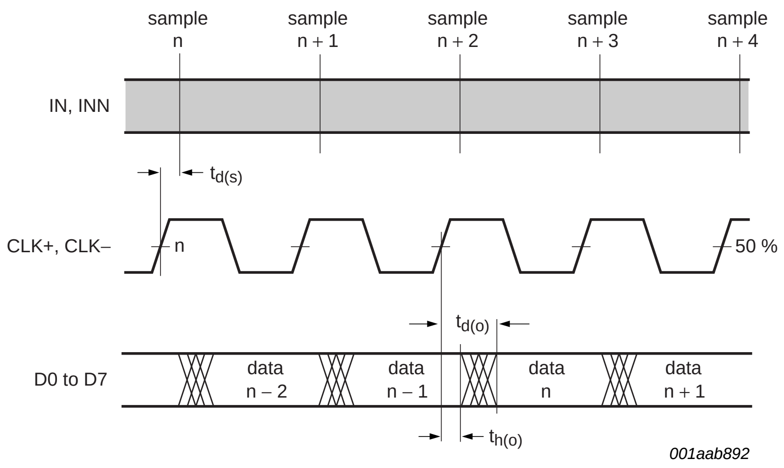


Fig 5. Output timing diagram (CCS not selected)

7.4 Timing complete conversion signal

The ADC0808S generates an adjustable clock output signal on pin CCS called Complete Conversion Signal, which can be used to control the acquisition of converted output data to the digital circuit connected to the ADC0808S output data bus.

Two logic input pins DEL0 and DEL1 control the delay of the edge of the CCS signal to achieve an optimal position in the stable, usable zone of the data as shown in Figure 6.

Table 7. Complete conversion signal selection

Pin DEL0	Pin DEL1	Pin CCS
LOW	LOW	high-impedance
HIGH	LOW	active; see Table 13
LOW	HIGH	
HIGH	HIGH	

Pin CCSSEL selects the CCS frequency; see Table 8.

Table 8. Complete conversion signal frequency selection

Pin CCSSEL	CCS frequency (f_{CCS})
HIGH or not connected	f_{clk}
LOW	f_{clk} / 2

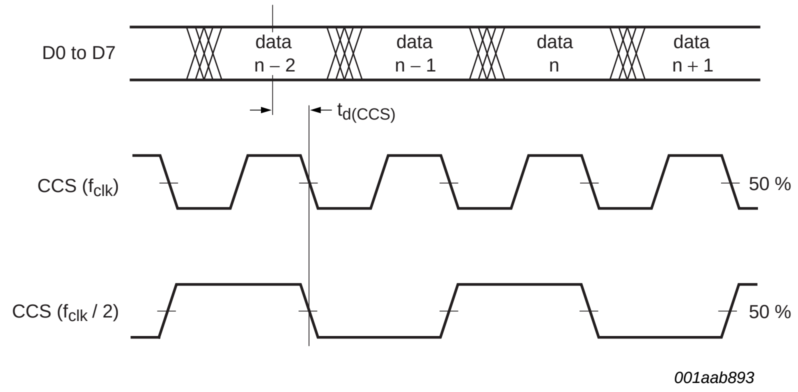


Fig 6. Complete conversion signal timing diagram using CCS

7.5 Full-scale input selection

The ADC0808S has an internal reference circuit which can be overruled by an external reference voltage. This can be done with the full-scale reference voltage ($V_{ref(fs)}$) according to Table 9.

The ADC provides the required common-mode voltage on pin CMADC. In case of internal regulation, the regulator output voltage on pin CMADC is 0.95 V.

Table 9. Full-scale input selection

Full-scale reference voltage $V_{ref(fs)}$	Common-mode output voltage $V_{O(cm)}$	Maximum peak-to-peak input voltage $V_{i(p-p)(max)}$
1.15 V	0.8 V	1.825 V
1.20 V	0.86 V	1.91 V
1.25 V	0.94 V	1.99 V
1.30 V	1.01 V	2.08 V
1.35 V	1.09 V	2.16 V

The internal reference circuit is enabled by connecting pin FSIN to ground. The common-mode output voltage $V_{O(cm)}$ on pin CMADC will then be 0.95 V, and the maximum peak-to-peak input voltage $V_{i(p-p)(max)}$ will be 2.0 V; see Figure 7 and Figure 8.

The ADC full-scale input selection principle is shown in Figure 9.

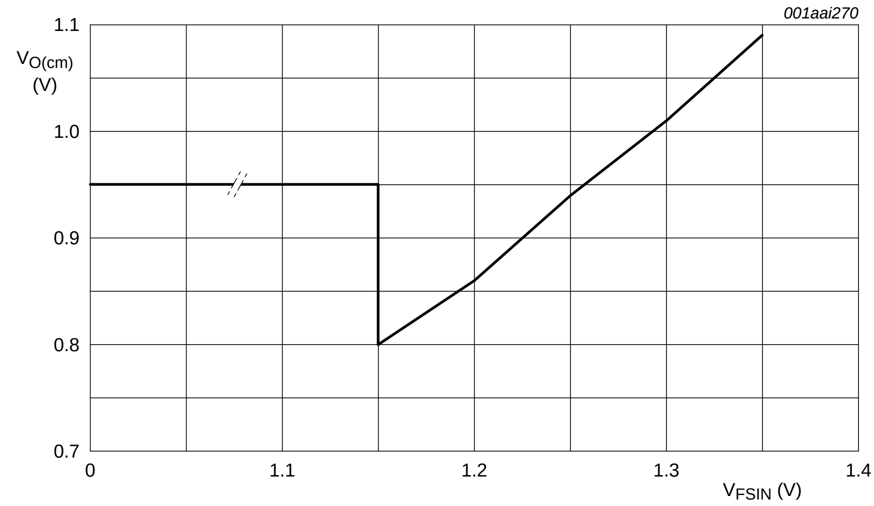


Fig 7. ADC common-mode output voltage $V_{O(cm)}$ as a function of V_{FSIN}

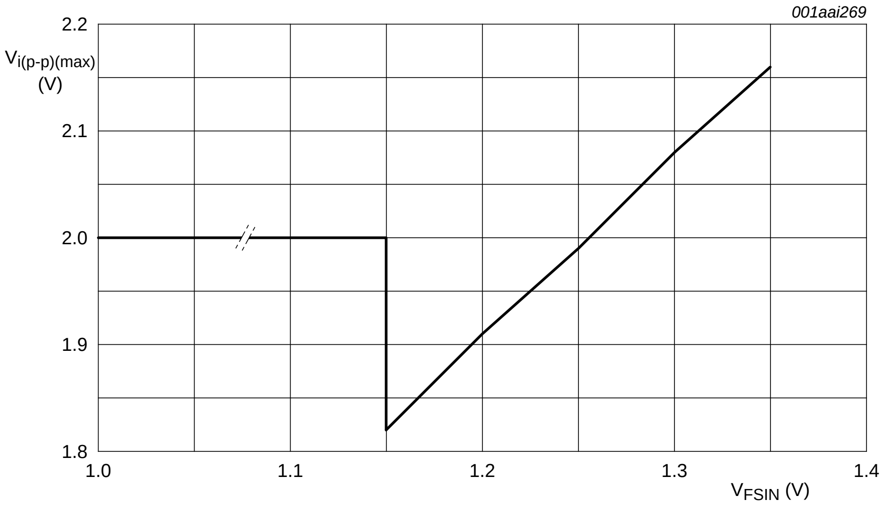


Fig 8. ADC maximum peak-to-peak input voltage $V_{i(p-p)(max)}$ as a function of V_{FSIN}

a. External reference voltage applied

b. Internal reference circuit enabled

Fig 9. ADC full-scale input selection

8. Limiting values

Table 10. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage		–0.5	+4.6	V
V_{CCD}	digital supply voltage		–0.5	+2.5	V
V_{CCO}	output supply voltage		–0.5	+2.5	V
$V_{i(IN)}$	input voltage on pin IN	referenced to AGND	–0.5	V_{CCA} + 1	V
$V_{i(INN)}$	input voltage on pin INN	referenced to AGND	–0.5	V_{CCA} + 1	V
$V_{i(CLK)}$	input voltage on pin CLK	referenced to DGND	–0.5	V_{CCD} + 0.55	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C

9. Thermal characteristics

Table 11. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	36.2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	14.3	K/W

[1] In compliance with JEDEC test board, in free air.

10. Static characteristics

Table 12. Static characteristics
V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = –40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V – 0.5 dB; $V_{I(cm)}$ = 0.95 V; V_{FSIN} = 0 V; typical values are measured at V_{CCA} = 3.3 V, V_{CCD} = V_{CCO} = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			3.0	3.3	3.6	V
V_{CCD}	digital supply voltage			1.65	1.80	1.95	V
V_{CCO}	output supply voltage			1.65	1.80	1.95	V
I_{CCA}	analog supply current	f_{clk} = 125 MHz; f_i = 1.25 MHz		-	60	-	mA
I_{CCD}	digital supply current	f_{clk} = 125 MHz; f_i = 1.25 MHz		-	12	-	mA
I_{CCO}	output supply current	f_{clk} = 125 MHz; f_i = 1.25 MHz		-	11	-	mA
P_{tot}	total power dissipation	f_{clk} = 125 MHz; f_i = 1.25 MHz		-	240	-	mW
Clock inputs: pins CLK+ and CLK–							
R_i	input resistance		[1]	-	10	-	kΩ
C_i	input capacitance		[1]	-	1	-	pF
LVDS clock input; see Figure 3							
ΔV_I	input voltage range	V_I on pin CLK+ or CLK–; $\lvert V_{gpd}\rvert$ < 50 mV	[2]	825	-	1575	mV

Table 12. Static characteristics *…continued*

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; V_{FSIN} = 0 V; typical values are measured at V_{CCA} = 3.3 V, V_{CCD} = V_{CCO} = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{idth}	input differential threshold voltage	$\|V_{gpd}\| < 50$ mV [2]	−100	-	+100	mV
I_I	input current	825 mV < V_I < 1575 mV	-	-	50	µA
1.8 V CMOS clock input; see Figure 4						
V_{IL}	LOW-level input voltage		DGND	-	$0.2V_{CCD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CCD}$	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.2V_{CCD}$	-	-	50	µA
I_{IH}	HIGH-level input current	$V_{IH} = 0.8V_{CCD}$	-	-	50	µA
Analog inputs: pins IN and INN						
R_i	input resistance	[1]	-	1.0	-	MΩ
C_i	input capacitance	[1]	-	1.0	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{i(IN)} = V_{i(INN)}$; output code = 127	0.7	0.95	1.0	V
Digital input pins: OTC, CE_N, DEL0, DEL1, CLKSEL and CCSSEL						
V_{IL}	LOW-level input voltage		DGND	-	$0.2V_{CCD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CCD}$	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.3V_{CCD}$	-	-	50	µA
I_{IH}	HIGH-level input current	$V_{IH} = 0.7V_{CCD}$	-	-	50	µA
Voltage controlled regulator output: pin CMADC						
$V_{O(cm)}$	common-mode output voltage		0.85	0.95	1.1	V
Reference voltage input: pin FSIN[3]						
V_{FSIN}	voltage on pin FSIN	internal reference	-	0	0.6	V
		external reference	1.15	1.25	1.35	V
$I_{i(FSIN)}$	input current on pin FSIN		-	12	-	µA
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	internal reference	1.92	2	2.03	V
		external reference				
		V_{FSIN} = 1.15 V	1.80	1.825	1.85	V
		V_{FSIN} = 1.25 V	1.98	1.99	2.03	V
		V_{FSIN} = 1.35 V	2.11	2.16	2.18	V
Digital outputs: pins D0 to D7, CCS and IR						
V_{OL}	LOW-level output voltage		OGND	-	0.2	V
V_{OH}	HIGH-level output voltage		$V_{CCO} - 0.2$	-	V_{CCO}	V

[1] Guaranteed by design.

[2] $|V_{gpd}|$ is the voltage of ground potential difference across or between boards.

[3] The ADC input range can be adjusted with an external reference voltage applied to pin FSIN. This voltage must be referenced to AGND.

11. Dynamic characteristics

Table 13. Dynamic characteristics

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = –40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V – 0.5 dB; $V_{I(cm)}$ = 0.95 V; V_{FSIN} = 0 V; typical values are measured at V_{CCA} = 3.3 V, V_{CCD} = V_{CCO} = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock timing input: pins CLK+ and CLK–							
$f_{clk(min)}$	minimum clock frequency			-	-	1	MHz
$f_{clk(max)}$	maximum clock frequency			250	-	-	MHz
$t_{w(clk)}$	clock pulse width	f_{clk} = 125 MHz		1.8	-	-	ns
Timing output: pins D0 to D7 and IR[1]; see Figure 5							
$t_{d(s)}$	sampling delay time	1.8 V CMOS clock		-	1.3	-	ns
		LVDS clock		-	1.65	-	ns
$t_{h(o)}$	output hold time	1.8 V CMOS clock		3.3	4.4	-	ns
		LVDS clock		4.2	4.8	-	ns
$t_{d(o)}$	output delay time	1.8 V CMOS clock		-	5.4	6.9	ns
		LVDS clock		-	5.8	7.3	ns
Timing complete conversion signal: pin CCS; see Figure 6							
$f_{CCS(max)}$	maximum CCS frequency			125	-	-	MHz
$t_{d(CCS)}$	CCS delay time	DEL0 = HIGH; DEL1 = LOW		-	0.3	-	ns
		DEL0 = LOW; DEL1 = HIGH		-	0.8	-	ns
		DEL0 = HIGH; DEL1 = HIGH		-	1.9	-	ns
3-state output delay time: pins CCS, IR and D7 to D0							
t_{dZH}	float to active HIGH delay time			-	2.1	-	ns
t_{dZL}	float to active LOW delay time			-	2.2	-	ns
t_{dHZ}	active HIGH to float delay time			-	3.3	-	ns
t_{dLZ}	active LOW to float delay time			-	2.9	-	ns
Analog signal processing (50 % clock duty factor); see Section 12							
INL	integral non-linearity	f_{clk} = 20 MHz; f_i = 21.4 MHz		-	±0.82	-	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; f_i = 21.4 MHz; no missing code guaranteed		-	±0.4	-	LSB
E_O	offset error	V_{CCA} = 3.3 V; V_{CCD} = 1.8 V; T_{amb} = 25 °C; output code = 127		-	2.5	-	mV
E_G	gain error	spread from device to device; V_{CCA} = 3.3 V; V_{CCD} = 1.8 V; T_{amb} = 25 °C		-	1.85	-	%
B	bandwidth	f_{clk} = 125 MHz; –3 dB; full-scale input	[2]	-	560	-	MHz
THD	total harmonic distortion	f_{clk} = 125 MHz; f_i = 78 MHz	[3]	-	–53	-	dB
		f_{clk} = 250 MHz; f_i = 125 MHz		-	–53	-	dB
$N_{th(RMS)}$	RMS thermal noise	shorted input; f_{clk} = 125 MHz		-	0.5	-	LSB
S/N	signal-to-noise ratio	f_{clk} = 125 MHz; f_i = 78 MHz	[4]	-	48	-	dBc
		f_{clk} = 250 MHz; f_i = 125 MHz		-	47	-	dBc

Table 13. Dynamic characteristics *…continued*

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; V_{FSIN} = 0 V; typical values are measured at V_{CCA} = 3.3 V, V_{CCD} = V_{CCO} = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SFDR	spurious free dynamic range	f_{clk} = 125 MHz; f_i = 78 MHz		-	55	-	dBc
		f_{clk} = 250 MHz; f_i = 125 MHz		-	55	-	dBc
IMD2	second-order intermodulation distortion	f_1 = 124 MHz; f_2 = 126 MHz; f_{clk} = 250 MHz	[5]	-	−55	-	dB
IMD3	third-order intermodulation distortion	f_1 = 124 MHz; f_2 = 126 MHz; f_{clk} = 250 MHz	[5]	-	−60	-	dB

[1] Output data acquisition: the output data is available after the maximum delay of $t_{d(o)}$.

[2] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[3] The total harmonic distortion is obtained with the addition of the first five harmonics.

[4] The signal-to-noise ratio takes into account all harmonics above five and noise up to Nyquist frequency.

[5] Intermodulation measured relative to either tone with analog input frequencies f_1 and f_2. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full-scale for each input signal). IMD3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third-order intermodulation product.

12. Definitions

12.1 Static parameters

12.1.1 Integral non-linearity

Integral non-linearity (INL) is defined as the deviation of the transfer function from a best-fit straight line (linear regression computation). The INL of the code is obtained from the equation:

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S} \tag{1}$$

where: S corresponds to the slope of the ideal straight line (code width), i corresponds to the code value, V_{in} is the input voltage.

12.1.2 Differential non-linearity

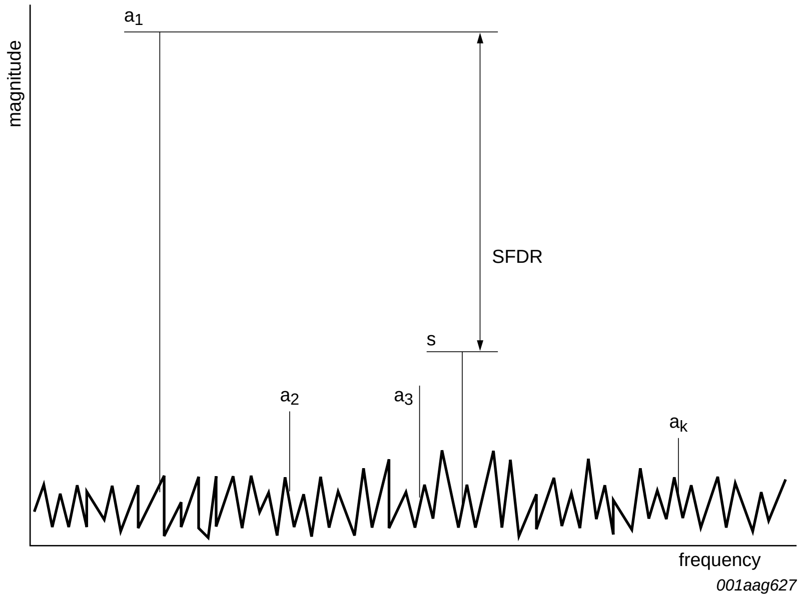
Differential non-linearity (DNL) is the deviation in code width from the value of 1 LSB.

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S} \tag{2}$$

where: V_{in} is the input voltage; i is a code value from 0 to ($2^n - 2$).

12.2 Dynamic parameters

Figure 10 shows the spectrum of a single tone full-scale input sine wave of frequency f_t, conforming to coherent sampling and which is digitized by the ADC under test. Coherent sampling: (f_t / f_s = M / N, where M = number of cycles and N = number of samples, M and N values being relatively prime).



a = harmonic.

s = single tone.

Fig 10. Single tone spectrum of full-scale input sine wave of frequency f_t

Remark: P_{noise} in the equations in the following sections, is the sum of noise sources which include random noise, non-linearities, sampling time errors, and quantization noise.

12.2.1 Signal-to-Noise And Distortion (SINAD)

SINAD is the ratio of the output signal power to the noise plus distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD[dB] = 10\log_{10}\left(\frac{P_{signal}}{P_{noise+distortion}}\right) \quad (3)$$

12.2.2 Effective Number Of Bits (ENOB)

ENOB is derived from SINAD and gives the theoretical resolution required by an ideal ADC to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

12.2.3 Total Harmonic Distortion (THD)

THD is the ratio of the power of the harmonics to the power of the fundamental. For k – 1 harmonics the THD is:

$$THD[dB] = 10\log_{10}\left(\frac{P_{harmonics}}{P_{signal}}\right) \quad (5)$$

where:

$$P_{harmonics} = a_2^2 + a_3^2 + \ldots + a_k^2 \quad (6)$$

$$P_{signal} = a_1^2 \quad (7)$$

The value of k is usually 6 (THD is calculated based on the first 5 harmonics).

12.2.4 Signal-to-Noise ratio (S/N)

S/N is the ratio of the output signal power to the noise power, excluding the harmonics and the DC component:

$$S/N = 10log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) \quad (8)$$

12.2.5 Spurious Free Dynamic Range (SFDR)

The SFDR value specifies the available signal range as the spectral distance between the amplitude of the fundamental (a_1) and the amplitude of the largest spurious harmonic and non-harmonic (max (s)), excluding the DC component:

$$SFDR[dB] = 20log_{10}\left(\frac{a_1}{max(s)}\right) \quad (9)$$

12.2.6 InterModulation Distortion (IMD)

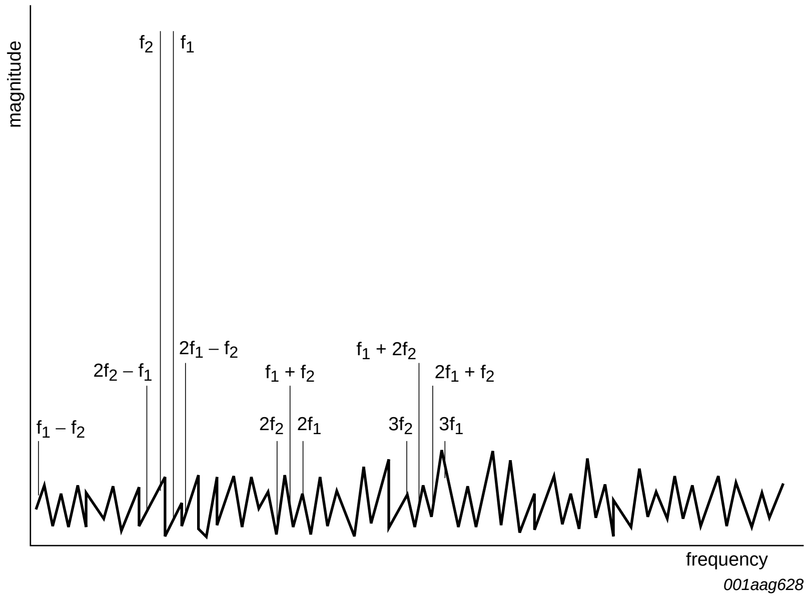


Fig 11. Spectrum of dual tone input sine wave of frequencies f_1 and f_2

The second-order and third-order intermodulation distortion products IMD2 and IMD3 are defined using a dual tone input sinusoid, where f_1 and f_2 are chosen according to the coherence criterion.

IMD is the ratio of the RMS value of either tone to the RMS value of the worst, second or third-order intermodulation products.

The total intermodulation distortion is given by:

$$IMD[dB] = 10log_{10}\left(\frac{P_{intermod}}{P_{signal}}\right) \quad (10)$$

where:

$$\begin{aligned} P_{intermod} = {} & a^2_{im(f_1-f_2)} - a^2_{im(f_1+f_2)} + a^2_{im(f_1-2f_2)} + a^2_{im(f_1+2f_2)} + \ldots \\ & \ldots + a^2_{im(2f_1-f_2)} + a^2_{im(2f_1+f_2)} \end{aligned} \quad (11)$$

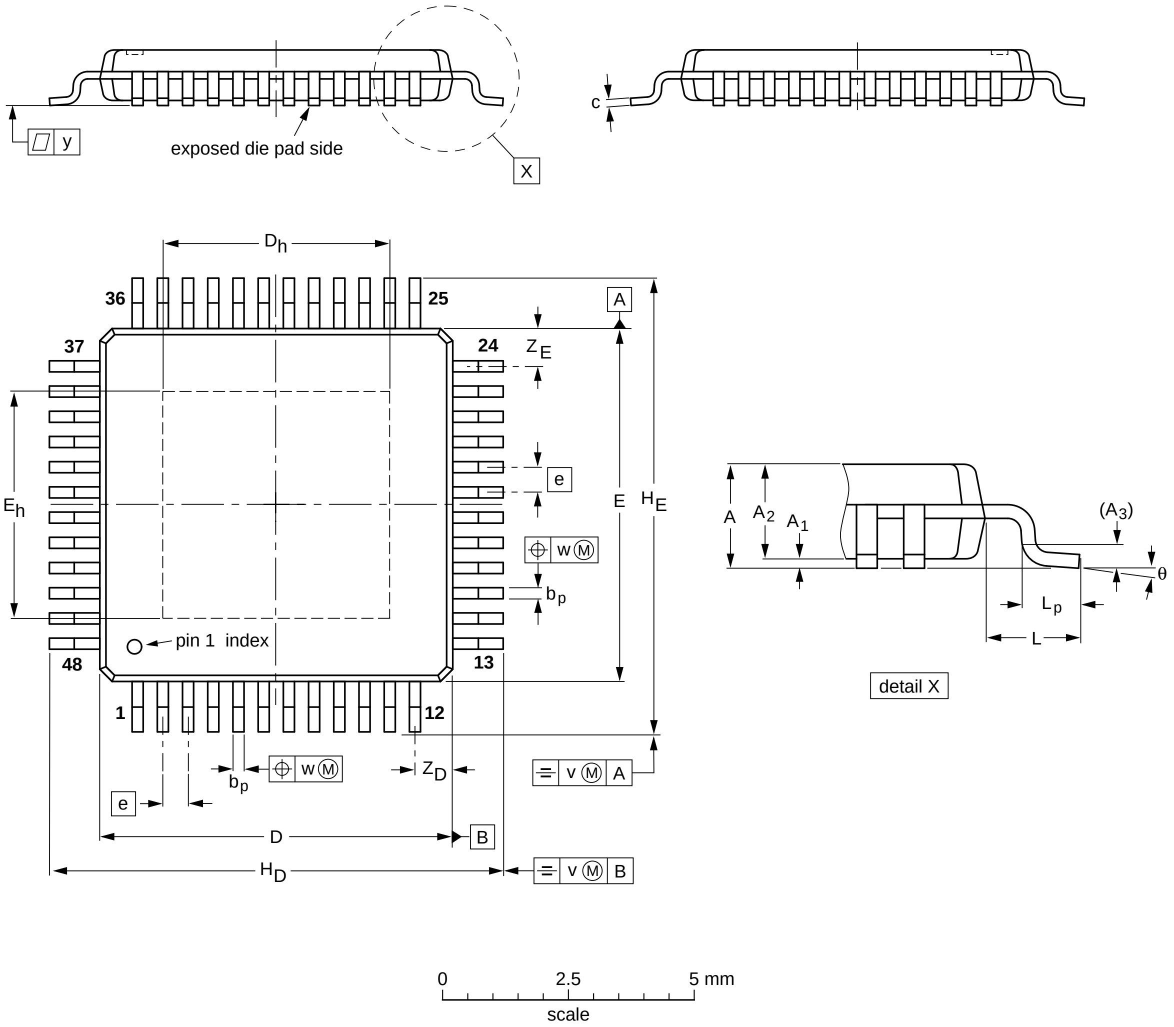
where $a^2_{im(f_n)}$ is the power in the intermodulation component at f_n.

$$P_{signal} = a^2_{f_1} + a^2_{f_2} \quad (12)$$

13. Package outline

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad

SOT545-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.9 0.6	0.9 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2		MS-026				~~03-04-07~~ 04-01-29

Fig 12. Package outline SOT545-2 (HTQFP48)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020C)

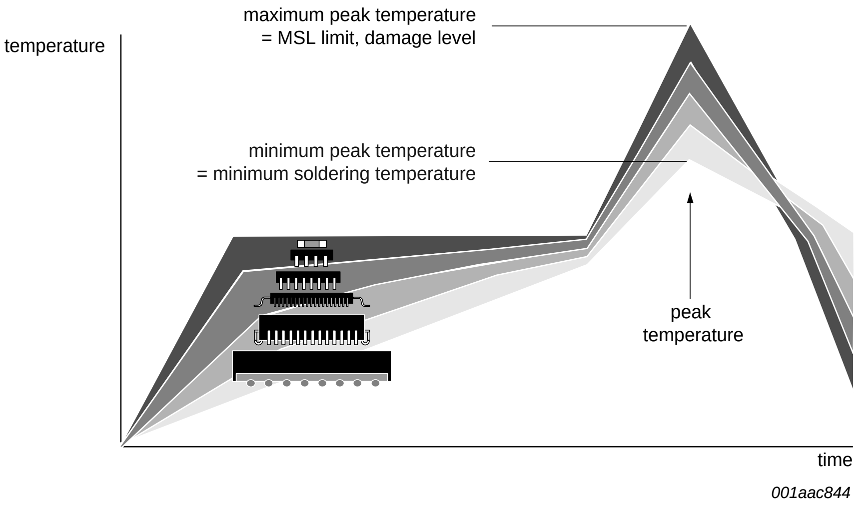
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC0808S125_ADC0808S250_4	20120702	Product data sheet	-	ADC0808S125_ADC0808S250_3
ADC0808S125_ADC0808S250_3	20090224	Product data sheet	-	ADC0808S125_ADC0808S250_2
Modifications:	• Table 13 updated.			
ADC0808S125_ADC0808S250_2	20081007	Product data sheet	-	TDA9917_1
TDA9917_1	20060609	Objective data sheet	-	-

16. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

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