Ordering number : ENA1589A

STK672-642A-E

ON Semiconductor®

http://onsemi.com

Thick-Film Hybrid IC

2-phase Stepping Motor Driver

Overview

The STK672-642A-E is a hybrid IC for use as a unipolar, 2-phase stepping motor driver with PWM current control.

Applications

- Office photocopiers, printers, etc.

Features

- Built-in overcurrent detection function (output current OFF).
- Built-in overheat detection function (output current OFF).
- If either over-current or overheat detection function is activated, the FAULT signal (active low) is output.
- Built-in power on reset function.
- The motor speed is controlled by the frequency of an external clock signal.
- 2 phase or 1-2 phase excitation switching function.
- Using either or both edges of the clock signal switching function.
- Phase is maintained even when the excitation mode is switched.
- Rotational direction switching function.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.089Ω: resistor tolerance ±2%), motor current can be set using two external resistors.
- The ENABLE pin can be used to cut output current while maintaining the excitation mode.
- With a wide current setting range, power consumption can be reduced during standby.
- No motor sound is generated during hold mode due to external excitation current control.
- Miniature package (provides pin compatibility with STK672-640A-E)

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +6.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +6.0	V
Output current 1	I_{OP} max	10μA, 1 pulse (resistance load)	20	A
Output current 2	I_{OH} max	V_{DD}=5V, CLOCK≥200Hz	4	A
Output current 3	I_{OF} max	Pin16 output current	10	mA
Allowable power dissipation 1	PdMF max	With an arbitrarily large heat sink. Per MOSFET	8.3	W
Allowable power dissipation 2	PdPK max	No heat sink	2.8	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	10 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input high voltage	V_{IH}	Pins 10, 12, 13, 14, 15, 17	2.5 to V_{DD}	V
Input low voltage	V_{IL}	Pins 10, 12, 13, 14, 15, 17	0 to 0.8	V
Output current 1	$I_{OH}1$	Tc=105°C, CLOCK≥200Hz, Continuous operation, duty=100%	3.0	A
Output current 2	$I_{OH}2$	Tc=80°C, CLOCK≥200Hz, Continuous operation, duty=100%, See the motor current (I_{OH}) derating curve	3.3	A
CLOCK frequency	f_{CL}	Minimum pulse width: at least 10μs	0 to 50	kHz
Phase driver withstand voltage	V_{DSS}	I_D=1mA (Tc=25°C)	100min	V
Recommended operating substrate temperature	Tc	No condensation	0 to 105	°C
Recommended Vref range	Vref	Tc=105°C	0.14 to 1.31	V

Refer to the graph for each conduction-period tolerance range for the output current and brake current.

Electrical Characteristics at Tc=25°C, V_{CC}=24V, V_{DD}=5.0V

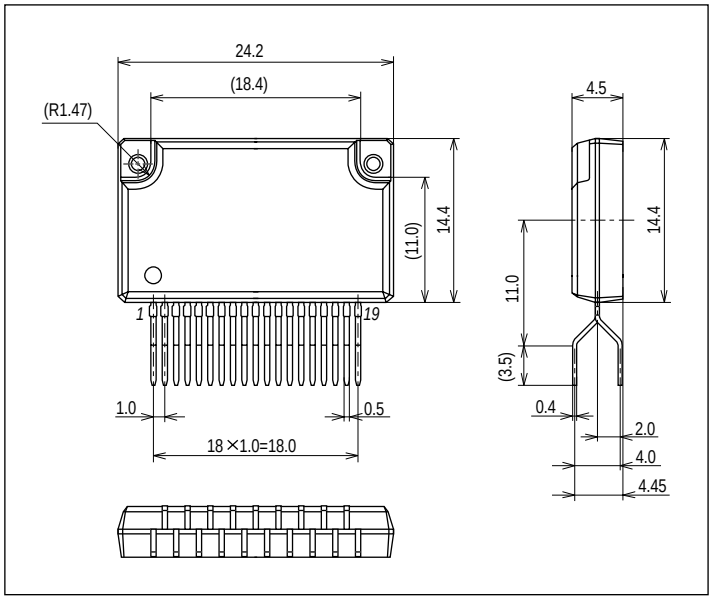
Parameter	Symbol	Conditions	min	typ	max	unit
V_{DD} supply current	I_{CCO}	Pin 9 current CLOCK=GND		4.4	8	mA
Output average current	Ioave	R/L=1Ω/0.62mH in each phase	0.519	0.625	0.731	A
FET diode forward voltage	Vdf	If=1A (R_L=23Ω)		0.83	1.5	V
Output saturation voltage	Vsat	R_L=23Ω		0.20	0.33	V
Input high voltage	V_{IH}	Pins 10, 12, 13, 14, 15, 17	2.5			V
Input low voltage	V_{IL}	Pins 10, 12, 13, 14, 15, 17			0.8	V
FAULT low output voltage	V_{OLF}	Pin 16 (I_O=5mA)		0.25	0.5	V
5V level FAULT leakage current	I_{ILF}	Pin 16=5V			10	μA
5V level input current	I_{ILH}	Pins 10, 12, 13, 14, 15, 17=5V		50	75	μA
GND level input current	I_{ILL}	Pins 10, 12, 13, 14, 15, 17=GND			10	μA
Vref input bias current	I_{IB}	Pin 19=1.0V		10	15	μA
PWM frequency	fc		29	45	61	kHz
Overheat detection temperature	TSD	Design guarantee		144		°C

*Ioave values are for when the lead frame of the product is soldered to the mounting substrate.

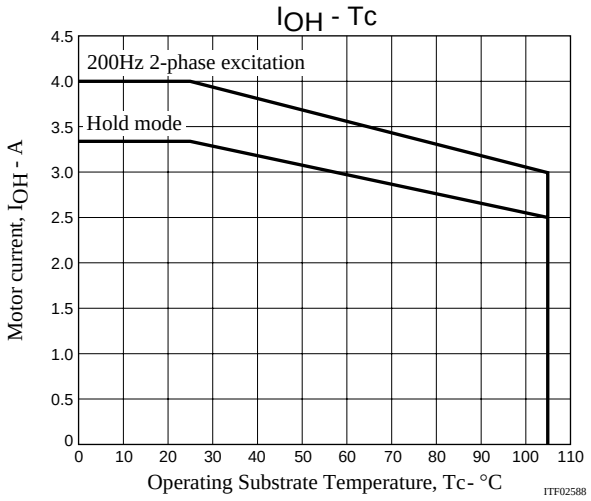
Notes: A fixed-voltage power supply must be used.

Package Dimensions

unit:mm (typ)



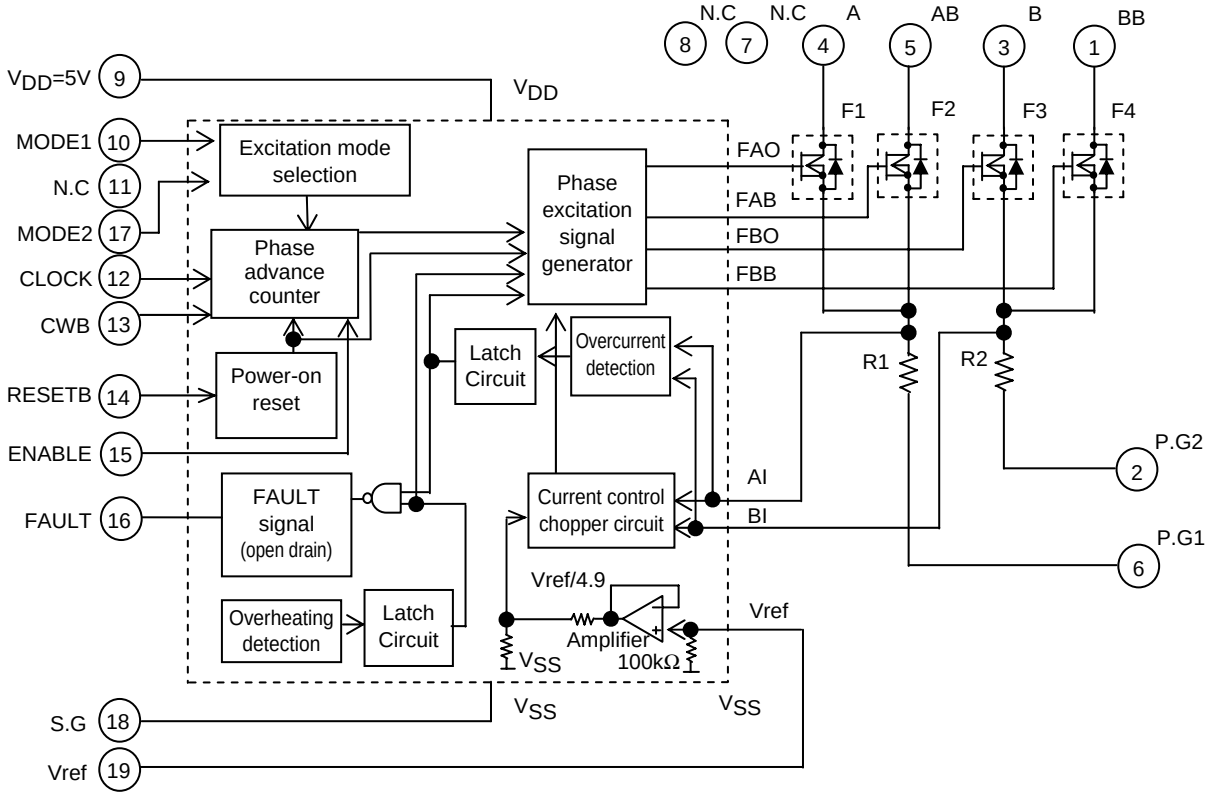
Derating curve of motor current, I_{OH}, vs. Operating substrate temperature, Tc



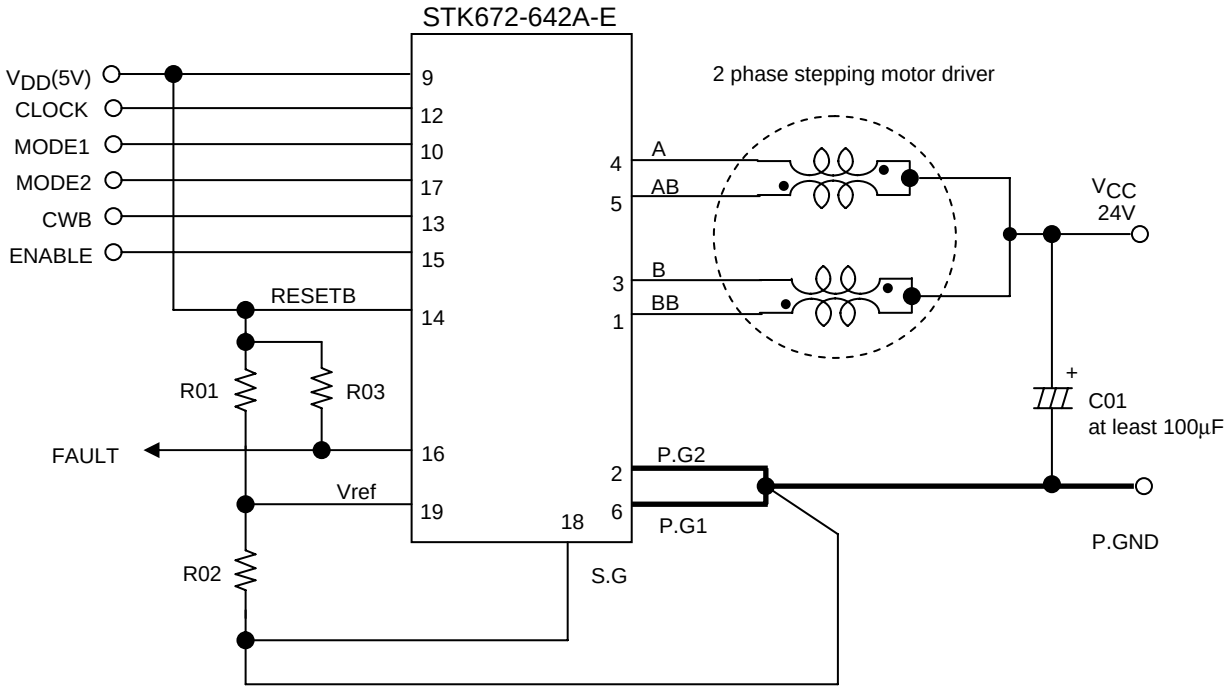
Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-6** series hybrid ICs given in a separate document.
- The operating substrate temperature, Tc, given above is measured while the motor is operating.
- Because Tc varies depending on the ambient temperature, Ta, the value of I_{OH}, and the continuous or intermittent operation of I_{OH}, always verify this value using an actual set.
- The Tc temperature should be checked in the center of the metal surface of the product package.

Block Diagram



Sample Application Circuit



Precautions

[GND wiring]

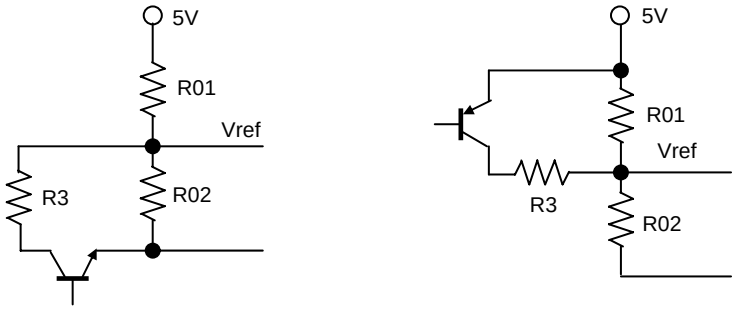
- To reduce noise on the 5V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the hybrid IC. Also, to achieve accurate current settings, be sure to connect Vref GND to Pin 18 (S.G) used to set the current and to the point where P.G1 and P.G2 share a connection.

[Input pins]

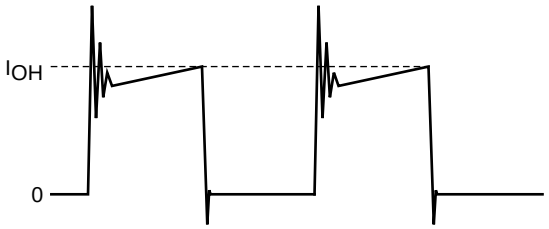
- If V_{DD} is being applied, use care that each input pin does not apply a negative voltage less than -0.3V to S.G, Pin 18, and do not apply a voltage greater than or equal to V_{DD} voltage.
- Do not wire by connecting the circuit pattern on the P.C.B side to Pins 7, 8, or 11 on the N.C. shown in the internal block diagram.
- Apply 2.5V high level input to pins 10, 12, 13, 14, 15, and 17.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 10, 12, 13, 14, 15, and 17 are used as inputs, a 1 to 20kΩ pull-up resistor (to V_{DD}) must be used.
  At this time, use a device for the open collector driver that has output current specifications that pull the voltage down to less than 0.8V at Low level (less than 0.8V at Low level when I_{OL}=5mA).

[Current setting Vref]

- Considering the specifications of the Vref input bias current, I_{IB}, a value of 1kΩ or less is recommended for R02.
  If the motor current is temporarily reduced, the circuit given below (STK672-630A-E, 632A-E: I_{OH}>0.2A, STK672-640A-E, 642A-E: I_{OH}>0.3A) is recommended.



- Motor current peak value I_{OH} setting



I_{OH}=(Vref÷4.9) ÷Rs
The value of 4.9 in Equation above represents the Vref voltage as divided by a circuit inside the control IC.
Vref=(R02÷ (R01+R02)) ×5V(or 3.3V)
Rs is an internal current detection resistor value of the hybrid IC.
Rs=0.089Ω when using the STK672-642A-E

[Smoke Emission Precuations]
If Pin 18 (S.G terminal) is attached to the PCB without using solder, overcurrent may flow into the MOSFET at V_{CC}ON (24V ON), causing to emit smoke because 5V circuits cannot be controlled.
In addition, as long as one of the output Pins, 1, 3, 4, or 5, is open, inductance energy stored in the motor results in electrical stress on the driver, possibly resulting in the emission of smoke.

Input Pin Functions

Pin Name	Pin No.	Function	Input Conditions When Operating
CLOCK	12	Reference clock for motor phase current switching	Operates on the rising edge of the signal (MODE2=H)
MODE1	10	Excitation mode selection	Low: 2-phase excitation High: 1-2 phase excitation
MODE2	17		High: Rising edge Low: Rising and falling edge
CWB	13	Motor direction switching	Low: CW (forward) High: CCW (reverse)
RESETB	14	System reset Initial state of A and BB phase excitation in the timing charts is set by switching from low to high.	A reset is applied by a low level
ENABLE	15	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

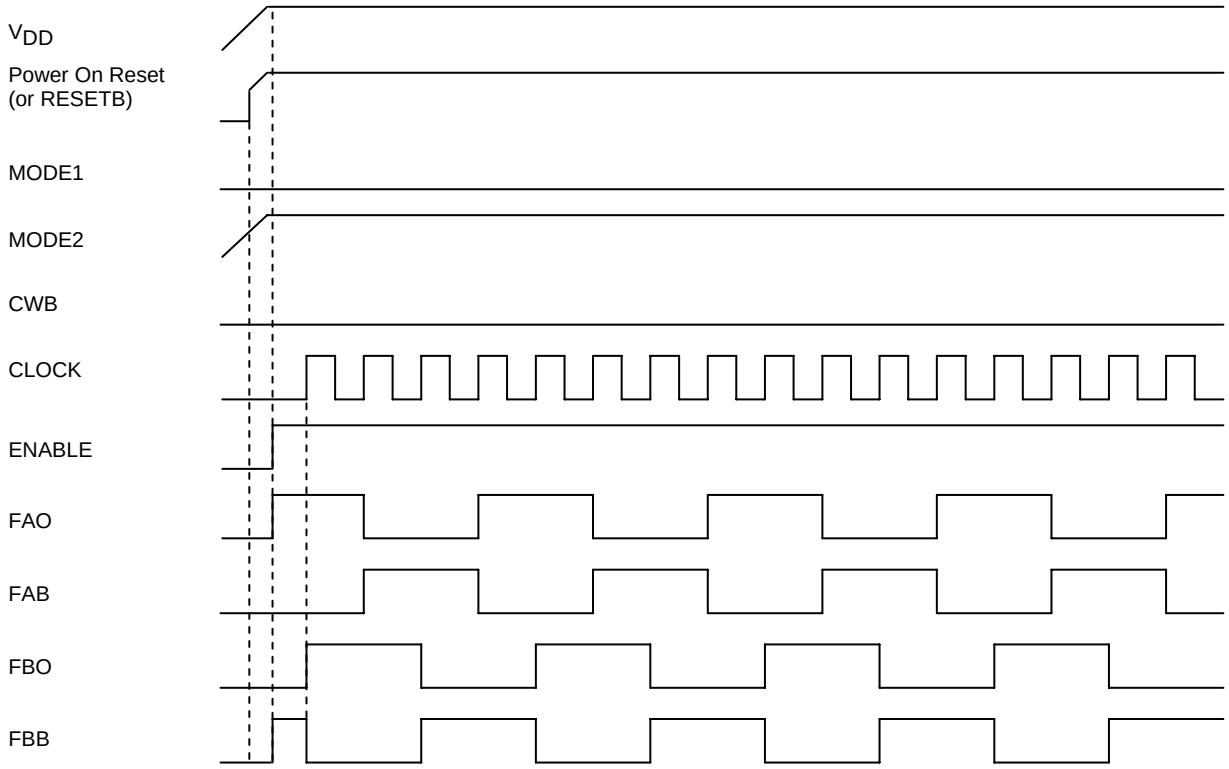
Output Pin Functions

Pin Name	Pin No.	Function	Input Conditions When Operating
FAULT	16	Monitor pin used when over-current detection or overheat detection function is activated.	Low level is output when detected.

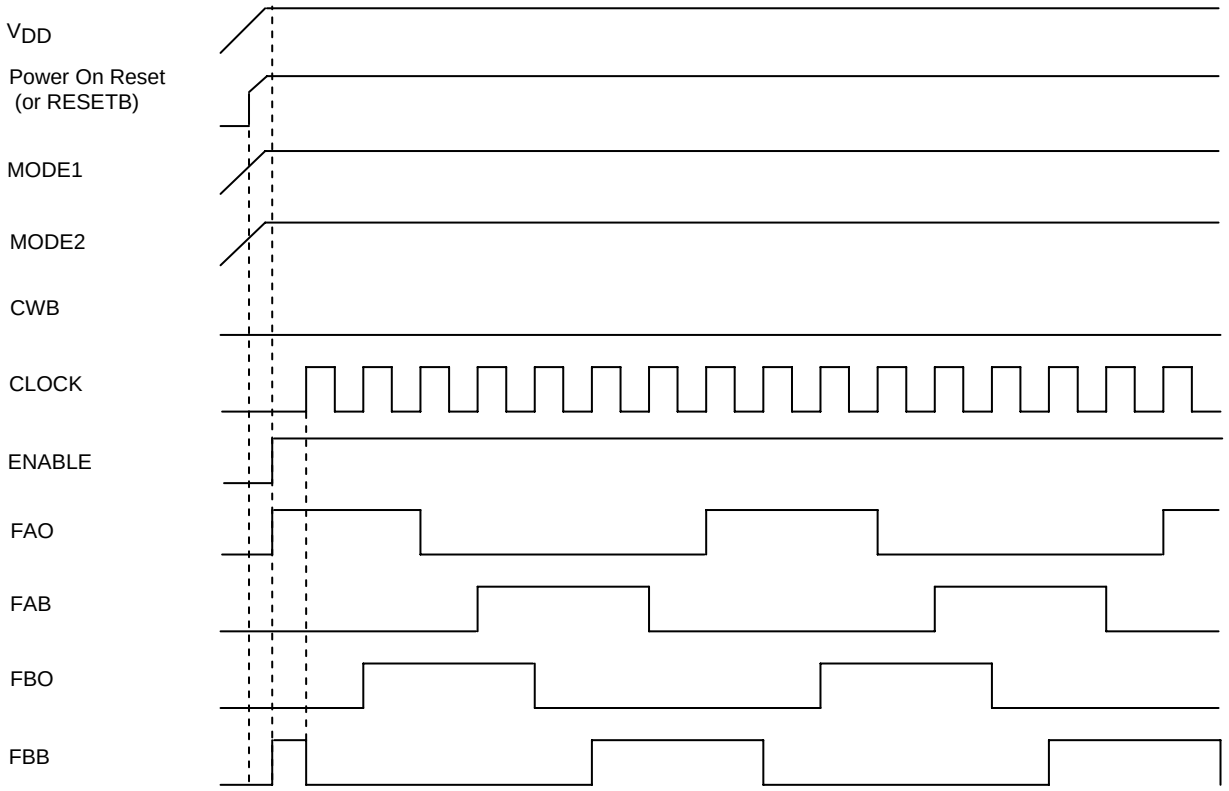
Note: See the timing chart for the concrete details on circuit operation.

Timing Charts

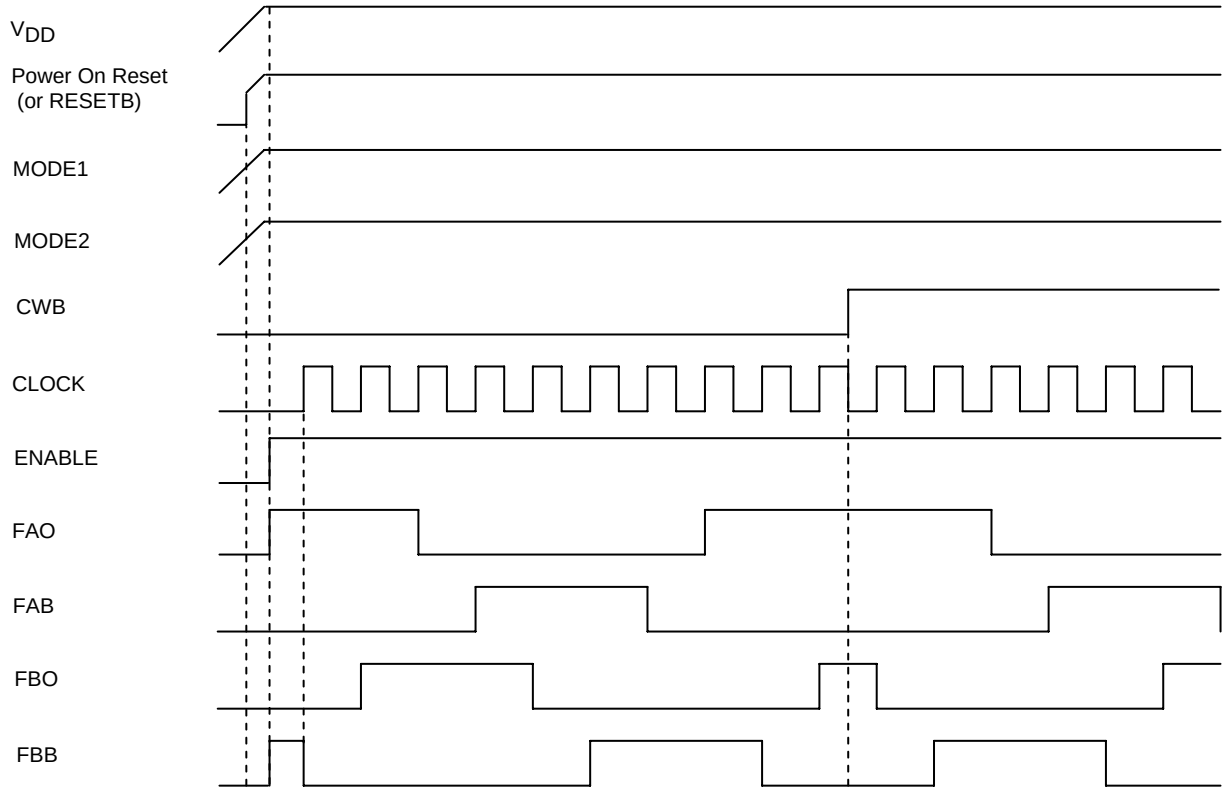
2-phase excitation



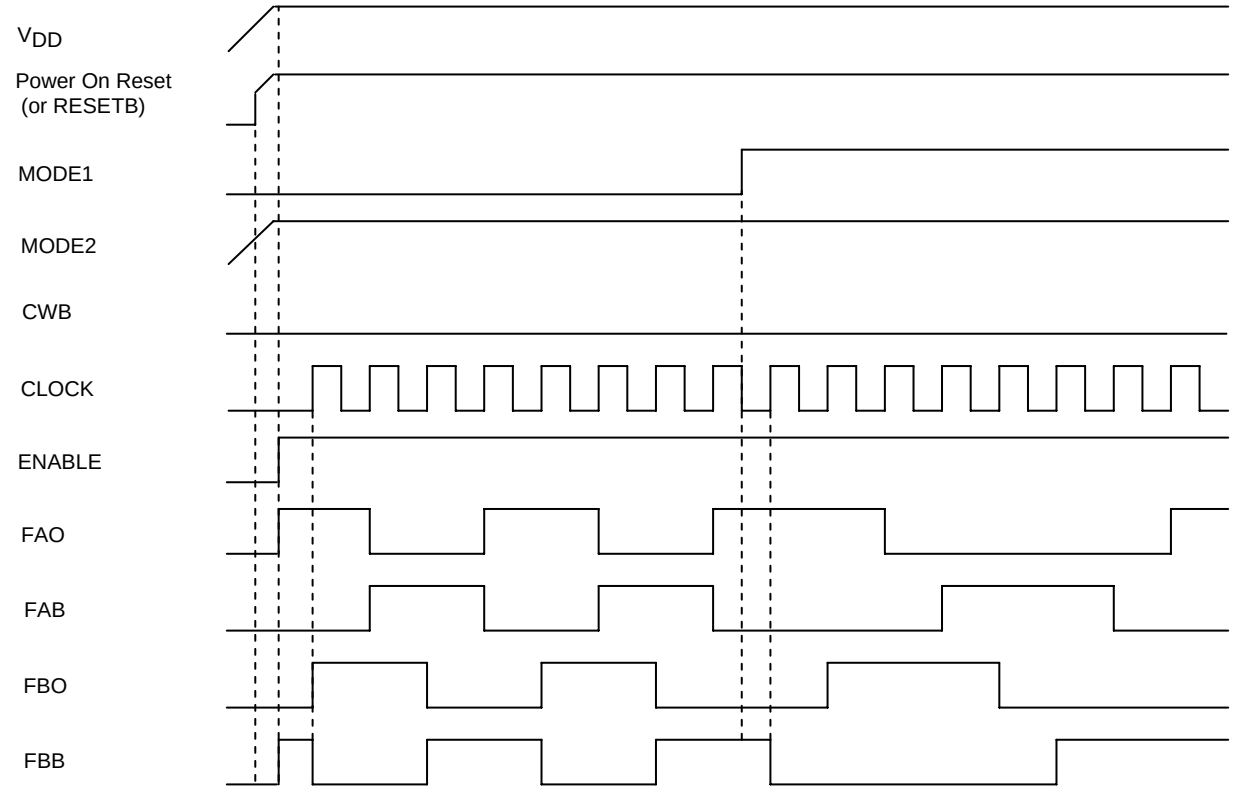
1-2 phase excitation



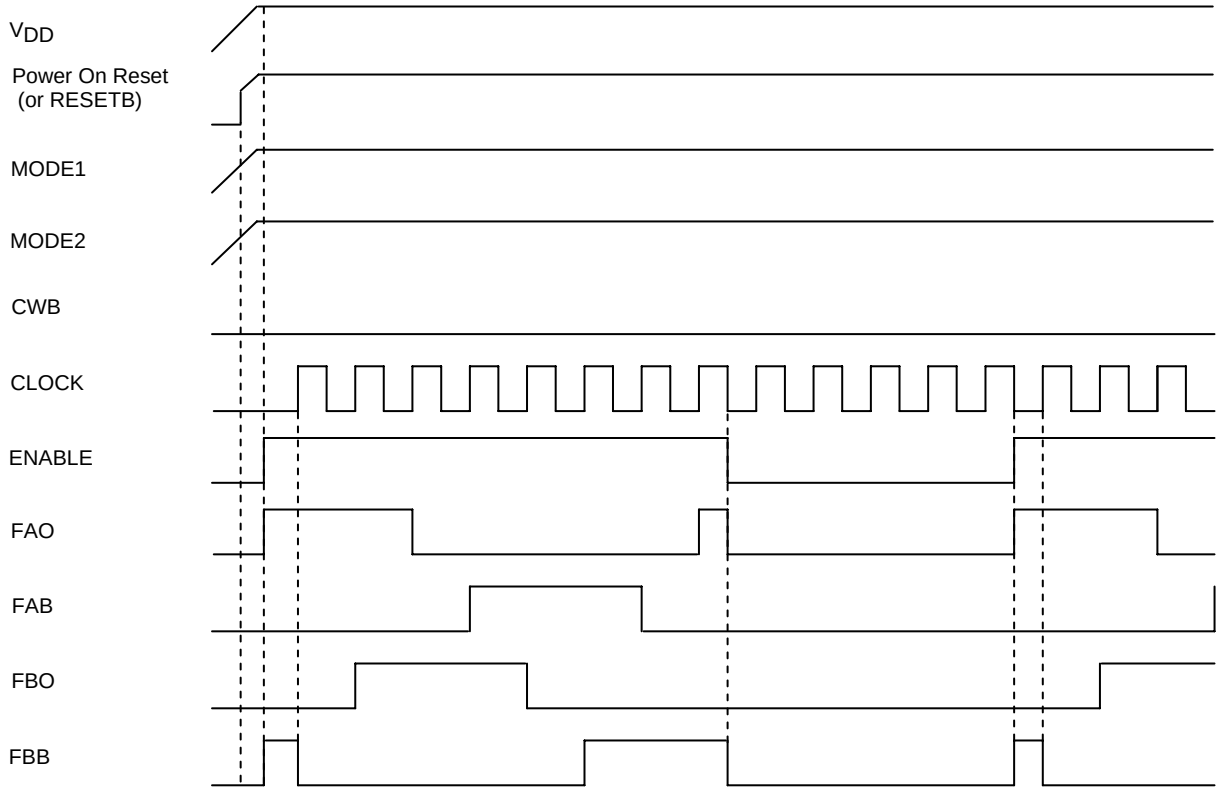
1-2 phase excitation (CWB)



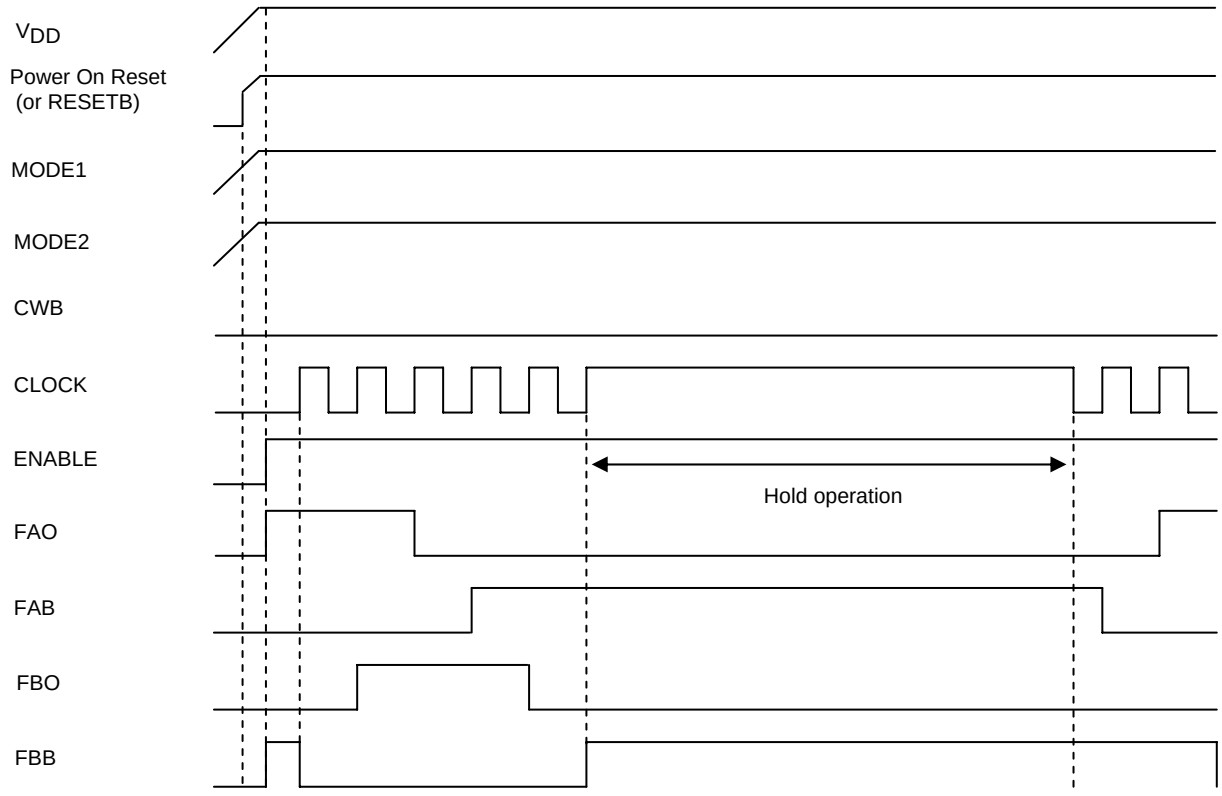
2 phase excitation → Switch to 1-2 phase excitation



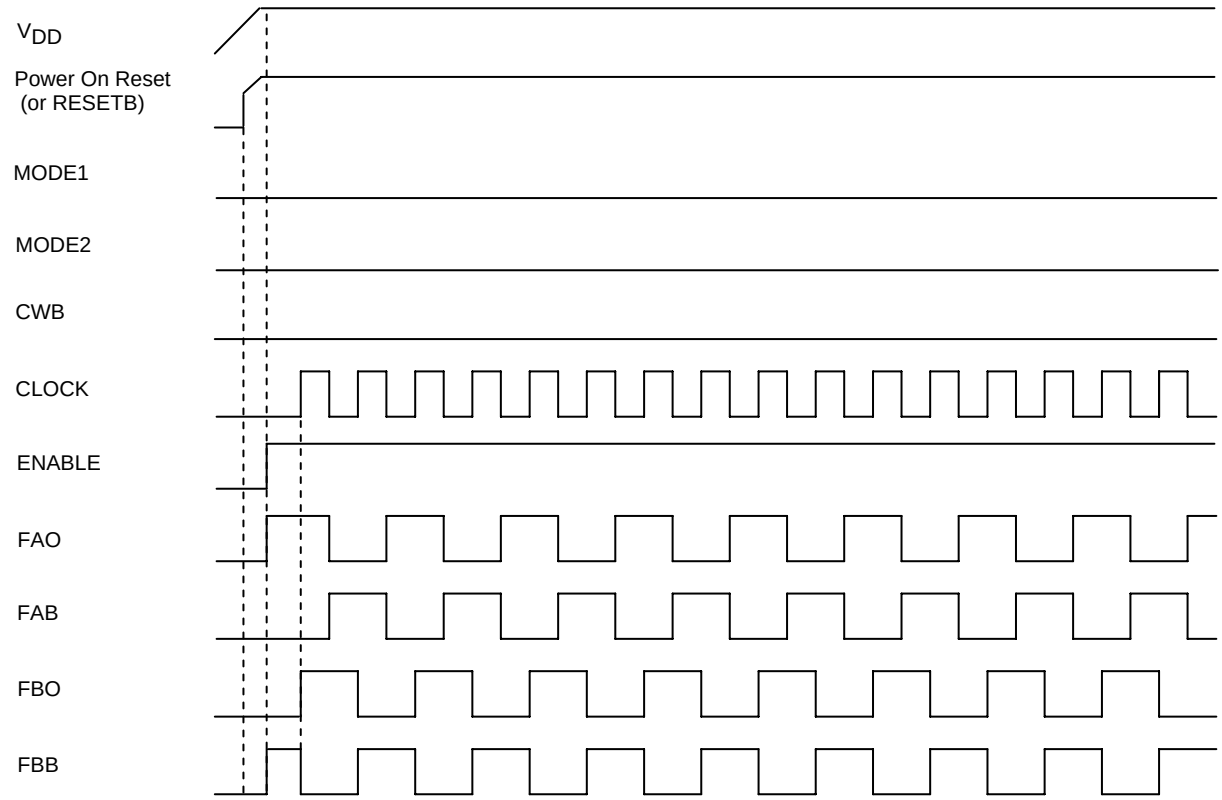
1-2 phase excitation (ENABLE)



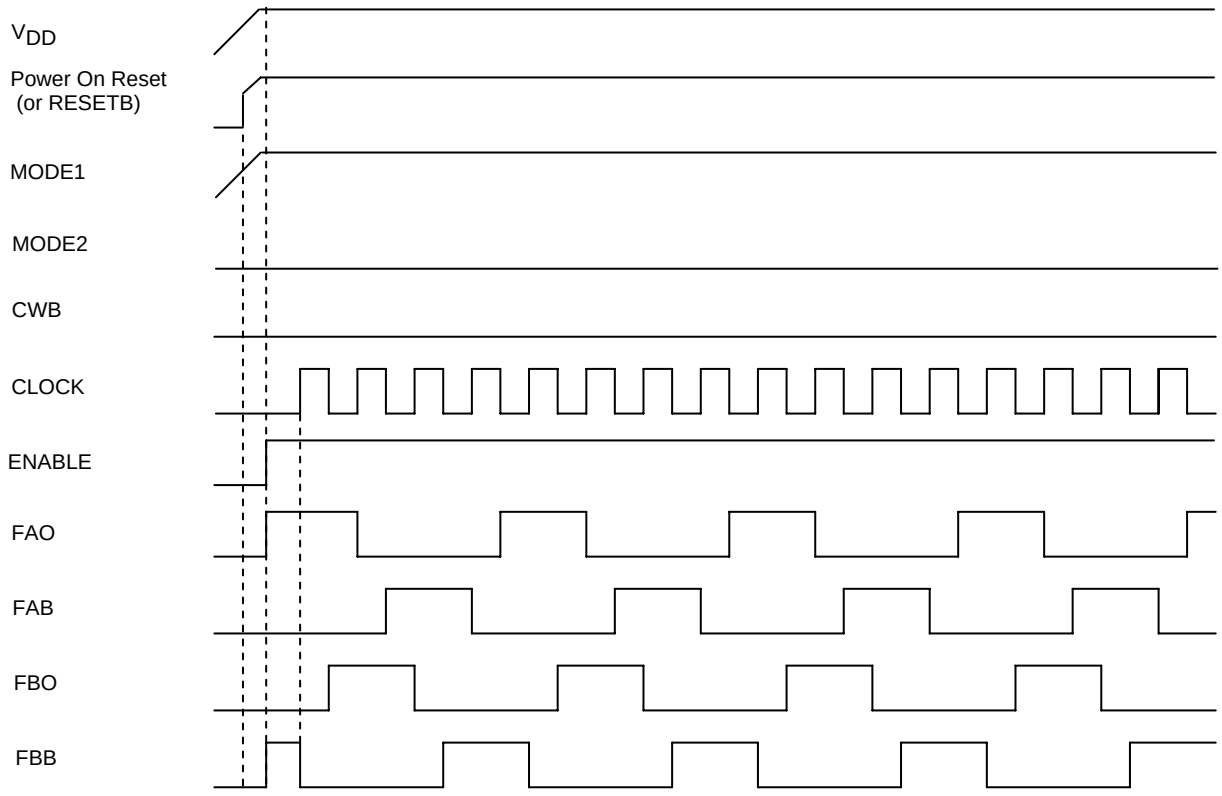
1-2 phase excitation (Hold operation results during fixed CLOCK)



2 phase excitation (MODE 2)



1-2 phase excitation (MODE 2)



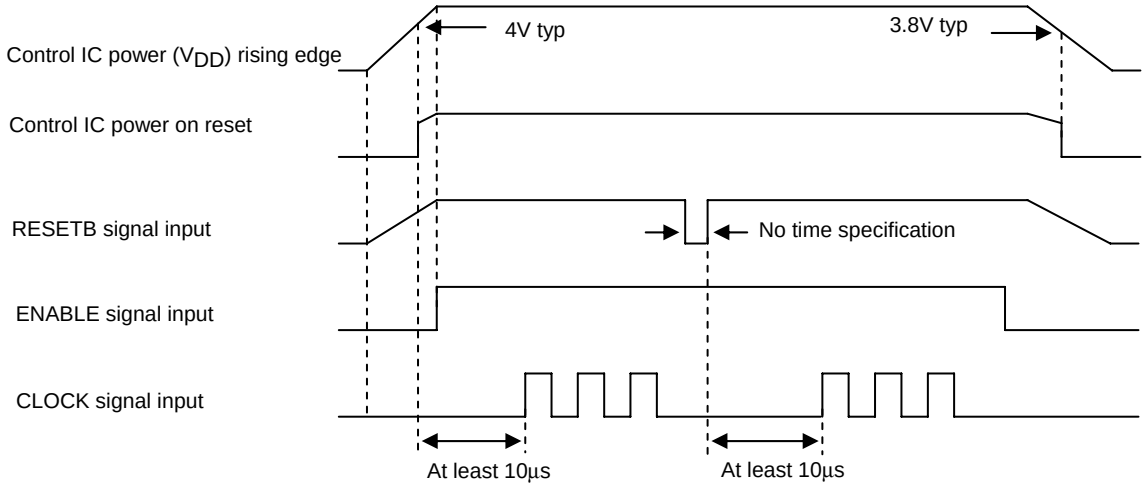
Usage Notes

1. Input signal functions and timing

[ENABLE, CLOCK and power on reset, RESETB (Input signal timing when power is first applied)]

The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is 5V±5%, conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE=Low while V_{DD}, which is outside the operating supply voltage, is less than 4.75V.

In addition, if the RESETB terminal is used to initialize output timing, be sure to allow at least 10μs until CLOCK input.



ENABLE, CLOCK, and RESETB Signals Input Timing

[CLOCK (Phase switching clock)]

- Input frequency: DC to 50kHz
- Minimum pulse width: 10μs
- MODE2=1(High) Signals are read on the rising edge.
- MODE2=0(Low) Signals are read on the rising and falling edges.

[CWB (Motor direction setting)]

The direction of rotation is switched by setting CWB to 1 (high) or 0 (low).

See the timing charts for details on the operation of the outputs.

Note: The state of the CWB input must not be changed during the 6.25μs period before and after the rising edge of the CLOCK input.

[ENABLE (Forcible on/off control of the A, AB, B, and BB outputs, and hybrid IC internal operation)]

ENABLE=1: Normal operation

ENABLE=0: Outputs A, AB, B, and BB forced to the off state.

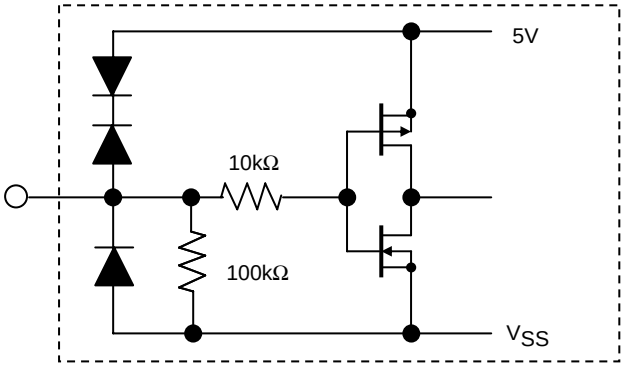
If, during the state where CLOCK signal input is provided, the ENABLE pin is set to 0 and then is later restored to the 1 state, the IC will resume operation with the excitation timing continued from before the point ENABLE was set to 0.

If sudden stop is applied to the CLOCK signal used for motor rotation, the motor axis may advance beyond the theoretical position due to inertia. To stop at the theoretical position, the SLOW DOWN setting for gradually slowing the CLOCK cycle is required.

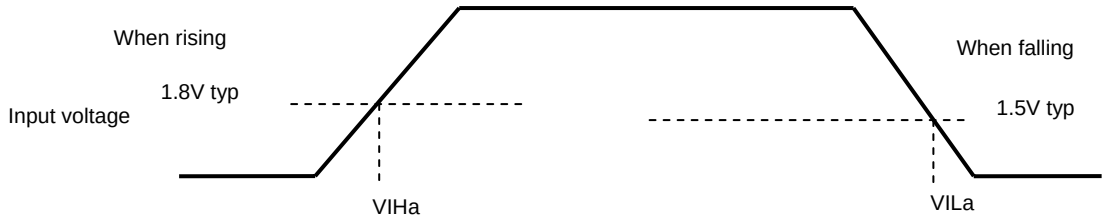
[MODE1 and MODE2 (Excitation mode selection)]
MODE1=0: 2-phase excitation
MODE2=1: Rising edge of CLOCK
MODE1=1: 1-2 phase excitation
MODE2=0: Rising and falling edges of CLOCK
See the timing charts for details on output operation in these modes.

Note: The state of the MODE input must not be changed during the 5μs period before and after the rising edge of the CLOCK input.

[Configuration of Each Input Pin]
<Configuration of the MODE1, MODE2, CLOCK, CWB, ENABLE, and RESETB input pins>
Input pins: Pin 10, 17, 12, 13, 15, and 14

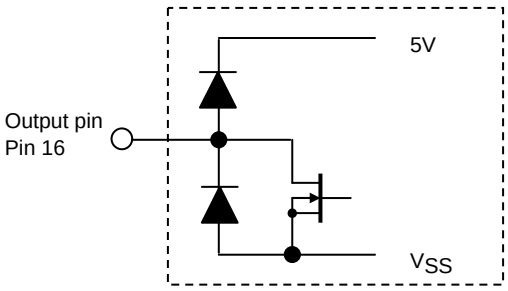


All input pins of this driver support schmitt input. Typ specifications at Tc = 25°C are given below. Hysteresis voltage is 0.3V (VIHa-VILa).

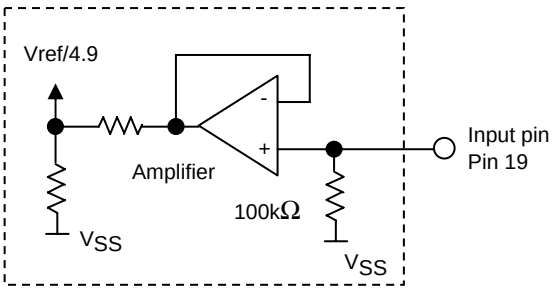


Input voltage specifications are as follows.
V_{IH}=2.5V min
V_{IL}=0.8V max

<Configuration of the FAULT Input Pin>



<Configuration of the Vref Input Pin>



The internal impedance, 100kΩ, is designed so that the increase in current is prevented while Pin 19 is open.
The recommended Vref voltage is 0.14V or higher because the output offset voltage of Vref/4.9 amplifier cannot be controlled down to 0V

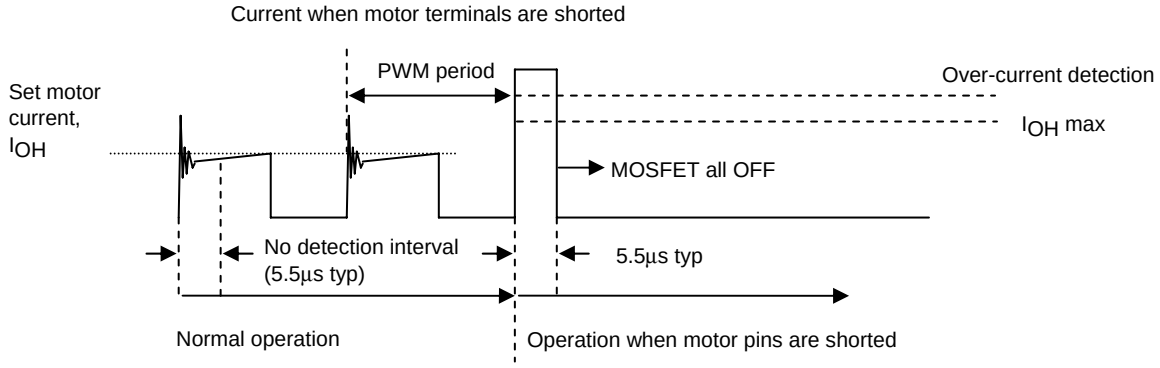
2. Overcurrent Detection and Overheat Detection Functions

Each detection function operates using a latch system and turns output off. Because a RESET signal is required to restore output operations, once the power supply, V_{DD}, is turned off, you must either again apply power on reset with V_{DD}ON or apply a RESETB=High→Low→High signal.

[Overcurrent detection]

This hybrid IC is equipped with a function for detecting overcurrent that arises when the motor burns out or when there is a short between the motor terminals.

Overcurrent detection occurs at 5.5A typ with the STK672-642A-E.



Overcurrent detection begins after an interval of no detection (a dead time of 5.5µs typ) during the initial ringing part during PWM operations. The no detection interval is a period of time where overcurrent is not detected even if the current exceeds I_{OH}.

[Overheat detection]

Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144°C typ).

Within the allowed operating range recommended in the specification manual, if a heat sink attached for the purpose of reducing the operating substrate temperature, Tc, comes loose, the semiconductor can operate without breaking. However, we cannot guarantee operations without breaking in the case of operations other than those recommended, such as operations at a current exceeding I_{OH} max that occurs before overcurrent detection is activated.

3. Calculating Internal Power Loss

The average internal power loss in each excitation mode of the STK672-642A-E can be calculated from the following formulas.

Each excitation mode
2-phase excitation mode
$2PdAVex=(Vsat+Vdf) \times 0.5 \times CLOCK \times I_{OH} \times t2+0.5 \times CLOCK \times I_{OH} \times (Vsat \times t1+Vdf \times t3)$

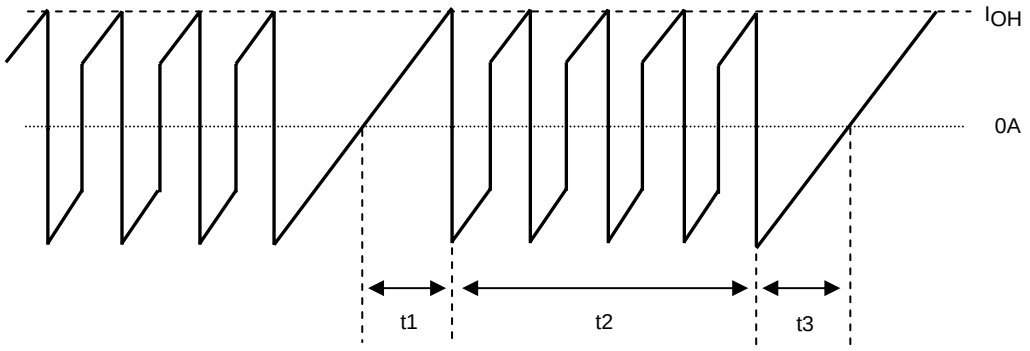
1-2 Phase excitation mode
$1\text{-}2PdAVex=(Vsat+Vdf) \times 0.25 \times CLOCK \times I_{OH} \times t2+0.25 \times CLOCK \times I_{OH} \times (Vsat \times t1+Vdf \times t3)$

Motor hold mode
$HoldPdAVex= (Vsat+Vdf) \times I_{OH}$

Vsat: Combined voltage represented by the Ron voltage drop+shunt resistor
Vdf: Combined voltage represented by the MOSFET body diode+shunt resistor
CLOCK: Input CLOCK (CLOCK pin signal frequency)

t1, t2, and t3 represent the waveforms shown in the figure below.

t1: Time required for the winding current to reach the set current (I_{OH})
t2: Time in the constant current control (PWM) region
t3: Time from end of phase input signal until inverse current regeneration is complete



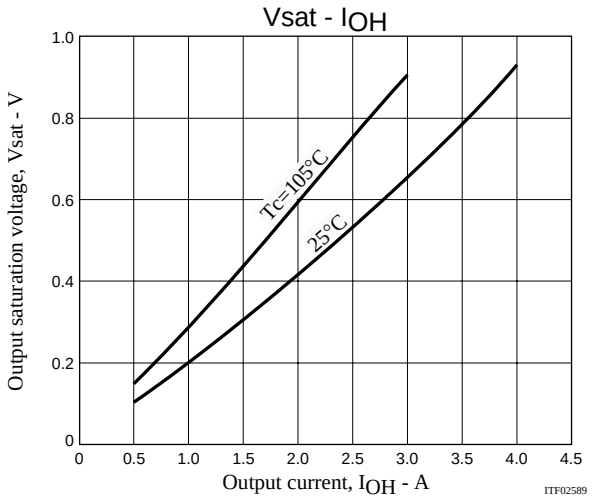
Motor COM Current Waveform Model

$t1= (-L/(R+0.20)) \text{ In } (1-((R+0.20)/V_{CC}) \times I_{OH})$
$t3= (-L/R) \text{ In } ((V_{CC}+0.20)/(I_{OH} \times R+V_{CC}+0.20))$
V_{CC}: Motor supply voltage (V)
L: Motor inductance (H)
R: Motor winding resistance (Ω)
I_{OH}: Motor set output current crest value (A)

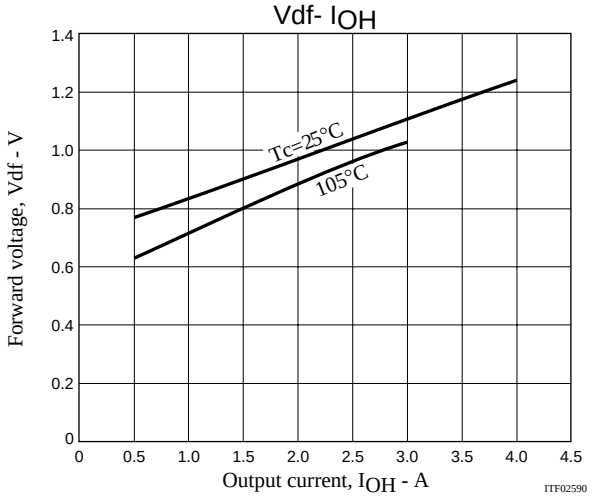
Relationship of CLOCK, t1, t2, and t3 in each excitation mode
2-phase excitation mode: t2= (2/CLOCK) - (t1+t3)
1-2 phase excitation mode: t2= (3/CLOCK) -t1

For Vsat and Vdf, be sure to substitute values from the graphs of Vsat vs. I_{OH} and Vdf vs. I_{OH} while the set current value is I_{OH}.
Then, determine whether a heat sink is required by comparing with the graph of ΔTc vs. Pd based on the average HIC power loss calculated.
When designing a heat sink, refer to the section “Thermal design” found on the next page. The average HIC power loss, PdAV, described above does not have the avalanche’s loss. To include the avalanche’s loss, be sure to add Equation (2), “STK672-6** Allowable Avalanche Energy Value” to PdAV above. When using this IC without a fin always check for temperature increases in the set, because the HIC substrate temperature, Tc, varies due to effects of convection around the HIC.

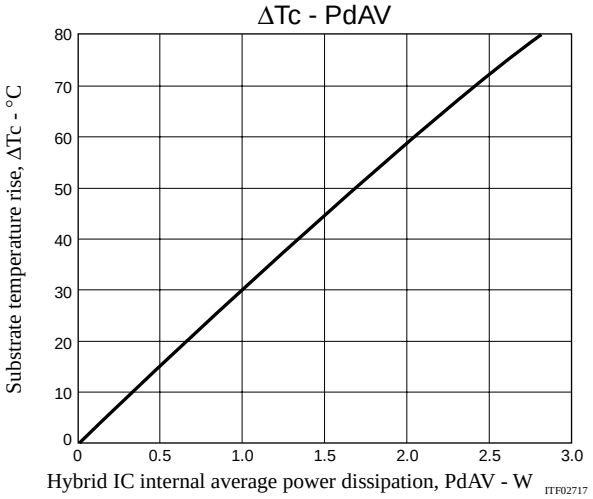
Output saturation voltage, Vsat - Output current, I_{OH}



Forward voltage, Vdf -Output current, I_{OH}



Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV



4. Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-6** Series hybrid IC, the waveforms shown in Figure 1 below result for the output current, I_D, and voltage, V_{DS}.

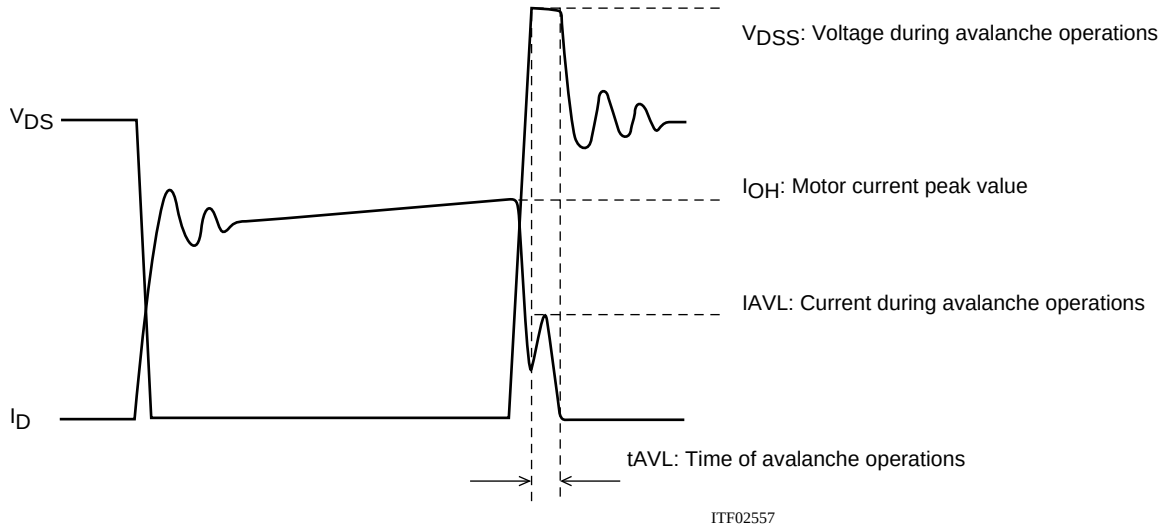


Figure 1 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-6** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-6** Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (1).

$$EAVL1=V_{DSS}\times IAVL\times 0.5\times tAVL \quad \text{---------- (1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-6** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (1).

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \quad \text{---------- (2)}$$

fc: Hz units (fc is set to the PWM frequency of 50kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-6** Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=1A, tAVL=0.2µs when using a STK672-642A-E driver, the result is:

$PAVL=110\times 1\times 0.5\times 0.2\times 10^{-6}\times 50\times 10^{3}=0.55W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (2) falls within the allowable range for avalanche operations.

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.
- Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

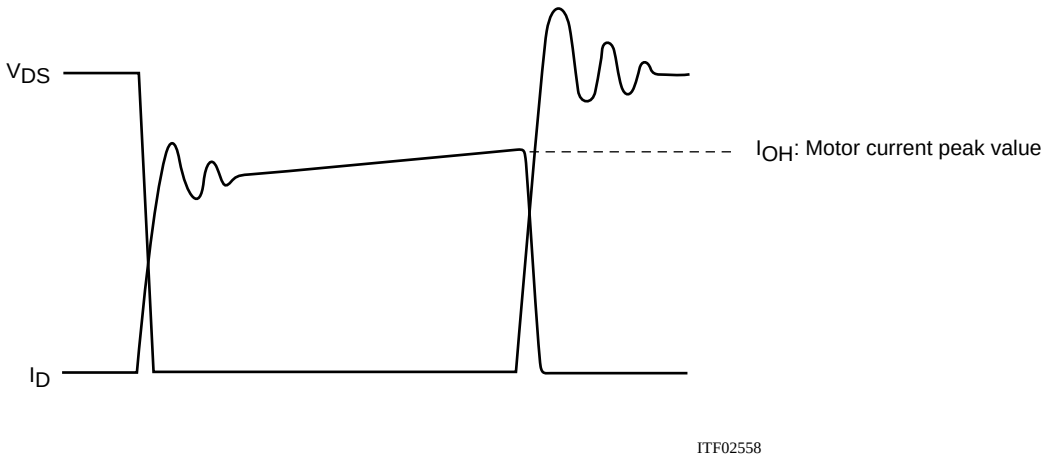
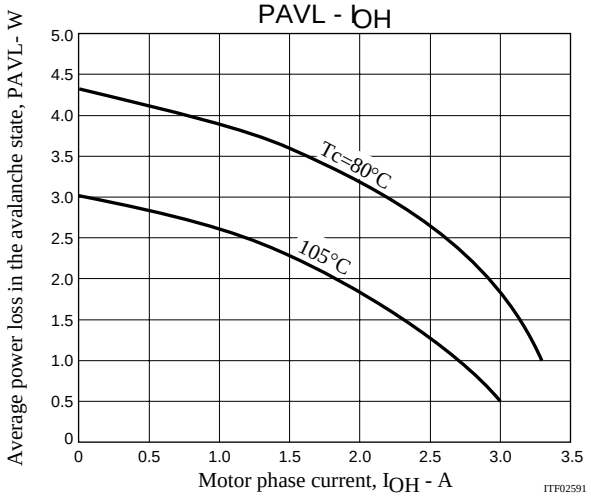


Figure 2 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-6** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 3 Allowable Loss Range, PAVL-I_{OH} During Avalanche Operations



Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 3W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

5. Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to “Calculating Internal HIC Loss for the STK672-642A-E”.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

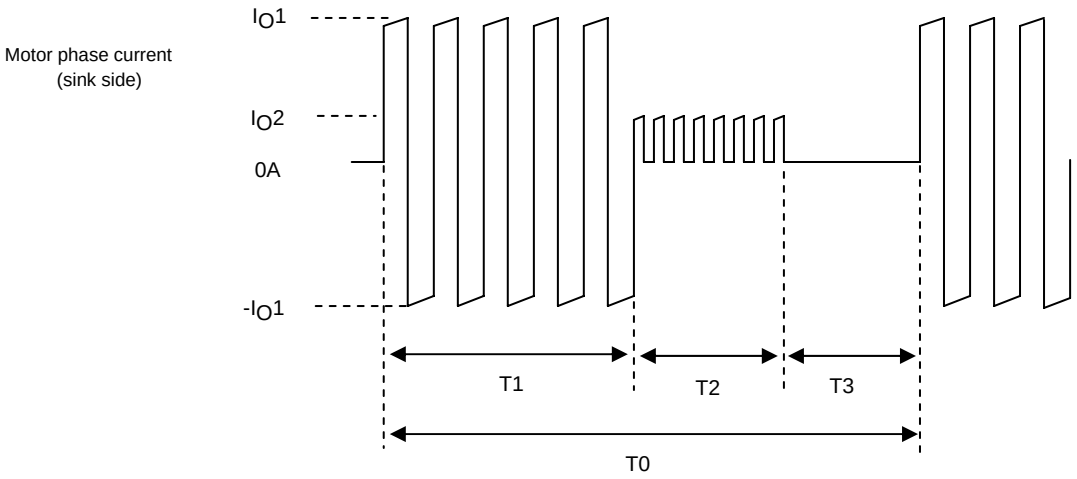


Figure 1 Motor Current Timing

T1: Motor rotation operation time

T2: Motor hold operation time

T3: Motor current off time

T2 may be reduced, depending on the application.

T0: Single repeated motor operating cycle

I_O1 and I_O2: Motor current peak values

Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.

Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

PdAV= (T1×P1+T2×P2+T3×0) ÷TO ---------- (I)

(Here, P1 is the PdAV for I_O1 and P2 is the PdAV for I_O2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

θc-a= (Tc max-Ta) ÷PdAV ---------- (II)

Tc max: Maximum operating substrate temperature =105°C

Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (2), “Allowable STK672-6** Avalanche Energy Value”, to PdAV.

Figure 2 Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV

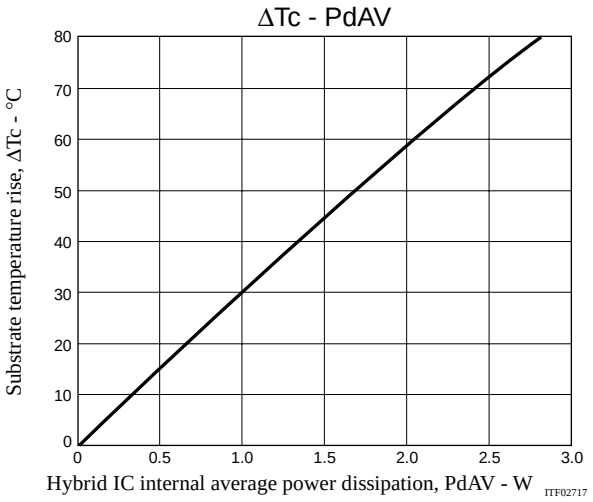
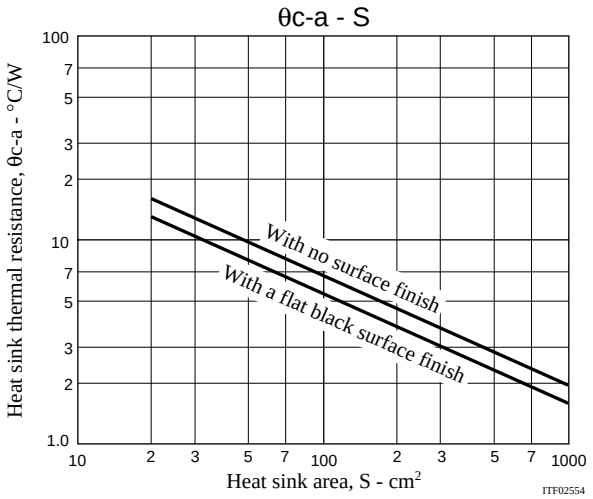


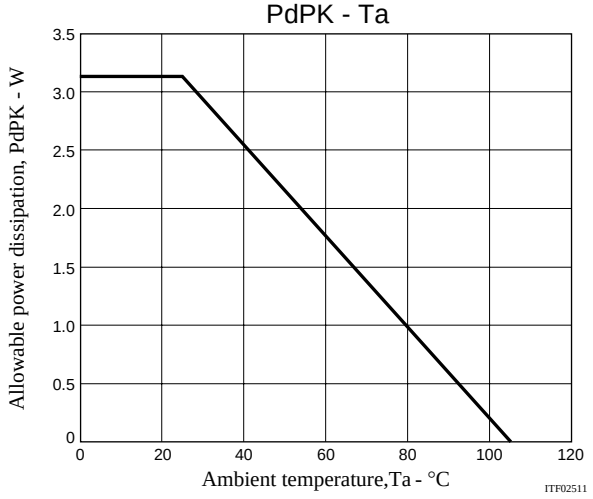
Figure 3 Heat sink area (Board thickness: 2mm) - θc-a



6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink. The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta. Power loss of up to 2.8W is allowable at Ta=25°C, and of up to 1.5W at Ta=60°C.

Allowable power dissipation, PdPK(no heat sink) - Ambient temperature, Ta



7. Example of Stepping Motor Driver Output Current Path (1-2 phase excitation)