

74HCT245

Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The 74HCT245 is identical in pinout to LS245. The device has TTL-Compatible Inputs.

The HCT245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

Features

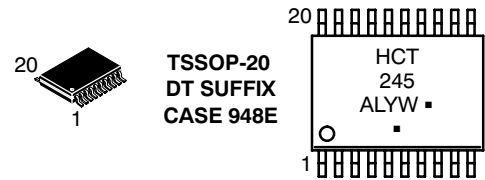
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 308 FETs or 77 Equivalent Gates
- This is a Pb-Free Device



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MARKING DIAGRAMS



HCT245 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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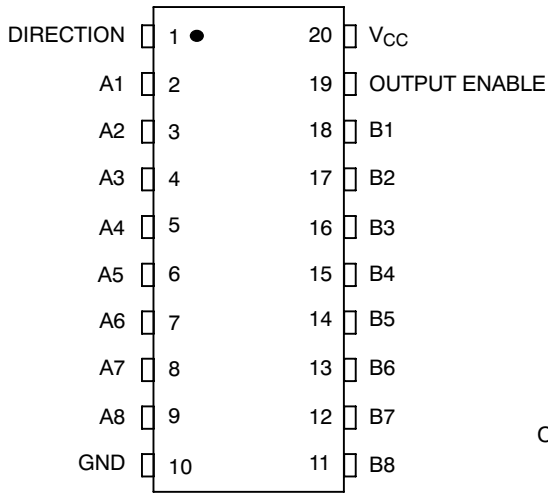


Figure 1. Pin Assignment

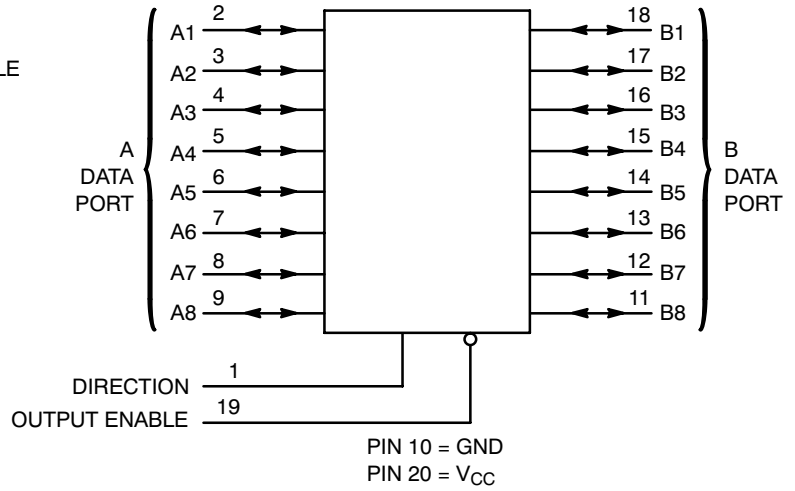


Figure 2. Logic Diagram

FUNCTION TABLE

| Control Inputs | | Operation |
|----------------|-----------|---------------------------------------|
| Output Enable | Direction | |
| L | L | Data Transmitted from Bus B to Bus A |
| L | H | Data Transmitted from Bus A to Bus B |
| H | X | Buses Isolated (High-Impedance State) |

X = don't care

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|-----------|-----------------------|
| 74HCT245DTR2G | TSSOP-20* | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit |
|----------------------|---|-------------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _{OUT} | DC Output Voltage (Note 2) | -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | ±20 | mA |
| I _{OK} | DC Output Diode Current | ±35 | mA |
| I _{OUT} | DC Output Sink Current | ±35 | mA |
| I _{CC} | DC Supply Current per Supply Pin | ±75 | mA |
| I _{GND} | DC Ground Current per Ground Pin | ±75 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | +150 | °C |
| θ _{JA} | Thermal Resistance TSSOP | 128 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C TSSOP | 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating Oxygen Index: 30% to 35% | UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) | > 2000 > 200 | V |
| I _{LATCHUP} | Latchup Performance Above V _{CC} and Below GND at 85°C (Note 5) | ±300 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|---|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 3) V _{CC} = 4.5 V | 0 | 500 | ns |

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} (V) | Guaranteed Limit | | | Unit |
|------------------|--|---|---------------------|------------------|-------------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1V I _{out} ≤ 20μA | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = V _{CC} - 0.1V I _{out} ≤ 20μA | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20μA | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20μA | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 4.5 | 0.26 | 0.33 | 0.40 | μA |
| | | | 5.5 | 0.26 | 0.33 | 0.40 | |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 5.5 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0μA | 5.5 | 4.0 | 40 | 40 | μA |
| ΔI _{CC} | Additional Quiescent Supply Current | V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0μA | 5.5 | ≥ -55°C | 25 to 125°C | | mA |
| | | | | 2.9 | 2.4 | | |

6. Information on typical parametric values can be found in Chapter 2the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

7. Total Supply Current = I_{CC} + ΣΔI_{CC}.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|-------------------|------------------|--------|---------|------|
| | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to B, B to A (Figures 1 and 3) | 4.5 | 15 | 19 | 22 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4) | 4.5 | 22 | 28 | 33 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4) | 4.5 | 22 | 28 | 33 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 4.5 | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance (Pin 1 or Pin 19) | - | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State I/O Capacitance (I/O in High-Impedance State) | - | 15 | 15 | 15 | pF |

8. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Transceiver Channel) (Note 9) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|--|---|--|----|
| | | 40 | | |
| | | | | |

9. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

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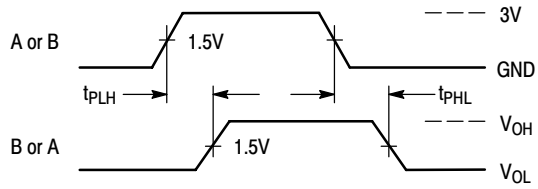


Figure 3. Switching Waveform

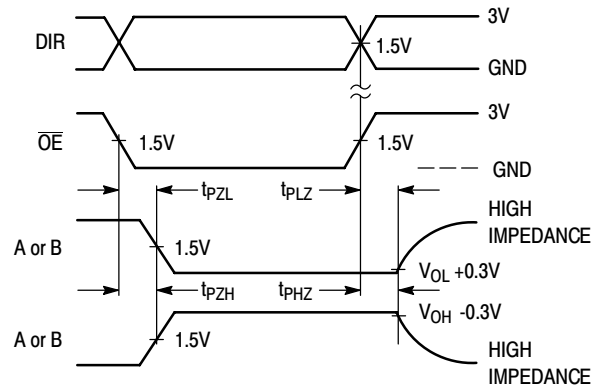
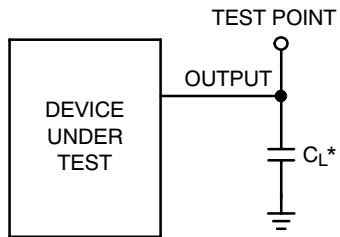
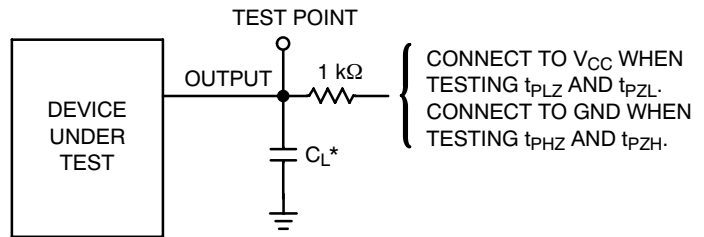


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

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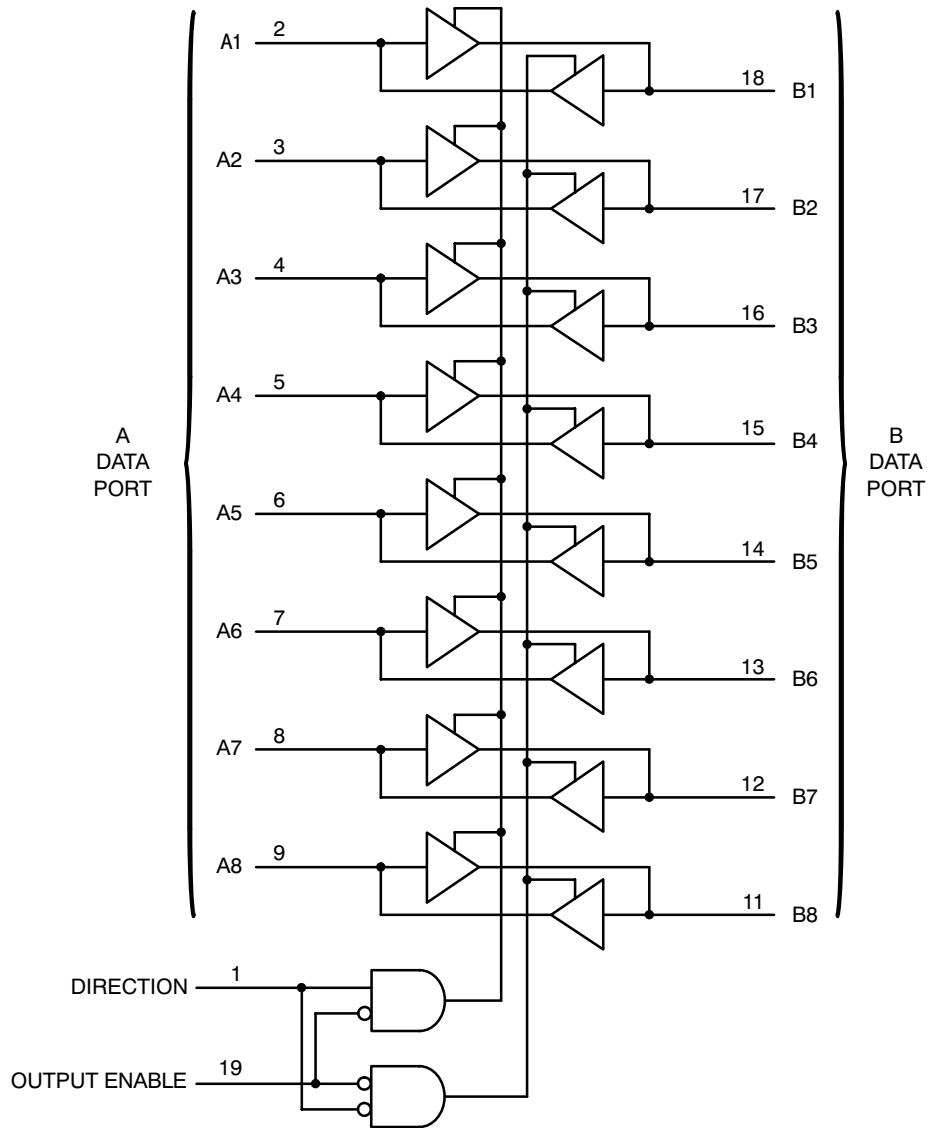
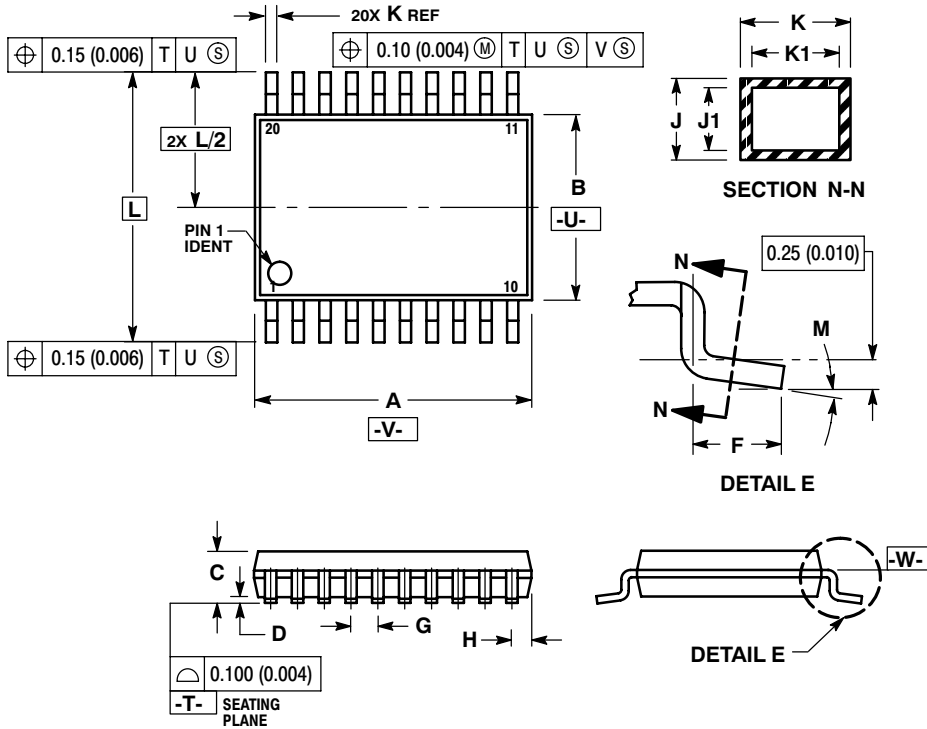


Figure 7. Expanded Logic Diagram

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PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

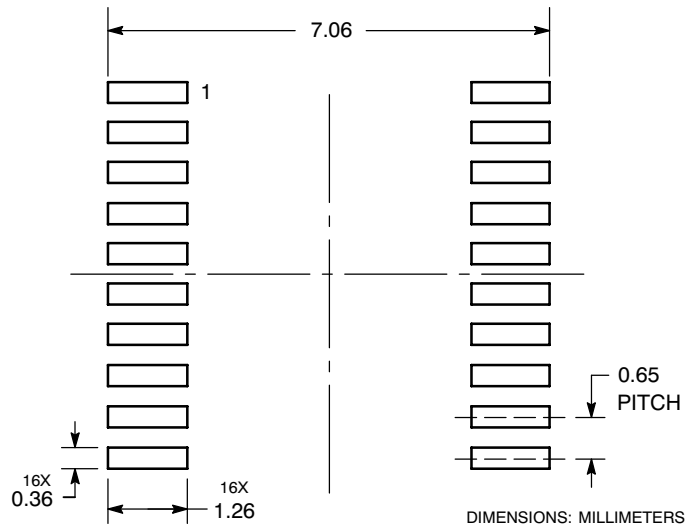


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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