# DDR SDRAM Small-Outline DIMM

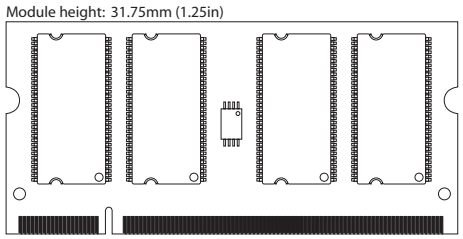
## MT5VDDT1672H – 128MB
## MT5VDDT3272H – 256MB

For component data sheets, refer to Micron's Web site: www.micron.com

## Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC-2100, PC-2700, or PC-3200
- 128MB[2] (16 Meg x 72) and 256MB (32 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD}$ = $V_{DD}Q$ = +2.5V
- $V_{DDSPD}$ = +2.3V to +3.6V
- JEDEC-standard 2.5V I/O (SSTL_2-compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data (source-synchronous data capture)
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable READ CAS latency for maximum compatibility
- Gold edge contacts

**Figure 1: 200-Pin SODIMM (MO-224 R/C C)**




| Options | Marking |
|---|---|
| • Operating temperature[1] | |
| – Commercial (0°C ≤ $T_A$ ≤ +70°C) | None |
| – Industrial (–40°C ≤ $T_A$ ≤ +85°C) | I |
| • Package | |
| – 200-pin SODIMM (standard)[2] | G |
| – 200-pin SODIMM (Pb-free) | Y |
| • Memory clock, frequency, CAS latency | |
| – 5ns (200 MHz), 400 MT/s, CL = 3 | -40B[3] |
| – 6ns (167 MHz), 333 MT/s, CL = 2.5 | -335 |
| – 7.5ns (133 MHz), 266 MT/s, CL = 2 | -262 |
| – 7.5ns (133 MHz), 266 MT/s, CL = 2 | -26A |
| – 7.5ns (133 MHz), 266 MT/s, CL = 2.5 | -265 |
| • PCB height | |
| – 31.75mm (1.25in) | |

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Consult factory for product availability.
3. -40B only available for 256MB modules.

**Table 1: Key Timing Parameters**

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | $^tRCD$ (ns) | $^tRP$ (ns) | $^tRC$ (ns) |
|---|---|---|---|---|---|---|---|
| | | CL = 3 | CL = 2.5 | CL = 2 | | | |
| -40B | PC-3200 | 400 | 333 | 266 | 15 | 15 | 55 |
| -335 | PC-2700 | – | 333 | 266 | 15 | 15 | 60 |
| -262 | PC-2100 | – | 266 | 266 | 15 | 15 | 60 |
| -26A | PC-2100 | – | 266 | 266 | 20 | 20 | 65 |
| -265 | PC-2100 | – | 266 | 200 | 20 | 20 | 65 |

**Table 2: Addressing**

| | 128MB | 256MB |
|---|---|---|
| Refresh count | 8K | 8K |
| Row addressing | 8K (A0–A12) | 8K (A0–A12) |
| Device bank addressing | 4 (BA0, BA1) | 4 (BA0, BA1) |
| Device configuration | 256Mb (16 Meg x 16) | 512Mb (32 Meg x 16) |
| Column addressing | 512 (A0–A8) | 1K (A0–A9) |
| Module rank addressing | 1 (SO#) | 1 (SO#) |

**Table 3: Part Numbers and Timing Parameters – 128MB**

Base device: MT46V16M16[1], 256Mb DDR SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT5VDDT1672H(I)G-335__ | 128MB | 16 Meg x 72 | 2.7 GB/s | 6ns/333 MT/s | 2.5-3-3 |
| MT5VDDT1672H(I)Y-335__ | 128MB | 16 Meg x 72 | 2.7 GB/s | 6ns/333 MT/s | 2.5-3-3 |
| MT5VDDT1672H(I)G-262__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT5VDDT1672H(I)Y-262__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT5VDDT1672H(I)G-26A__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT5VDDT1672H(I)Y-26A__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT5VDDT1672H(I)G-265__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |
| MT5VDDT1672H(I)Y-265__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

**Table 4: Part Numbers and Timing Parameters – 256MB**

Base device: MT46V32M16[1], 512Mb DDR SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT5VDDT3272H(I)G-40B__ | 256MB | 32 Meg x 72 | 3.2 GB/s | 5ns/400 MT/s | 3-3-3 |
| MT5VDDT3272H(I)Y-40B__ | 256MB | 32 Meg x 72 | 3.2 GB/s | 5ns/400 MT/s | 3-3-3 |
| MT5VDDT3272H(I)G-335__ | 256MB | 32 Meg x 72 | 2.7 GB/s | 6ns/333 MT/s | 2.5-3-3 |
| MT5VDDT3272H(I)Y-335__ | 256MB | 32 Meg x 72 | 2.7 GB/s | 6ns/333 MT/s | 2.5-3-3 |

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT5VDDT1672HG-335F3.

# Pin Assignments and Descriptions

**Table 5: Pin Assignments**

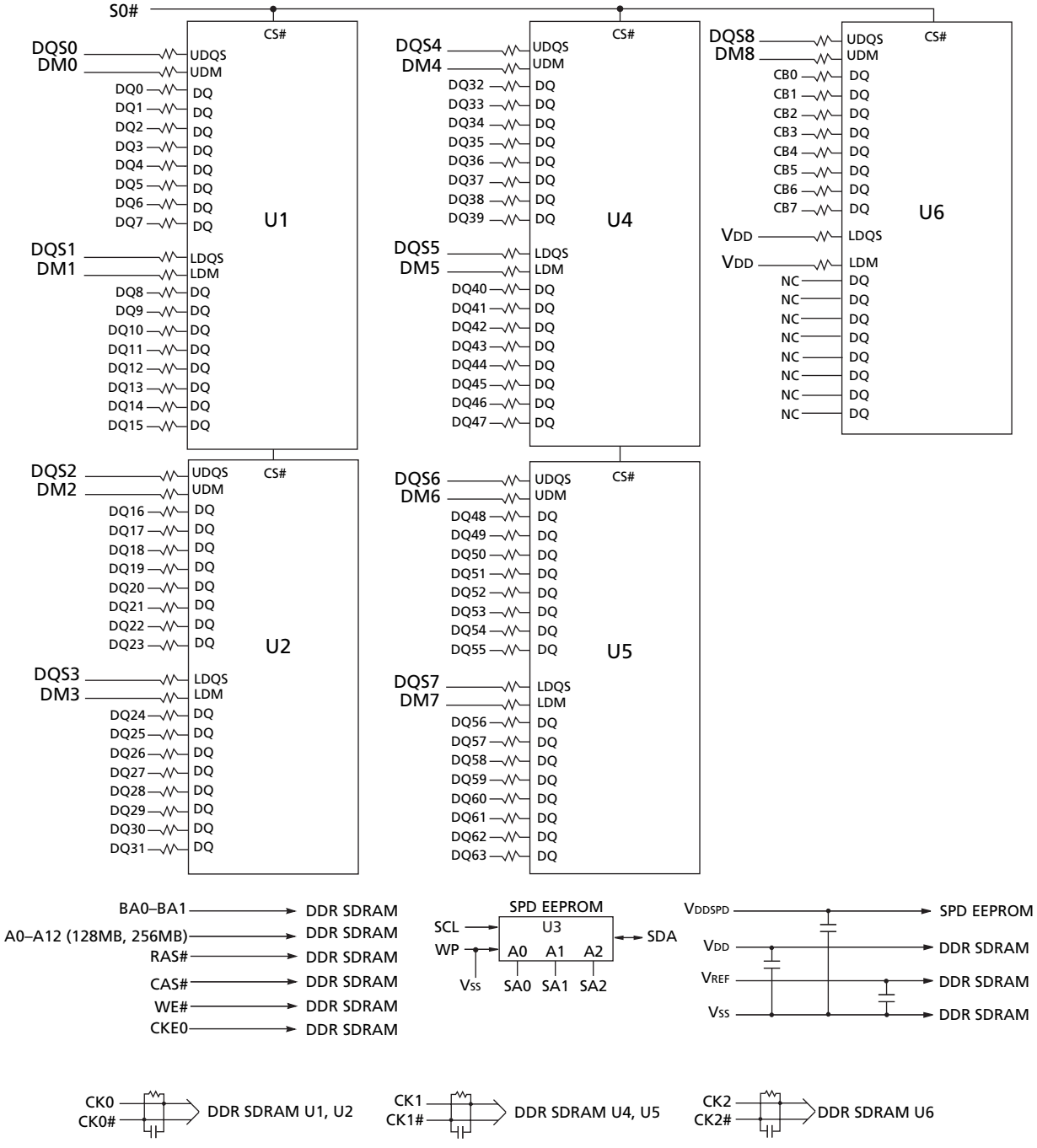
| 200-Pin SODIMM Front | | | | | | | | 200-Pin SODIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VREF | 51 | VSS | 101 | A9 | 151 | DQ42 | 2 | VREF | 52 | VSS | 102 | A8 | 152 | DQ46 |
| 3 | VSS | 53 | DQ19 | 103 | VSS | 153 | DQ43 | 4 | VSS | 54 | DQ23 | 104 | VSS | 154 | DQ47 |
| 5 | DQ0 | 55 | DQ24 | 105 | A7 | 155 | VDD | 6 | DQ4 | 56 | DQ28 | 106 | A6 | 156 | VDD |
| 7 | DQ1 | 57 | VDD | 107 | A5 | 157 | VDD | 8 | DQ5 | 58 | VDD | 108 | A4 | 158 | CK1# |
| 9 | VDD | 59 | DQ25 | 109 | A3 | 159 | VSS | 10 | VDD | 60 | DQ29 | 110 | A2 | 160 | CK1 |
| 11 | DQS0 | 61 | DQS3 | 111 | A1 | 161 | VSS | 12 | DM0 | 62 | DM3 | 112 | A0 | 162 | VSS |
| 13 | DQ2 | 63 | VSS | 113 | VDD | 163 | DQ48 | 14 | DQ6 | 64 | VSS | 114 | VDD | 164 | DQ52 |
| 15 | VSS | 65 | DQ26 | 115 | A10 | 165 | DQ49 | 16 | VSS | 66 | DQ30 | 116 | BA1 | 166 | DQ53 |
| 17 | DQ3 | 67 | DQ27 | 117 | BA0 | 167 | VDD | 18 | DQ7 | 68 | DQ31 | 118 | RAS# | 168 | VDD |
| 19 | DQ8 | 69 | VDD | 119 | WE# | 169 | DQS6 | 20 | DQ12 | 70 | VDD | 120 | CAS# | 170 | DM6 |
| 21 | VDD | 71 | CB0 | 121 | S0# | 171 | DQ50 | 22 | VDD | 72 | CB4 | 122 | NC | 172 | DQ54 |
| 23 | DQ9 | 73 | CB1 | 123 | NC | 173 | VSS | 24 | DQ13 | 74 | CB5 | 124 | NC | 174 | VSS |
| 25 | DQS1 | 75 | VSS | 125 | VSS | 175 | DQ51 | 26 | DM1 | 76 | VSS | 126 | VSS | 176 | DQ55 |
| 27 | VSS | 77 | DQS8 | 127 | DQ32 | 177 | DQ56 | 28 | VSS | 78 | DM8 | 128 | DQ36 | 178 | DQ60 |
| 29 | DQ10 | 79 | CB2 | 129 | DQ33 | 179 | VDD | 30 | DQ14 | 80 | CB6 | 130 | DQ37 | 180 | VDD |
| 31 | DQ11 | 81 | VDD | 131 | VDD | 181 | DQ57 | 32 | DQ15 | 82 | VDD | 132 | VDD | 182 | DQ61 |
| 33 | VDD | 83 | CB3 | 133 | DQS4 | 183 | DQS7 | 34 | VDD | 84 | CB7 | 134 | DM4 | 184 | DM7 |
| 35 | CK0 | 85 | NC | 135 | DQ34 | 185 | VSS | 36 | VDD | 86 | NC | 136 | DQ38 | 186 | VSS |
| 37 | CK0# | 87 | VSS | 137 | VSS | 187 | DQ58 | 38 | VSS | 88 | VSS | 138 | VSS | 188 | DQ62 |
| 39 | VSS | 89 | CK2 | 139 | DQ35 | 189 | DQ59 | 40 | VSS | 90 | VSS | 140 | DQ39 | 190 | DQ63 |
| 41 | DQ16 | 91 | CK2# | 141 | DQ40 | 191 | VDD | 42 | DQ20 | 92 | VDD | 142 | DQ44 | 192 | VDD |
| 43 | DQ17 | 93 | VDD | 143 | VDD | 193 | SDA | 44 | DQ21 | 94 | VDD | 144 | VDD | 194 | SA0 |
| 45 | VDD | 95 | NC | 145 | DQ41 | 195 | SCL | 46 | VDD | 96 | CKE0 | 146 | DQ45 | 196 | SA1 |
| 47 | DQS2 | 97 | NC | 147 | DQS5 | 197 | VDDSPD | 48 | DM2 | 98 | NC | 148 | DM5 | 198 | SA2 |
| 49 | DQ18 | 99 | A12 | 149 | VSS | 199 | NC | 50 | DQ22 | 100 | A11 | 150 | VSS | 200 | NC |

**Table 6: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| WE#, CAS#, RAS# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| CK0, CK0#, CK1, CK1#, CK2, CK2# | Input | **Clocks:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#. |
| CKE0 | Input | **Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. |
| S0# | Input | **Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code. |
| BA0, BA1 | Input | **Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| A0–A12 | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| DM0–DM8 | Input | **Data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. |
| SDA | Input/ Output | **Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| SCL | Input | **Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module. |
| SA0–SA2 | Input | **Presence-detect address inputs:** These pins are used to configure the presence-detect device. |
| DQS0–DQS8 | Input/ Output | **Data strobe:** Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data. |
| CB0–CB7 | Input/ Output | Check bits. |
| DQ0–DQ63 | Input/ Output | **Data input/output:** Data bus. |
| $V_{REF}$ | Supply | SSTL_2 reference voltage. |
| $V_{DD}$ | Supply | **Power supply:** +2.5V ±0.2V. (-40B speed grade requires 2.6V ±0.1V) |
| $V_{SS}$ | Supply | Ground. |
| $V_{DDSPD}$ | Supply | **Serial EEPROM positive power supply:** +2.3V to +3.6V. |
| NC | – | **No connect:** These pins should be left unconnected. |

# Functional Block Diagram

**Figure 2: Functional Block Diagram**



# General Description

The MT5VDDT1672H and MT5VDDT3272H are high-speed CMOS, dynamic random-access, 128MB and 256MB memory modules organized in a x72 (ECC) configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clocks (CK, CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect (SPD) Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard $I^2C$ bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to $V_{SS}$ on the module, permanently disabling hardware write protect.

# Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 7: Absolute Maximum Ratings**

| Symbol | Parameter/Condition | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | | 2.3 | 2.7 | V |
| $V_{REF}$ | I/O reference voltage | | 0.49 × $V_{DD}Q$ | 0.51 × $V_{DD}Q$ | V |
| $V_{TT}$ | I/O termination voltage (system) | | $V_{REF}$ - 0.04 | $V_{REF}$ + 0.04 | V |
| $V_{IH}$(DC) | Input high (logic 1) voltage | | $V_{REF}$ + 0.15 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$(DC) | Input low (logic 0) voltage | | –0.3 | $V_{REF}$ - 0.15 | V |
| $I_I$ | Input leakage current; Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$; $V_{REF}$ pin 0V ≤ $V_{IN}$ ≤ 1.35V (All other pins not under test = 0V) | Command/address, RAS#, CAS#, WE#, CKE, S#, BA | –10 | 10 | µA |
| | | CK0, CK0#, CK1, CK1# | –4 | 4 | |
| | | DM, CK2, CK2# | –2 | 2 | |
| $I_{OZ}$ | Output leakage current (DQ pins are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}Q$) | DQ, DQS | –5 | 5 | µA |
| $I_{OH}$ | Output levels | | –16.8 | – | mA |
| $I_{OL}$ | High current ($V_{OUT}$ = $V_{DD}Q$ - 0.373V, MIN $V_{REF}$, MIN $V_{TT}$)<br>Low current ($V_{OUT}$ = 0.373V, MAX $V_{REF}$, MAX $V_{TT}$) | | 16.8 | – | mA |
| $I_{OH}$ | Output levels (reduced drive option) | | –9 | – | mA |
| $I_{OL}$ | High current ($V_{OUT}$ = $V_{DD}Q$ - 0.373V, MIN $V_{REF}$, MIN $V_{TT}$)<br>Low current ($V_{OUT}$ = 0.373V, MAX $V_{REF}$, MAX $V_{TT}$) | | 9 | – | mA |
| $T_A$ | Module ambient operating temperature | Commercial | 0 | +70 | °C |
| | | Industrial | –40 | +85 | |

## Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

## Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

**Table 8: Module and Component Speed Grades**

| Module Speed Grade | Component Speed Grade |
|---|---|
| -40B | -5B |
| -335 | -6 |
| -262 | -75E |
| -26A | -75Z |
| -265 | -75 |

## IDD Specifications

**Table 9: DDR IDD Specifications and Conditions – 128MB**

Values shown for MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

| Parameter/Condition | | Symbol | -335 | -262 | -26A/ -265 | Units |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | IDD0 | 625 | 625 | 525 | mA |
| **Operating one bank active-read-precharge current:** Burst = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle | | IDD1 | 900 | 850 | 775 | mA |
| **Precharge power-down standby current:** All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = (LOW) | | IDD2P | 20 | 20 | 20 | mA |
| **Idle standby current:** CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | | IDD2F | 250 | 225 | 225 | mA |
| **Active power-down standby current:** One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD3P | 150 | 125 | 125 | mA |
| **Active standby current:** CS# = HIGH; CKE = HIGH; One device bank; Active-precharge; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | 300 | 250 | 250 | mA |
| **Operating current:** Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA | | IDD4R | 1,100 | 925 | 925 | mA |
| **Operating current:** Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | IDD4W | 900 | 725 | 725 | mA |
| **Auto refresh current** | $^{t}REFC = {}^{t}RFC$ (MIN) | IDD5 | 1,275 | 1,175 | 1,175 | mA |
| | $^{t}REFC$ = 7.8125µs | IDD5A | 30 | 30 | 30 | mA |
| **Self refresh current:** CKE ≤ 0.2V | | IDD6 | 20 | 20 | 20 | mA |
| **Operating current:** Four device bank interleaving READs (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands | | IDD7 | 2,200 | 1,900 | 1,900 | mA |

**Table 10: DDR IDD Specifications and Conditions – 256MB**

Values shown for MT46V32M16 DDR SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

| Parameter/Condition | | Symbol | -40B | -335 | Units |
|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^{t}$RC = $^{t}$RC (MIN); $^{t}$CK = $^{t}$CK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | IDD0 | 775 | 650 | mA |
| **Operating one bank active-read-precharge current:** Burst = 4; $^{t}$RC = $^{t}$RC (MIN); $^{t}$CK = $^{t}$CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle | | IDD1 | 925 | 800 | mA |
| **Precharge power-down standby current:** All device banks idle; Power-down mode; $^{t}$CK = $^{t}$CK (MIN); CKE = (LOW) | | IDD2P | 25 | 25 | mA |
| **Idle standby current:** CS# = HIGH; All device banks idle; $^{t}$CK = $^{t}$CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | | IDD2F | 275 | 225 | mA |
| **Active power-down standby current:** One device bank active; Power-down mode; $^{t}$CK = $^{t}$CK (MIN); CKE = LOW | | IDD3P | 225 | 175 | mA |
| **Active standby current:** CS# = HIGH; CKE = HIGH; One device bank; Active-precharge; $^{t}$RC = $^{t}$RAS (MAX); $^{t}$CK = $^{t}$CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | 300 | 250 | mA |
| **Operating current:** Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^{t}$CK = $^{t}$CK (MIN); IOUT = 0mA | | IDD4R | 950 | 825 | mA |
| **Operating current:** Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^{t}$CK = $^{t}$CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | IDD4W | 975 | 775 | mA |
| **Auto refresh current** | $^{t}$REFC = $^{t}$RFC (MIN) | IDD5 | 1,725 | 1,450 | mA |
| | $^{t}$REFC = 7.8125µs | IDD5A | 55 | 50 | mA |
| **Self refresh current:** CKE ≤ 0.2V | | IDD6 | 25 | 25 | mA |
| **Operating current:** Four device bank interleaving READs (BL = 4) with auto precharge; $^{t}$RC = $^{t}$RC (MIN); $^{t}$CK = $^{t}$CK (MIN); Address and control inputs change only during active READ or WRITE commands | | IDD7 | 2,250 | 2,025 | mA |

# Serial Presence-Detect

**Table 11: Serial Presence-Detect EEPROM DC Operating Conditions**
All voltages referenced to $V_{SS}$; $V_{DDSPD}$ = +2.3V to +3.6V

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 2.3 | 3.6 | V |
| Input high voltage: Logic 1; All inputs | $V_{IH}$ | $V_{DDSPD} \times 0.7$ | $V_{DDSPD}$ + 0.5 | V |
| Input low voltage: Logic 0; All inputs | $V_{IL}$ | –1 | $V_{DDSPD} \times 0.3$ | V |
| Output low voltage: $I_{OUT}$ = 3mA | $V_{OL}$ | – | 0.4 | V |
| Input leakage current: $V_{IN}$ = GND to $V_{DD}$ | $I_{LI}$ | – | 10 | µA |
| Output leakage current: $V_{OUT}$ = GND to $V_{DD}$ | $I_{LO}$ | – | 10 | µA |
| Standby current: SCL = SDA = $V_{DD}$ - 0.3V; All other inputs = $V_{SS}$ or $V_{DD}$ | $I_{SB}$ | – | 30 | µA |
| Power supply current: SCL clock frequency = 100 kHz | $I_{CC}$ | – | 2 | mA |

**Table 12: Serial Presence-Detect EEPROM AC Operating Conditions**
All voltages referenced to $V_{SS}$; $V_{DDSPD}$ = +2.3V to +3.6V

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| SCL LOW to SDA data-out valid | $^{t}AA$ | 0.2 | 0.9 | µs | 1 |
| Time the bus must be free before a new transition can start | $^{t}BUF$ | 1.3 | – | µs | |
| Data-out hold time | $^{t}DH$ | 200 | – | ns | |
| SDA and SCL fall time | $^{t}F$ | – | 300 | ns | 2 |
| Data-in hold time | $^{t}HD:DAT$ | 0 | – | µs | |
| Start condition hold time | $^{t}HD:STA$ | 0.6 | – | µs | |
| Clock HIGH period | $^{t}HIGH$ | 0.6 | – | µs | |
| Noise suppression time constant at SCL, SDA inputs | $^{t}I$ | – | 50 | ns | |
| Clock LOW period | $^{t}LOW$ | 1.3 | – | µs | |
| SDA and SCL rise time | $^{t}R$ | – | 0.3 | µs | 2 |
| SCL clock frequency | $^{f}SCL$ | – | 400 | kHz | |
| Data-in setup time | $^{t}SU:DAT$ | 100 | – | ns | |
| Start condition setup time | $^{t}SU:STA$ | 0.6 | – | µs | 3 |
| Stop condition setup time | $^{t}SU:STO$ | 0.6 | – | µs | |
| WRITE cycle time | $^{t}WRC$ | – | 10 | ms | 4 |

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time ($^{t}WRC$) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

**Table 13: Serial Presence-Detect Matrix (-335, -26A, and -265 Speed Grades)**

| Byte | Description | Entry (Version) | 128MB | 256MB |
|---|---|---|---|---|
| 0 | Number of SPD bytes used by Micron | 128 | 80 | 80 |
| 1 | Total number of bytes in SPD device | 256 | 08 | 08 |
| 2 | Fundamental memory type | DDR SDRAM | 07 | 07 |
| 3 | Number of row addresses on assembly | 12,13 | 0D | 0D |
| 4 | Number of column addresses on assembly | 9, 10 | 09 | 0A |
| 5 | Number of physical ranks on DIMM | 1 | 01 | 01 |
| 6 | Module data width | 72 | 48 | 48 |
| 7 | Module data width (continued) | 0 | 00 | 00 |
| 8 | Module voltage interface levels | SSTL 2.5V | 04 | 04 |
| 9 | SDRAM cycle time, $^{t}$CK, CL = 2.5 | 6ns (-335)<br>7ns (-262/-26A)<br>7.5ns (-265) | 60<br>70<br>75 | 60<br>70<br>75 |
| 10 | SDRAM access from clock, $^{t}$AC, CL = 2.5 | 0.7ns (-335)<br>0.75ns (-262/-26A/ -265) | 70<br>75 | 70<br>75 |
| 11 | Module configuration type | ECC | 02 | 02 |
| 12 | Refresh rate/type | 15.62µs, 7.8µs/SELF | 82 | 82 |
| 13 | SDRAM device width (primary DDR SDRAM) | 16 | 10 | 10 |
| 14 | Error-checking DDR SDRAM data width | 16 | 10 | 10 |
| 15 | MIN clock delay, back-to-back random column access | 1 clock | 01 | 01 |
| 16 | Burst lengths supported | 2, 4, 8 | 0E | 0E |
| 17 | Number of banks on DDR SDRAM device | 4 | 04 | 04 |
| 18 | CAS latencies supported | 2.5, 2 | 0C | 0C |
| 19 | CS latency | 0 | 01 | 01 |
| 20 | WE latency | 1 | 02 | 02 |
| 21 | SDRAM module attributes | Unbuffered/diff. clock | 20 | 20 |
| 22 | SDRAM device attributes: general | Fast/concurrent AP | C1 | C1 |
| 23 | SDRAM cycle time, $^{t}$CK, CL = 2 | 7.5ns (-335/-262/-26A)<br>10ns (-265) | 75<br>A0 | 75<br>A0 |
| 24 | SDRAM access from clock, $^{t}$AC, CL = 2 | 0.7ns (-335)<br>0.75ns (-262/-26A/ -265) | 70<br>75 | 70<br>75 |
| 25 | SDRAM cycle time, $^{t}$CK, CL = 1.5 | | 00 | 00 |
| 26 | SDRAM access from CK, $^{t}$AC, CL = 1.5 | | 00 | 00 |
| 27 | MIN row precharge time, $^{t}$RP[4] | 18ns (-335)<br>15ns (-262)<br>20ns (-26A/-265) | 48<br>3C<br>50 | 48<br>3C<br>50 |
| 28 | MIN row active-to-row active, $^{t}$RRD | 12ns (-335)<br>15ns (-262/-26A/-265) | 30<br>3C | 30<br>3C |
| 29 | MIN RAS#-to-CAS# delay, $^{t}$RCD[4] | 18ns (-335)<br>15ns (-262)<br>20ns (-26A/-265) | 48<br>3C<br>50 | 48<br>3C<br>50 |
| 30 | MIN RAS# pulse width, $^{t}$RAS[2] | 42ns (-335)<br>45ns (-262/-26A/-265) | 2A<br>2D | 2A<br>2D |
| 31 | Module rank density | 128MB, 256MB | 20 | 40 |
| 32 | Address and command setup time, $^{t}$IS[3] | 0.8ns (-335)<br>1.0ns (-262/-26A/-265) | 80<br>A0 | 80<br>A0 |

**Table 13: Serial Presence-Detect Matrix (-335, -26A, and -265 Speed Grades) (continued)**

| Byte | Description | Entry (Version) | 128MB | 256MB |
|---|---|---|---|---|
| 33 | Address and command hold time, $^{t}IH$[3] | 0.8ns (-335)<br>1.0ns (-262/-26A/-265) | 80<br>A0 | 80<br>A0 |
| 34 | Data/data mask input setup time, $^{t}DS$ | 0.45ns (-335)<br>0.5ns (-262/-26A/-265) | 45<br>50 | 45<br>50 |
| 35 | Data/data mask input hold time, $^{t}DH$ | 0.45ns (-335)<br>0.5ns (-262/-26A/-265) | 45<br>50 | 45<br>50 |
| 36–40 | Reserved | 0 | 00 | 00 |
| 41 | MIN active-to-active/refresh time, $^{t}RC$ | 60ns (-335/-262)<br>65ns (-26A/-265) | 3C<br>41 | 3C<br>41 |
| 42 | MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period, $^{t}RFC$ | 72ns (-335)<br>75ns (-262/-26A/-265) | 48<br>4B | 48<br>4B |
| 43 | SDRAM device MAX cycle time, $^{t}CK$ (MAX) | 12ns (-335)<br>13ns (-262/-26A/-265) | 30<br>34 | 30<br>34 |
| 44 | SDRAM device MAX DQS–DQ skew time, $^{t}DQSQ$ | 0.45ns (-335)<br>0.5ns (-262/-26A/-265) | 2D<br>32 | 2D<br>32 |
| 45 | SDRAM device MAX read data hold skew factor, $^{t}QHS$ | 0.55ns (-335)<br>0.75ns (-262/-26A/-265) | 55<br>75 | 55<br>75 |
| 46 | Reserved | 0 | 00 | 00 |
| 47 | DIMM height | | 01 | 01 |
| 48–61 | Reserved | 0 | 00 | 00 |
| 62 | SPD revision | Release 1.0 | 10 | 10 |
| 63 | Checksum for bytes 0–62 | -335<br>-262<br>-26A<br>-265 | 29<br>BC<br>E9<br>19 | 4A<br>DD<br>0A<br>3A |
| 64 | Manufacturer's JEDEC ID code | MICRON | 2C | 2C |
| 65–71 | Manufacturer's JEDEC ID code | (continued) | 00 | 00 |
| 72 | Manufacturing location | 1–12 | 01–0C | 01–0C |
| 73–90 | Module part number (ASCII) | – | Variable data | Variable data |
| 91 | PCB identification code | 1–9 | 01–09 | 01–09 |
| 92 | Identification code (continued) | 0 | 00 | 00 |
| 93 | Year of manufacture in BCD | – | Variable data | Variable data |
| 94 | Week of manufacture in BCD | – | Variable data | Variable data |
| 95–98 | Module serial number | – | Variable data | Variable data |
| 99–127 | Reserved for manufacturer-specific data | | 00 | 00 |

Notes:
1. The value for -26A $^{t}CK$ set to 7ns (0 x 70) for optimum BIOS compatibility. Actual device specification value is 7.5ns.
2. The value of $^{t}RAS$ used for -262/-26A/-265 modules is calculated from $^{t}RC$ - $^{t}RP$. Actual device specification value is 40ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.
4. The value of $^{t}RP$, $^{t}RCD$, and $^{t}RAP$ for -335 modules indicated as 18ns to align with industry specifications; actual DDR SDRAM device specification is 15ns.

**Table 14: Serial Presence-Detect Matrix (-40B Speed Grade)**

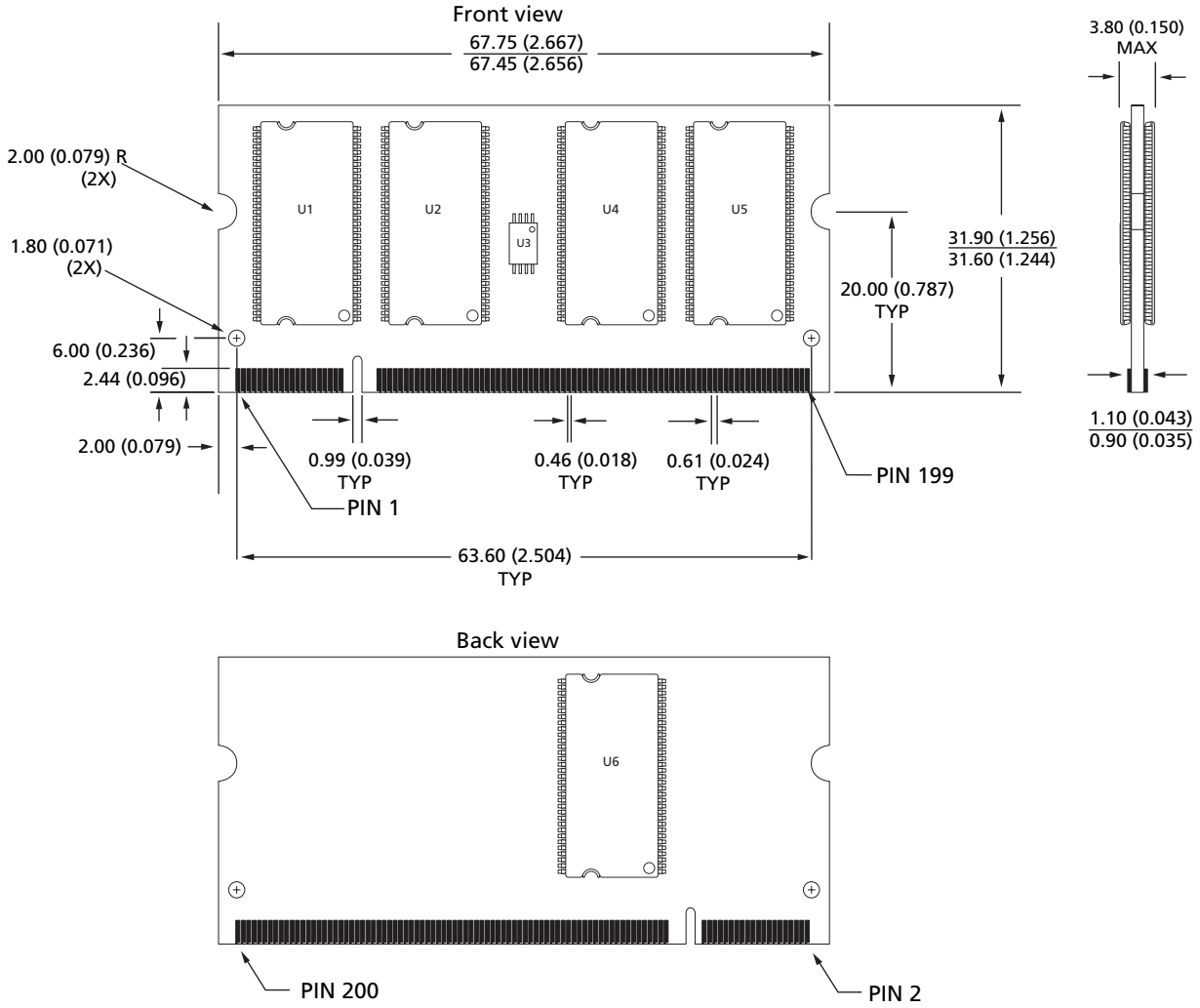
| Byte | Description | Entry (Version) | 256MB |
|---|---|---|---|
| 0 | Number of SPD bytes used by Micron | 128 | 80 |
| 1 | Total number of bytes in SPD device | 256 | 08 |
| 2 | Fundamental memory type | DDR SDRAM | 07 |
| 3 | Number of row addresses on assembly | 13 | 0D |
| 4 | Number of column addresses on assembly | 10 | 0A |
| 5 | Number of physical ranks on DIMM | 1 | 01 |
| 6 | Module data width | 72 | 48 |
| 7 | Module data width (continued) | 0 | 00 |
| 8 | Module voltage interface levels | SSTL 2.5V | 04 |
| 9 | SDRAM cycle time, $^{t}$CK, CL = 3 | 5ns | 50 |
| 10 | SDRAM access from clock, $^{t}$AC, CL = 3 | 0.7ns | 70 |
| 11 | Module configuration type | ECC | 02 |
| 12 | Refresh rate/type | 7.8µs/SELF | 82 |
| 13 | SDRAM device width (primary DDR SDRAM) | 16 | 10 |
| 14 | Error-checking DDR SDRAM data width | 16 | 10 |
| 15 | MIN clock delay, back-to-back random column access | 1 clock | 01 |
| 16 | Burst lengths supported | 2, 4, 8 | 0E |
| 17 | Number of banks on DDR SDRAM device | 4 | 04 |
| 18 | CAS latencies supported | 3, 2.5, 2 | 1C |
| 19 | CS latency | 0 | 01 |
| 20 | WE latency | 1 | 02 |
| 21 | SDRAM module attributes | Unbuffered/diff. clock | 20 |
| 22 | SDRAM device attributes: general | Fast/concurrent AP | C1 |
| 23 | SDRAM cycle time, $^{t}$CK, CL = 2.5 | 6ns | 60 |
| 24 | SDRAM access from clock, $^{t}$AC, CL = 2.5 | 0.7ns (-335 compatibility) | 70 |
| 25 | SDRAM cycle time, $^{t}$CK, CL = 2 | 7.5ns | 75 |
| 26 | SDRAM access from CK, $^{t}$AC, CL = 2 | 0.75ns (-265 compatibility) | 75 |
| 27 | MIN row precharge time, $^{t}$RP | 15ns | 3C |
| 28 | MIN row active-to-row active, $^{t}$RRD | 10ns | 28 |
| 29 | MIN RAS#-to-CAS# delay, $^{t}$RCD | 15ns | 3C |
| 30 | MIN RAS# pulse width, $^{t}$RAS | 40ns | 28 |
| 31 | Module rank density | 256MB | 40 |
| 32 | Address and command setup time, $^{t}$IS | 0.6ns | 60 |
| 33 | Address and command hold time, $^{t}$IH | 0.6ns | 60 |
| 34 | Data/data mask input setup time, $^{t}$DS | 0.4ns | 40 |
| 35 | Data/data mask input hold time, $^{t}$DH | 0.4ns | 40 |
| 36–40 | Reserved | 0 | 00 |
| 41 | MIN active-to-active/refresh time, $^{t}$RC | 55ns | 37 |
| 42 | MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period, $^{t}$RFC | 70ns | 46 |
| 43 | SDRAM device MAX cycle time,$^{t}$CK (MAX) | 12ns | 30 |
| 44 | SDRAM device MAX DQS–DQ skew time, $^{t}$DQSQ | 0.4ns | 28 |
| 45 | SDRAM device MAX read data hold skew factor, $^{t}$QHS | 0.5ns | 50 |
| 46 | Reserved | 0 | 00 |
| 47 | DIMM height | | 01 |

**Table 14: Serial Presence-Detect Matrix (-40B Speed Grade) (continued)**

| Byte | Description | Entry (Version) | 256MB |
|---|---|---|---|
| 48–61 | Reserved | 0 | 00 |
| 62 | SPD revision | Release 1.1 | 11 |
| 63 | Checksum for bytes 0–62 | – | A3 |
| 64 | Manufacturer's JEDEC ID code | MICRON | 2C |
| 65–71 | Manufacturer's JEDEC ID code | (continued) | 00 |
| 72 | Manufacturing location | 1–12 | 01–0C |
| 73–90 | Module part number (ASCII) | – | Variable data |
| 91 | PCB identification code | 1–9 | 01–09 |
| 92 | Identification code (continued) | 0 | 00 |
| 93 | Year of manufacture in BCD | – | Variable data |
| 94 | Week of manufacture in BCD | – | Variable data |
| 95–98 | Module serial number | – | Variable data |
| 99–127 | Reserved for manufacturer-specific data | | 00 |

# Module Dimensions

**Figure 3: 200-Pin SODIMM Dimensions**




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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