

μPG2163T5N-EVAL-A

Evaluation Board

- Description
- Insertion Loss of Through Board
- Assembly Drawing

Description:

The uPG2163T5N-EVAL-A evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2163T5N switch. In addition to the device, the board provides DC block capacitors, power supply bypass capacitors, and RF and DC connectors.

A DC block capacitor is required at all RF ports. On this board, two parallel capacitors of 22pF are used for this purpose. This configuration minimizes the mismatch effect associated with the serial capacitor over a relatively wide frequency range (2 to 6GHz). For a narrow band application or an application where the operating frequency is outside the specific frequency range, the user may select a different capacitance value. Generally the performance of the switch circuit is not sensitive, to a certain extent, to the value of DC block capacitors.

A 1000pF DC bypass capacitor is used on all control lines. For high speed applications the user may choose smaller capacitance or no capacitor at all.

DC supply connectors:

P1 is control voltage V_{cont1} , P2 is V_{cont2} and pins P3 and P4 are the ground. V_{cont1} and V_{cont2} should be connected to separate power supplies to provide the required control logic.

RF connectors:

As indicated on the board, J1 (IN) is connected to the ANT port, J2 (OUT1) is connected to the TX port, and J3 (OUT2) is connected to the RX.

Information on Board Material:

The board material is 20 mil thick Duroid 6002. Its dielectric constant is 2.94.

Switch Logic Table:

The following table lists the logic table for switch states.

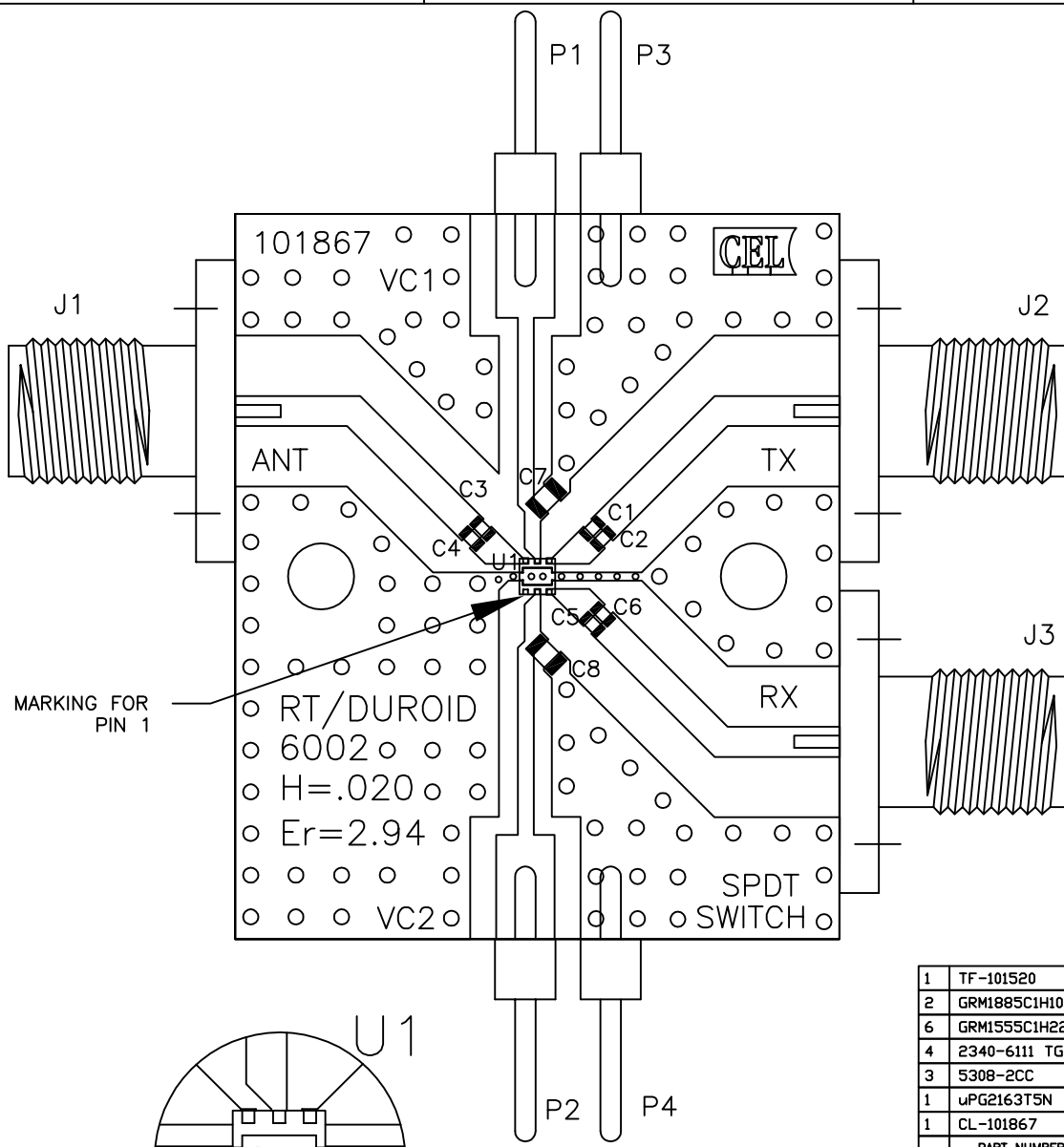
Vcont1	Vcont2	(IN)ANT – OUT1(TX)	(IN)ANT – OUT2(RX)
H	L	OFF	ON
L	H	ON	OFF

Insertion Loss of Through Board:

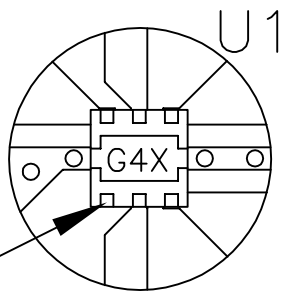
In assessing the insertion loss of the switch by measuring S21 of the evaluation board, it is necessary to take into account the loss through the connectors and PCB trace. To this end a through board was characterized to determine the board/connector loss. The table below lists the board loss at different frequencies.

INPUT FREQUENCY (GHz)	BOARD LOSS (dB)
2.4	0.12
2.5	0.13
4.9	0.24
5.8	0.30
6.0	0.32

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



MARKING FOR PIN 1



MARKING FOR PIN 1 (PIN NOT CONNECTED)

QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	TF-101520		TEST CIRCUIT BLOCK	7
2	GRM1885C1H102JA01D	C7,C8	0603 1000pF CAP MURATA	6
6	GRM1555C1H220JZ01D	C1 THRU C6	0402 22pF CAP MURATA	5
4	2340-6111 TG	P1,P2,P3,P4	PIN HEADER 3M	4
3	5308-2CC	J1,J2,J3	SMA FEMALE CONNECTOR TENSOLITE	3
1	uPG2163T5N	U1	NEC GaAs Switch uPG2163T5N	2
1	CL-101867	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

NEXT ASSY	USED ON	APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
 TOLERANCES
 DECIMALS ANGULAR
 .XX± .01 ± 1°
 .XXX± .005
 DO NOT SCALE DRAWING
 MATERIAL
 FINISH

APPROVALS	
Drawing by: Hugues de Saint Salvy	2005/04/22
Designed by: Hugues de Saint Salvy	2005/04/22
Checked by:	
Project Engineer:	
Quality Control:	

CEL CALIFORNIA EASTERN LABS
 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
 uPG2163T5N-EVAL-A
 ASSEMBLY DRAWING

SIZE C	FSCM NO.	DWG NO. AD-101867	REV —
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SCALE NONE RELEASE DATE PROTOTYPE SHEET 1 OF 1