Freescale Semiconductor
Product Brief

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MPC8308 Product Brief PowerQUICC™ II Pro Processor

This document provides an overview of the MPC8308 PowerQUICC II Pro processor features, including a block diagram showing the major functional components. The MPC8308 is a cost-effective, low-power, highly integrated host processor that addresses the requirements of networking applications such as low-end printing, smart grid home energy gateway, data concentrators, wireless LAN access points, wireless femto base stations, and industrial applications such as industrial control and factory automation. The MPC8308 extends the PowerQUICC II Pro family, adding high CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

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1 Application Examples

The features of the MPC8308 make it suitable for a wide variety of printer and network communication applications as described in this section.

1.1 Low-End Printer CPU

Figure 1 illustrates how the MPC8308 can interface with the main ASIC on a low-end printer application.

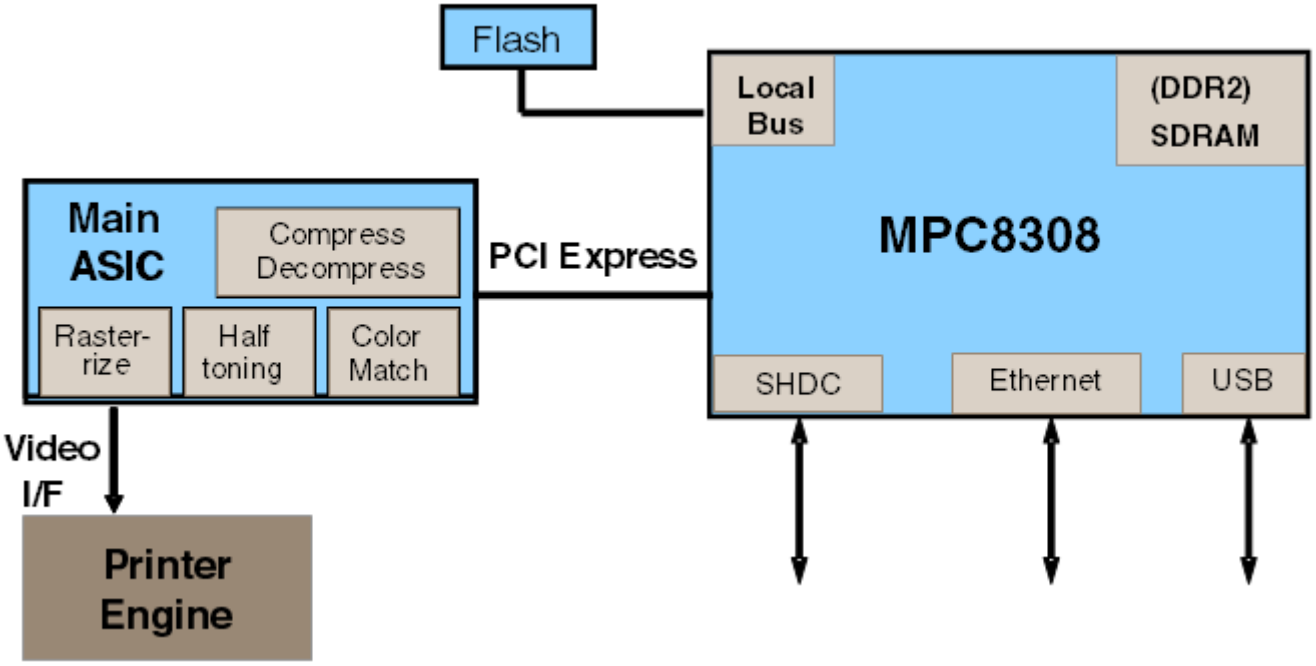

Figure 1. MPC8308 Serving as the Main CPU in a Low-End Printer Application

In this application, the device interfaces to the main ASIC through the high-bandwidth PCI-Express bus. Low-end multi-function printers (MFPs) are able to share the same platform simply by adding a scanner/fax engine. The processor provides various network interfaces that are used to access the printer.

Image data coming through the scanner or fax interface is sent to the main ASIC, which processes the image by implementing algorithms for image compression/decompression and rendering. The image data is then processed in the FPU in the CPU core at high speeds and sent to the printer engine. Likewise, image data or text data that are interfaced at the Ethernet interface on the processor are also manipulated at the main ASIC and CPU and sent to the printer engine.

Recent MFP systems require higher processor performance in order to manipulate large, high-quality images at high speeds. Required networking interfaces including USB, PCI Express, eSHDC, and Gigabit Ethernet are integrated on the MPC8308. As a result, an MFP application can be developed by combining the MPC8308 with the main ASIC (graphic processing ASIC) at a lower cost .

1.2 Smart Energy Metering Gateway

Figure 2 illustrates how an MPC8308 can function as a host CPU in a smart energy metering gateway.

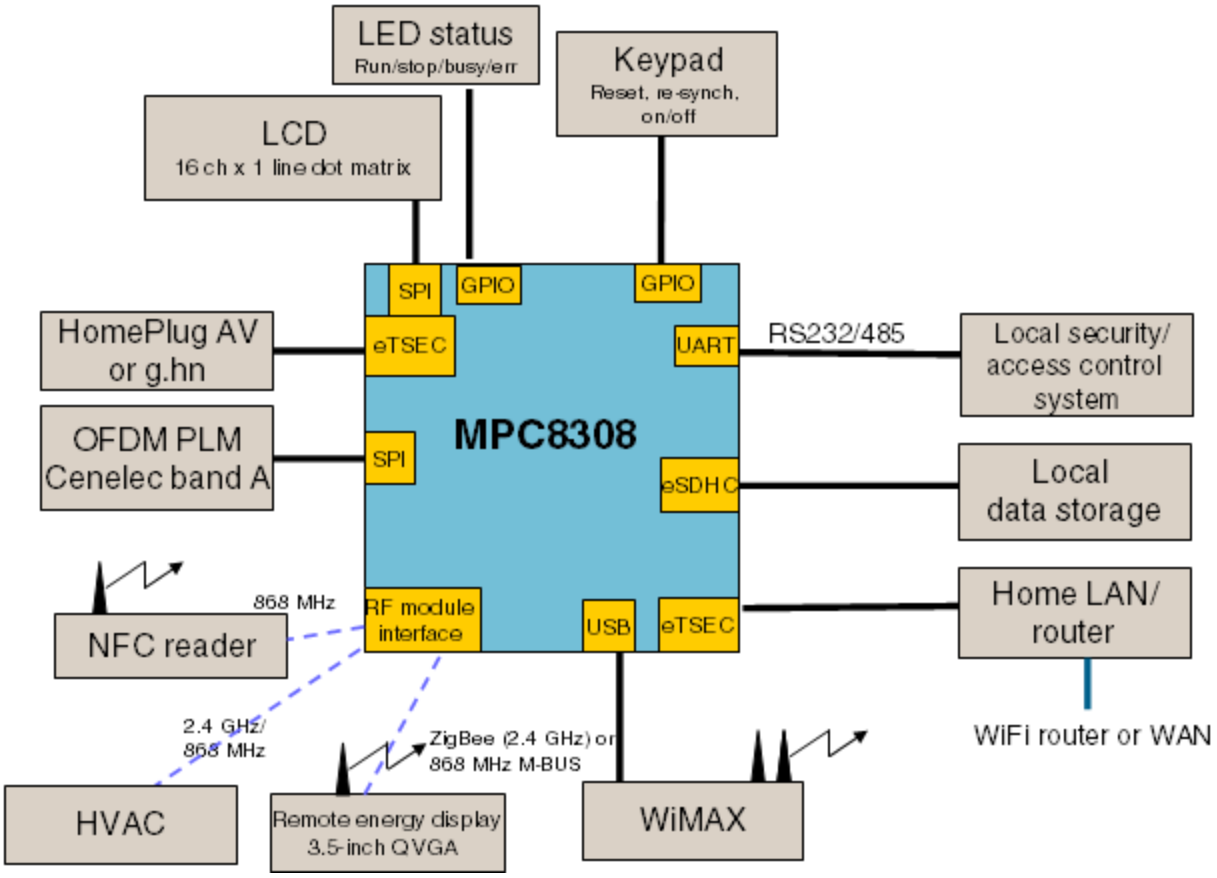

Figure 2. MPC8308 Implementation in a Smart Energy Metering Gateway Application

In this application, MPC8308 resides in the gateway box, separate from the meter, and provides the wireless connectivity for transmitting and receiving data using the IP network. A customer can implement a variety of Wide Area Network (WAN) cards such as Wimax (using USB 2.0 interface), Powerline communication module (using MII interface) etc. to communicate with the utility customer's back office.

MPC8308 processor can also provide connectivity for the Local Area Network via the eTSEC (RGMII, MII) interface to the wireless router in the home.

As shown in the application diagram, MPC8308 provides a wide range of interfaces to complete a smart energy metering gateway system.

1.3 IEEE Std 1588™ in Test and Measurement and Industrial Automation

Figure 3 shows how a test and measurement application can use the IEEE 1588 precise time synchronization.

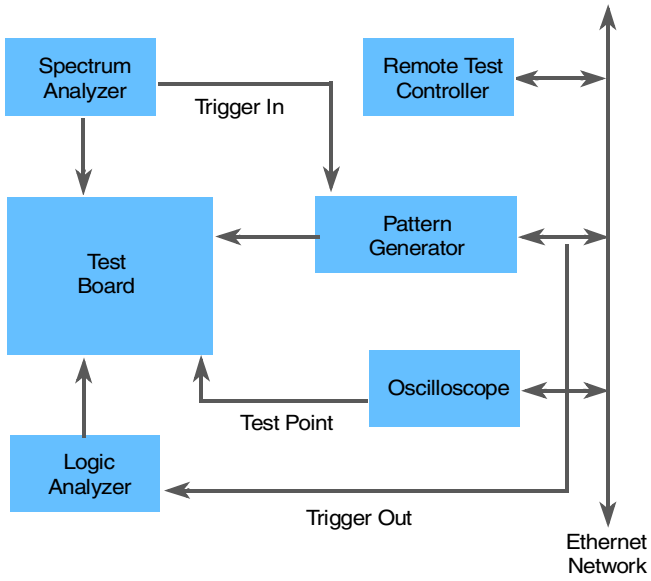

Figure 3. IEEE 1588 in Test and Measurement

In this application, IEEE 1588 allows coordination and control of test and measurement equipment over a distributed Ethernet network. Precise timing delivery allows test equipment to deliver patterns and measure responses at specific times, enabling accurate timestamping of measured data and allowing coordination of input stimuli and any associated measured data. The trigger inputs and outputs enable coordination of other devices.

Figure 4 illustrates how an industrial control application is able to take advantage of the IEEE 1588 precise time synchronization.

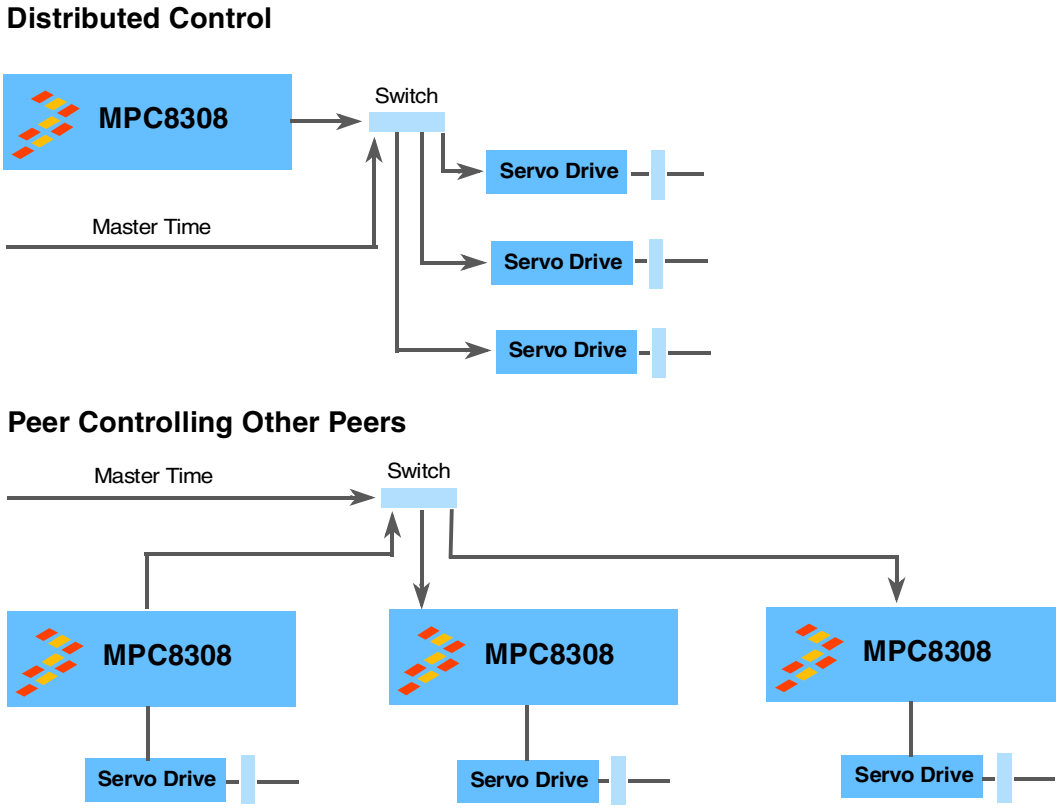

Figure 4. IEEE 1588 in Industrial Control

As shown in the example on the top of the figure, IEEE 1588 allows precision control over a distributed Ethernet network. Precise timing delivery allows drive units to be placed where required. Traditional mechanical control mechanisms can limit the placement of systems.

In the bottom of the figure, timing synchronization at the drive enables flexibility in system configuration. Issues due to mismatched cable lengths are minimized. Servos can be added or deleted without having to rewire other servos. Industrial control applications typically augment IEEE 1588 hardware to provide trigger inputs and outputs.

In summary, IEEE 1588 support in the MPC8308 enables accurate synchronization of clocks with varying precision, resolution, and oscillator stability in distributed systems. IEEE 1588 synchronizes individual clocks to maintain accurate distribution-wide timing. It enhances applications that need local clocks at each control node and provides sub-microsecond synchronization over long distances using standard cabling. Target applications for systems with IEEE 1588 are test and measurement appliances and industrial control and automation.

1.4 IEEE Std 802.11*n*™ WLAN Access Point

Figure 5 illustrates the MPC8308 acting as an IEEE 802.11*n* WLAN access point.

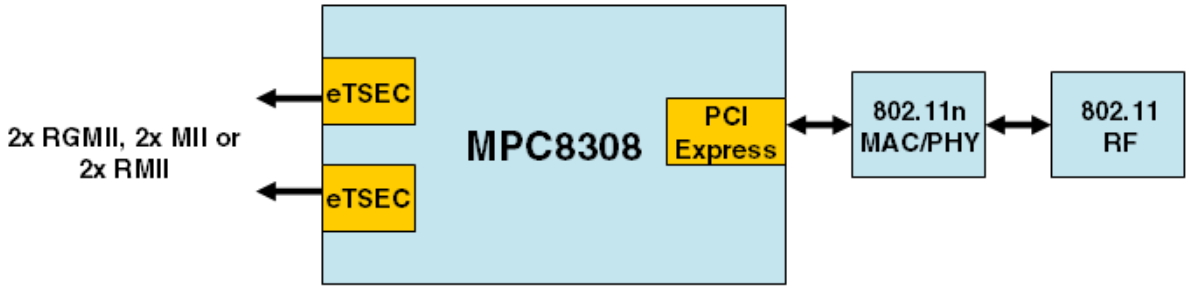

Figure 5. MPC8308 as a WLAN Access Point

Current systems are being designed for IEEE 802.11 a/b/g/n as well as combo radios. The WiFi chipsets are on PCI-Express bus in current systems. With the requirement of streaming video and other increased management features required by the IT community, there is a need for higher performance.

These WLAN access points (WAPs) require low power and are usually powered exclusively by Power over Ethernet (POE). Each Ethernet line can power about 12 W. With the power the radios draw and the rest of the board this usually only leaves < 2.5 W for the embedded processor.

2 Features

The MPC8308 incorporates the e300 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support.

In addition to the e300 core, the SoC platform includes features such as a dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with IEEE 1588 support, a 32- or 16-bit DDR2 SDRAM memory controller, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8308 also offers peripheral interfaces such as 16-bit enhanced local bus interface with up to 66-MHz operation, SDHC, and USB 2.0 controller.

The MPC8308 offers additional high speed interconnect support with single-lane PCI Express interface.

2.1 Block Diagram

A block diagram of the MPC8308 is shown in Figure 6.

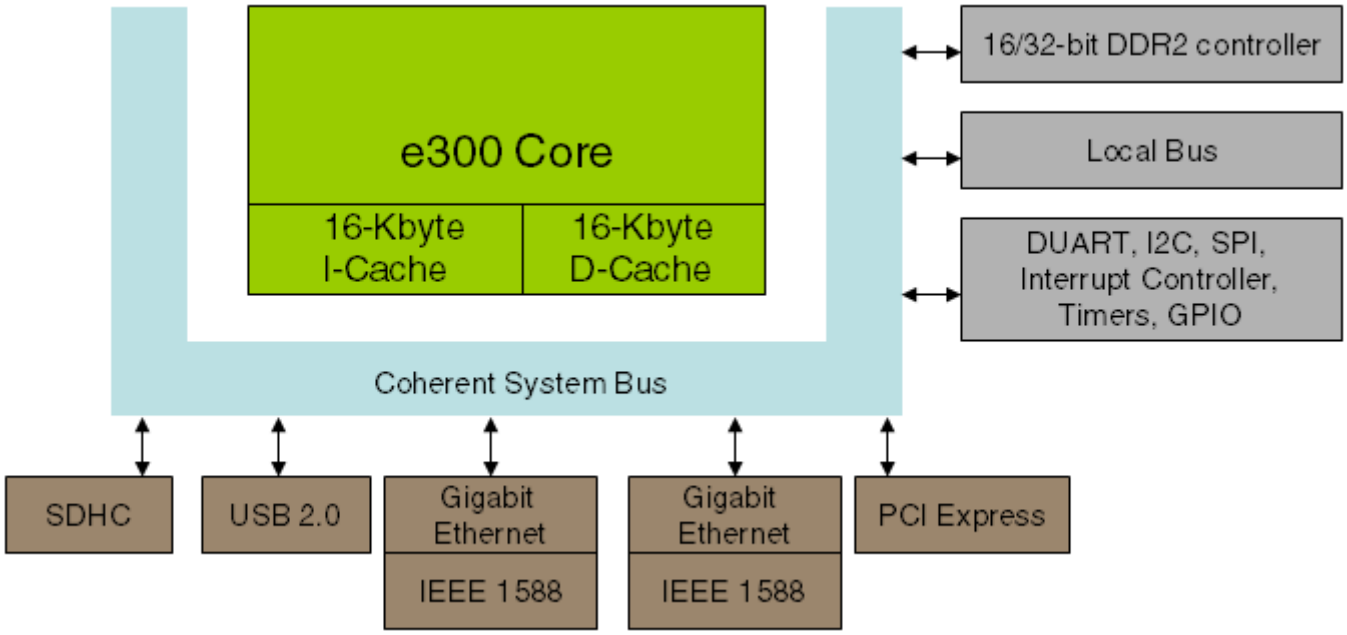

Figure 6. MPC8308 Block Diagram

2.2 Chip-Level Features

The major features of the MPC8308 are as follows:

- e300 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, a floating point unit, and performance monitor
- Single PCI Express x1 controller with integrated SerDes PHY
- Dual three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSEC)
- 32/16-bit DDR2 memory controller
- Secure digital Host controller (SDHC) interface
- USB 2.0 host and device controller
- Flexible enhanced local bus controller (eLBC)
- Integrated programmable interrupt controller (IPIC)
- General Purpose DMA controller
- Single I^2C controller
- Serial peripheral interface (SPI) controller with master and slave support
- General-purpose I/O (GPIO) port with 24 parallel I/O pins muxed on various interfaces
- System timers including a periodic interrupt timer, real-time clock, software watchdog timer, and four general-purpose timers
- Dual UART (DUART)

- Designed to comply with IEEE Std 1149.1™, JTAG boundary scan
- 473 MAPBGA package

2.3 Module Features

The PowerQUICC II Pro MPC8308 is a high-performance, power-saving, highly integrated host processor solution.

2.3.1 e300 Core

The e300 core has the following features:

- Operates at up to 333 MHz
- 16-Kbyte instruction cache, 16-Kbyte data cache with ECC
- Floating point unit
- Software-compatible with the Freescale processor families implementing the Power Architecture™
- Performance monitor

2.3.2 Single PCI Express Interface

The PCI Express interface has the following features:

- PCI Express 1.0a-compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor-based DMA engine per interface with separate read and write channels

2.3.3 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8308 eTSECs include the following features:

- Designed to comply with IEEE Std 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ab™, 802.3ac™, and IEEE 1588
- Support for different Ethernet physical interfaces:
  - 1000 Mbps IEEE 802.3 RGMII, full-duplex
  - 10/100 Mbps IEEE 802.3 MII full and half-duplex
  - 10/100 Mbps IEEE 802.3 RMII full and half-duplex

- 9.6 Kbyte jumbo frame support
- RMON statistics support
- Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per eTSEC module
- MII management interface for external PHY control and status
- Programmable CRC generation and checking
- Support for weighted round robin and strict priority queueing
- TCP/IP checksum offload for Rx and Tx
- IPv6 and Magic Packet support
- IEEE 1588 support added
- Lossless flow control support
- QoS support for 8 Rx and 8 Tx hardware queues
- Customizable per-packet rejection
- Customizable per-packet filtering/filing to 64 logical receive queues.
  - Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.
- Layer 2 features
  - VLAN insertion and deletion per frame
  - 2 exact-match MAC addresses
- Increased hash table address matching

2.3.4 DDR2 Memory Controller

The MPC8308 DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting DDR2 SDRAM.
- Supports single-bit error correction, double-bit error detection when ECC is enabled, and error injection
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- SDRAM chip configurations up to 2-Gbit (for DDR2) devices with x8/x16/x32 data ports
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus OR one 32-bit device or two 16-bit devices or four 8-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-V SSTL2 compatible I/O

2.3.5 USB Dual-Role Controller

The MPC8308 USB controller includes the following features:

- Designed to comply with *USB Revision 2.0 Specification*

- Supports operation as a stand-alone USB device
  - — Supports one upstream facing port
  - — Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - — Supports USB root hub with one downstream-facing port
  - — Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports USB on-the-go (OTG) mode, which includes both device and host functionality when using an external ULPI (UTMI+ low-pin interface) PHY
- Supports ULPI

2.3.6 Enhanced Secure Digital Host Controller (eSDHC)

The eSDHC includes the following features:

- Compatible to SD Host Controller Standard Specification version 2.0 with test event register support
- Compatible with the MMC System Specification version 4.0
- Compatible with the SD Memory Card Specification version 2.0, and supports High Capacity SD memory cards
- Compatible with the SDIO Card Specification version 1.2
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC mode devices

2.3.7 Enhanced Local Bus Controller (eLBC)

The MPC8308 enhanced local bus controller (eLBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system.

The eLBC offers the following features:

- Non-multiplexed 26-bit address and 16-bit data operating at up to 66 MHz
- Four chip selects support four external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes are controlled by an on-chip memory controller

- Three protocol engines available on a per chip select basis:
  - General-purpose chip select machine (GPCM)
  - NAND flash control machine (FCM)
  - Three user programmable machines (UPMs)
- Default boot ROM chip select with configurable bus width (8 or 16 bits)

2.3.8 Integrated Programmable Interrupt Controller (IPIC)

The IPIC implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.3.9 DMA Controller

The DMA is a highly-programmable data transfer engine, which is optimized to minimize the required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known, and is not defined within the data packet itself. The DMA hardware supports the following:

- Single design with two channels (Tx and Rx)
- 32-byte transfer control descriptor per channel stored in local memory
- 32 bytes of data registers, used as temporary storage to support burst transfers

Throughout this section, *n* is used to reference the channel number. Additionally, data sizes are defined as byte (8-bit), halfword (16-bit), word (32-bit) and doubleword (64-bit).

2.3.10 Single I^2C, Serial Peripheral Interface (SPI), DUART, Timers

The I^2C controller is a synchronous, multi-master bus that can be connected to additional devices for expansion and system development.

The serial peripheral interface (SPI) allows the MPC8308 to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8308 system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

The general purpose timers have the following features:

- Four 16-bit programmable timers

- Two timers cascaded internally or externally to form a 32-bit timer
- One timer cascaded internally or externally to form a 64-bit timer
- Three programmable input clock sources for the timer prescalers
- Input capture capability
- Output compare with programmable mode for the output pin
- Free run and restart modes
- Functional and programming compatibility with MPC8260 timers

3 Developer Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support, and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e300 core.

Freescale also provides an RDB board as a reference platform and programming development environment for the MPC8308 with a complete Linux board support package. The RDB board will support on-board DDR2 memory, a PCI-Express interface, and a debug port.

4 Document Revision History

Table 1 shows the revision history of this product brief.

Table 1. Revision History

Rev. Number	Date	Substantive Change(s)
0	11/2009	Initial public release.

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