CSI2 to Parallel Bridge Board

User's Guide

February 2013
Revision: EB81_01.1

Introduction

The CSI2 to Parallel Bridge Board comprises a compact, low cost, MIPI CSI2 (Camera Serial Interface) image sensor, lens and lens housing with adjustable focus, that can bolt directly onto the Lattice HDR-60 Base Board or the MachXO2™ Dual Sensor Interface Board. Both the CSI2 to Parallel Bridge Board and the MachXO2 Dual Sensor Interface Board are designed to work together. These boards plug into the HDR-60 Base Board to allow for a demonstration. The CSI2 to Parallel Bridge Board is designed to use the Sony IMX169 CMOS Digital Image Sensors which feature:

- Up to 13 megapixels
- HD video (1080p30 mode configurable)
- Selectable video or single frame modes
- MIPI CSI2 output, either two or four data lanes

Read more about the image sensor specifications in the Sony IMX169 data sheet.

Features

Key features of the CSI2 to Parallel Bridge Board include:

- Sony IMX169 CMOS Digital Image Sensor
- Lens: F/1.59, <7% distortion, with minimized flare, halo, and ghosting
- Lens holder with adjustable focus
- CSI2 or parallel signal connections to the MachXO2 Dual Sensor Interface Board or HDR-60 Base Board
- Selectable on-board 27.000 MHz MEMs oscillator, or HDR-60 Base Board oscillator
- Power status LEDs with one user-defined LED

General Description

The CSI2 to Parallel Bridge Board has been designed for use on the MachXO2 Dual Interface Sensor Board and the HDR-60 Base Board. The CSI2 to Parallel Bridge Board contains the camera sensor portion, while the MachXO2 Dual Sensor Interface Board performs the CSI2 to parallel conversion. The HDR-60 Base Board allows the user to see an image on a HDMI monitor. See RD1146, MIPI CSI2 to CMOS Parallel Sensor Bridge, for more information concerning a related demo.

Initial Setup and Handling

The following is recommended reading prior to removing the CSI2 to Parallel Bridge Board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the boards can be damaged by improper handling.

The devices on the evaluation boards contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static-sensitive to conditions that exceed their designed-in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation boards when they are removed from the static shielding bag. If you will not be using the boards for a while, it is best to put them back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the boards when they are not in use.

When reaching for the boards, it is recommended that you first touch the outside shield portion of the J11 BNC connector on the HDR-60 Base Board. If the CSI2 to Parallel Bridge Board is not installed on the HDR-60 Base Board, then when reaching for the CSI2 to Parallel Bridge Board, it is recommended that you first touch the outside edge of the mounting holes on the CSI2 to Parallel Bridge Board. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connection to the board, should be from test equipment chassis ground to the J11 BNC shield GND on the HDR-60 Base Board.

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the J11 BNC shield GND on the HDR-60 Base Board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it is not in a static shielding bag, please keep one finger on the J11 BNC shield GND on the HDR-60 Base Board. If carrying the CSI2 to Parallel Bridge Board alone, keep one finger one of the mounting holes. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 42mm x 42mm (1.654" x 1.654"). Additional mechanical board dimension information is included on the mechanical drawing shown in Appendix A, Figure . On the physical board itself, connectors include pin 1 indictors as either an arrow, or triangle point near pin 1 on the outer layer silk screen. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation

Functional Description

Figure 1. CSI2 to Parallel Bridge Board Revision B

Voltage Regulators

The CSI2 to Parallel Bridge Board power is supplied by the 5V DC power applied at connectors J7 and J8, pins 1, 2, 39 and 40. The on-board linear voltage regulators then provide the necessary supply voltages to power the sensor: 2.7V, VDDIO, 1.2V, 1.8V, 2.5V and 3.3V. The regulator in location U10 can be configured as shown in Table 1.

Table 1. CSI2 to Parallel Bridge Board Regulator Voltages

Supply	Voltage Regulator	Resistor Ratio	Comment
V1P8_V3P3	On HDR-60 Base Board	R45/R50 1.8V R58/R50 2.5V R59/R50 3.3V	Jumper J253 short: 1.8V: 1 and 2 2.5V: 3 and 4 (default configuration) 3.3V: 5 and 6

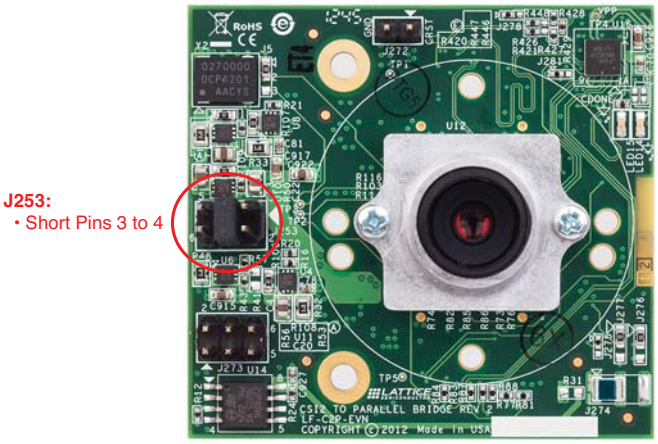
Each of the LT3025 regulators are the linear low dropout voltage type that incorporate an external resistor divider voltage feedback to divide down the regulator output voltage and compare it against an internal reference voltage. The regulator then adjusts the output voltage higher or lower such that the resistor divided voltage matches the internal reference. By doing this, each regulator output voltage remains at a constant voltage value independent of the load it drives. Each regulator output voltage follows this equation:

V_{OUT} = (1 + resistor ratio) x (regulator internal reference voltage)

See the LT3025 device data sheet for additional details about this device.

The default configuration for J253 is for 2.5V via shorting pins 3 and 4 as shown in Figure 2.

Figure 2. CSI2 to Parallel Bridge Board with Sony IMX169 CSI2 Sensor



MEMS Oscillator (Y2)

As shown in Figure 2, J5 is set such that the IMX169 sensor will receive a clock input signal from the internal 27.000 MHz MEMS oscillator (Y2). The alternate position of J5 will select the HDR-60 Base Board oscillator for the sensor clock input.

High-Speed CSI2 Connector (J8)

The Sony IMX169 (U12) will produce high-speed CSI2 differential signals after proper configuration via SCLK and SADDR pins. There is a CSI2 differential clock and up to four CSI2 differential data lanes. The J8 connector can plug into the MachXO2 Dual Sensor Interface Board or into the HDR-60 Base Board. The signals are identified in Table 2.

Table 2. CSI2 to Parallel Bridge Board (J8)

J8 Pin	IMX169 I/O Pin	Signal	Polarity	Description
13	K4	CSI2 data0	P	Differential CSI2 data
11	J4	CSI2 data0	N	Differential CSI2 data
29	K6	CSI2 data1	P	Differential CSI2 data
27	J6	CSI2 data1	N	Differential CSI2 data
21	K3	CSI2 data2	P	Differential CSI2 data
19	J3	CSI2 data2	N	Differential CSI2 data
26	K7	CSI2 data3	P	Differential CSI2 data
24	J7	CSI2 data3	N	Differential CSI2 data
18	K5	CSI2 clock	P	Differential CSI2 clock
16	J5	CSI2 clock	N	Differential CSI2 clock
12	J4	CSI2 low speed data bit 0	—	Single-ended CSI2 data 0 N side

Parallel Connector (J7)

Connector J7 is primarily reserved for future use. When used with the MachXO2 Dual Sensor Interface Board, only a few pins are used as shown in Table 3.

Table 3. CSI2 to Parallel Bridge Board (J7)

J7 Pins	IMX169 I/O Pin	Signal	Polarity	Description
30	K4	CSI2 low speed data bit 0	—	Single-ended CSI2 data 0 P side
28	C5	I^2C SCLK	—	Serial clock to program IMX169
26	B5	I^2C SADDR	—	Serial address to program IMX169
9-25, 27, 29, 31			—	Reserved for future use via iCE40

References

- RD1146, MIPI CSI2 to CMOS Parallel Sensor Bridge
- HDR-60 Video Camera Development Kit web page
- DS1021, LatticeECP3 Family Data Sheet
- HB1009, LatticeECP3 Family Handbook
- EB59, HDR-60 Base Board User's Guide
- EB69, MachXO2 Dual Sensor Interface Board User's Guide
- QS010, LatticeECP3 Video Camera Development Kit QuickSTART Guide

Ordering Information

The CSI2 to Parallel Bridge Board is designed solely for use with the MachXO2 Dual Sensor Interface Board and/or the HDR-60 Video Camera Development Kit.

Description	Ordering Part Number	China RoHS Environment Friendly
CSI2 to Parallel Bridge Board	LF-C2P-EVN	
MachXO2 Dual Sensor Interface Board	LCMXO2-4000HE-DSIB-EVN	
HDR-60 Video Camera Development Kit *(Contains: HDR-60 Base Board with LatticeECP3 FPGA pre-loaded with Image Signal Processing (ISP) Demo, two USB cables, HDMI cable with HDMI-to-DVI adapter, 12V AC adapter power supply, QuickSTART Guide)*	LFE3-70EAHDR60-DKN	

Technical Support Assistance

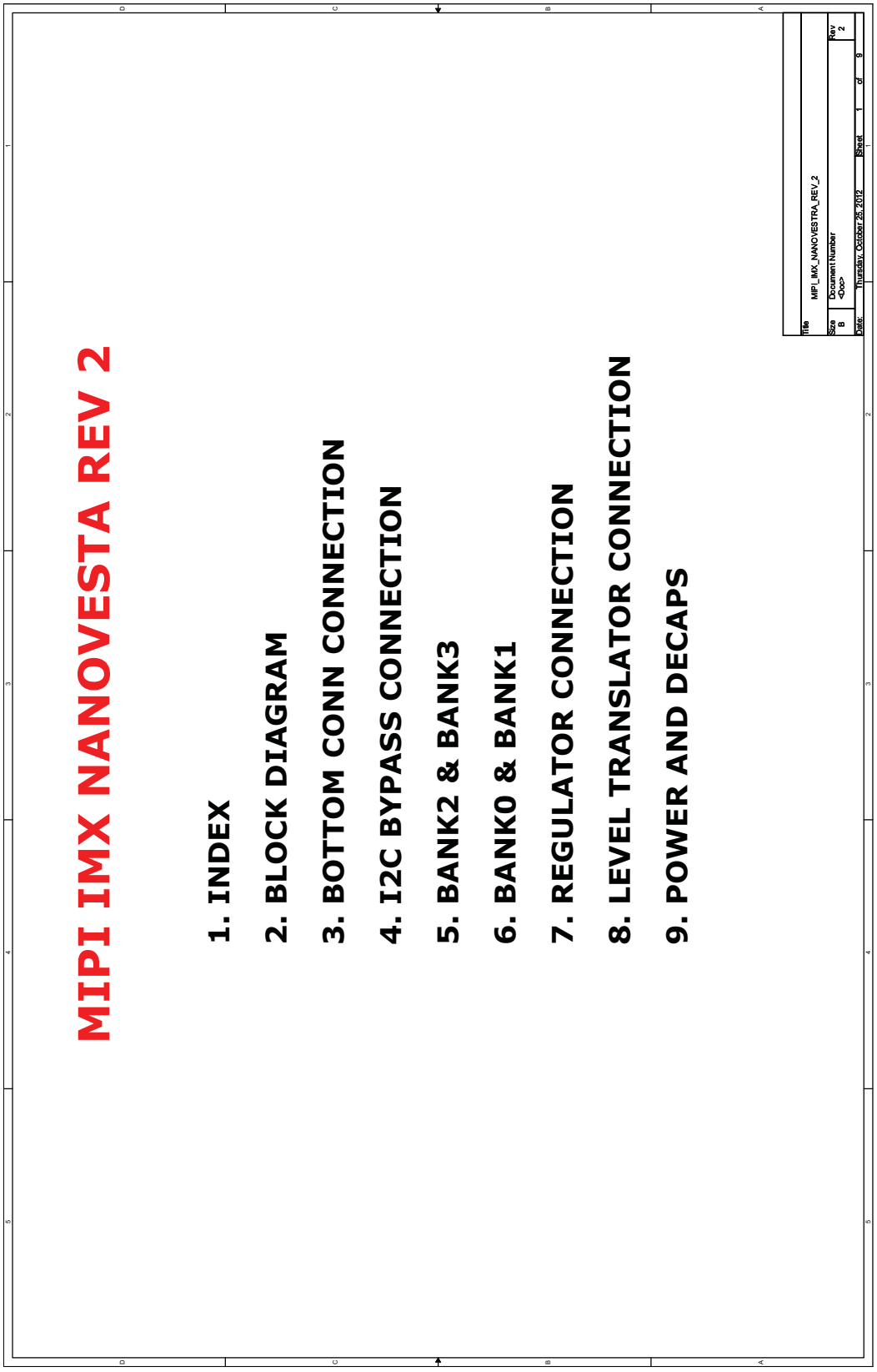
Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

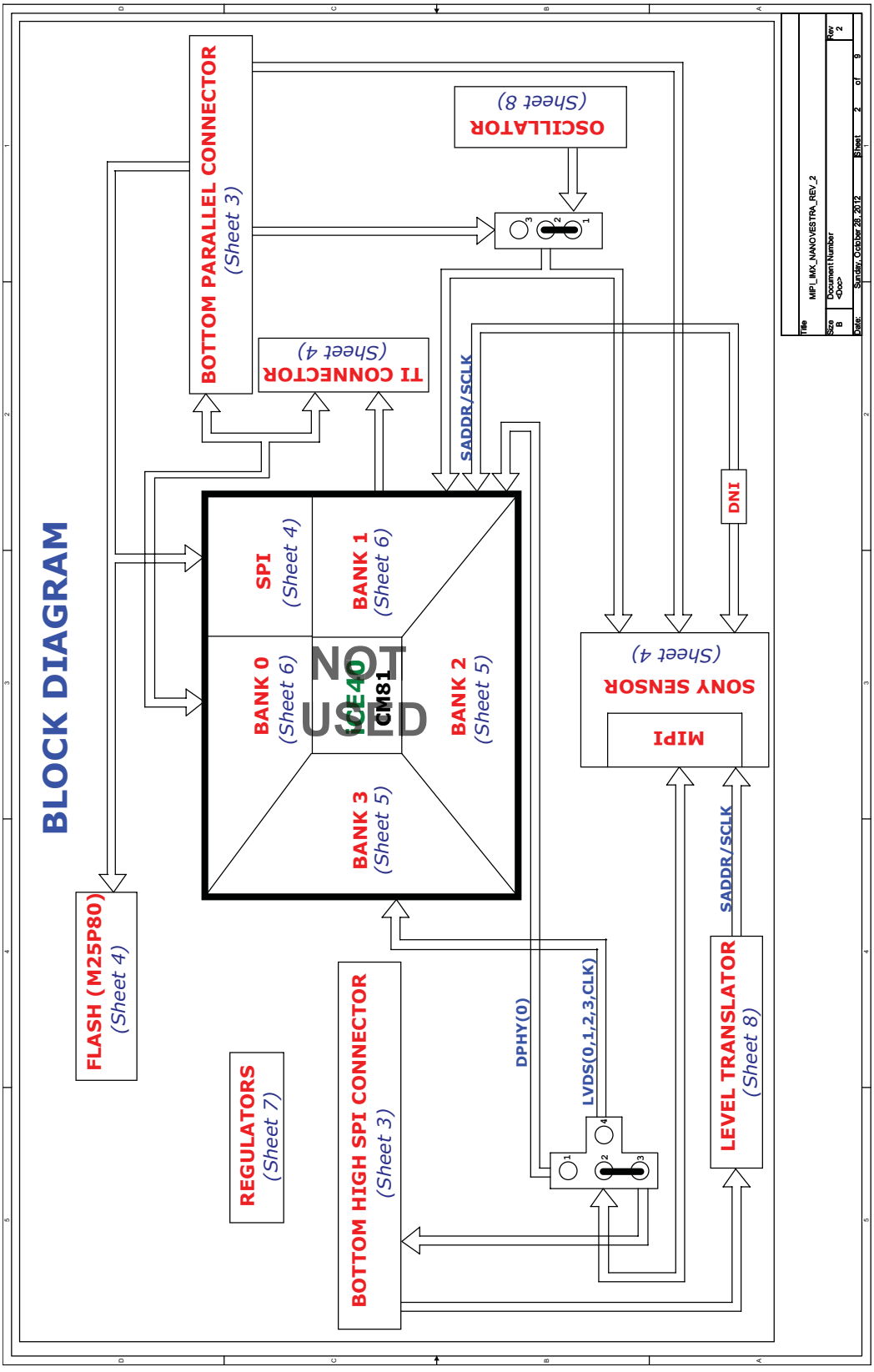
Date	Version	Change Summary
December 2012	01.0	Initial release.
February 2013	01.1	Clarify that CSI-2 is for use with MachXO2.

Appendix A. Schematic

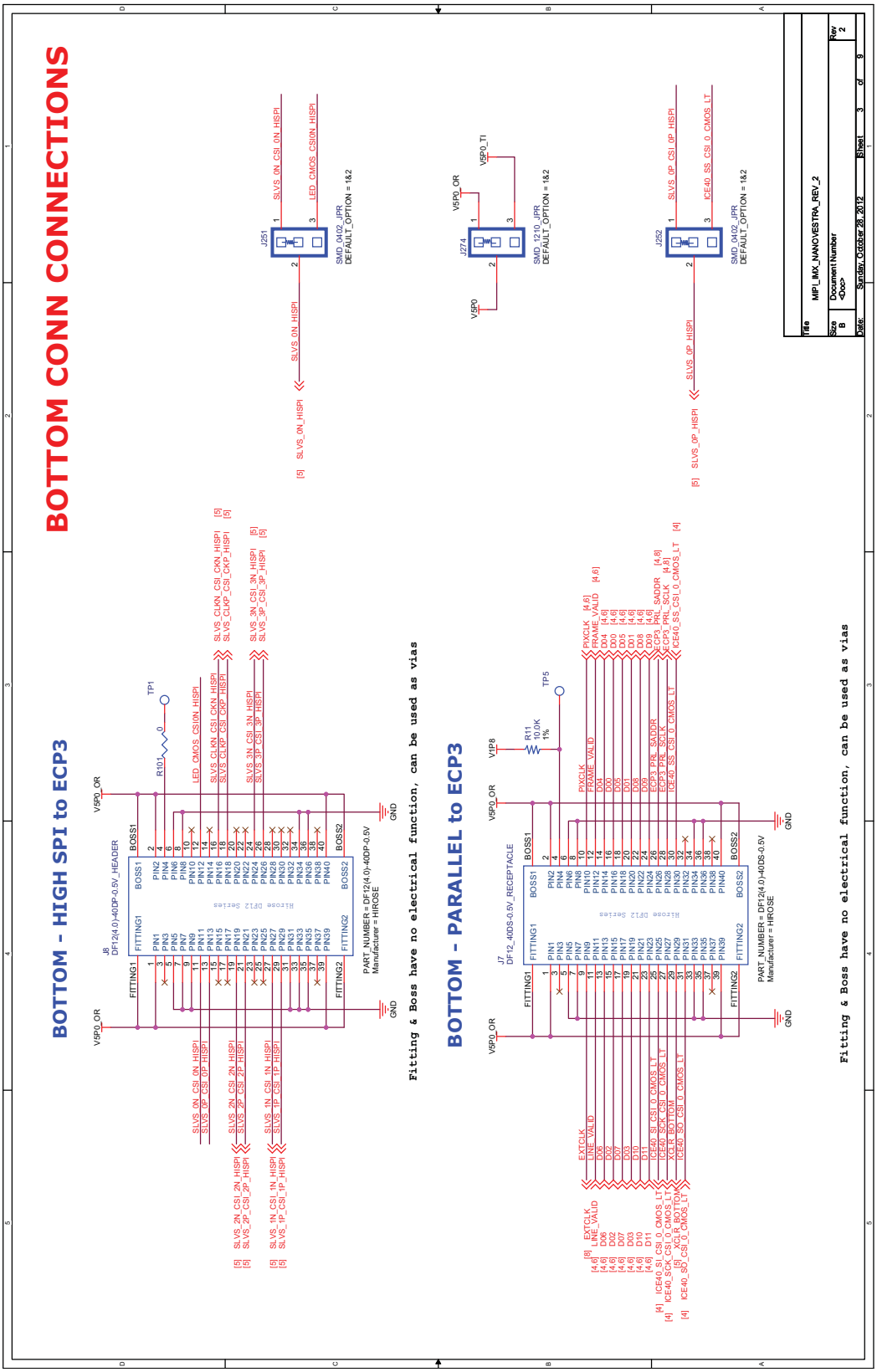
Index



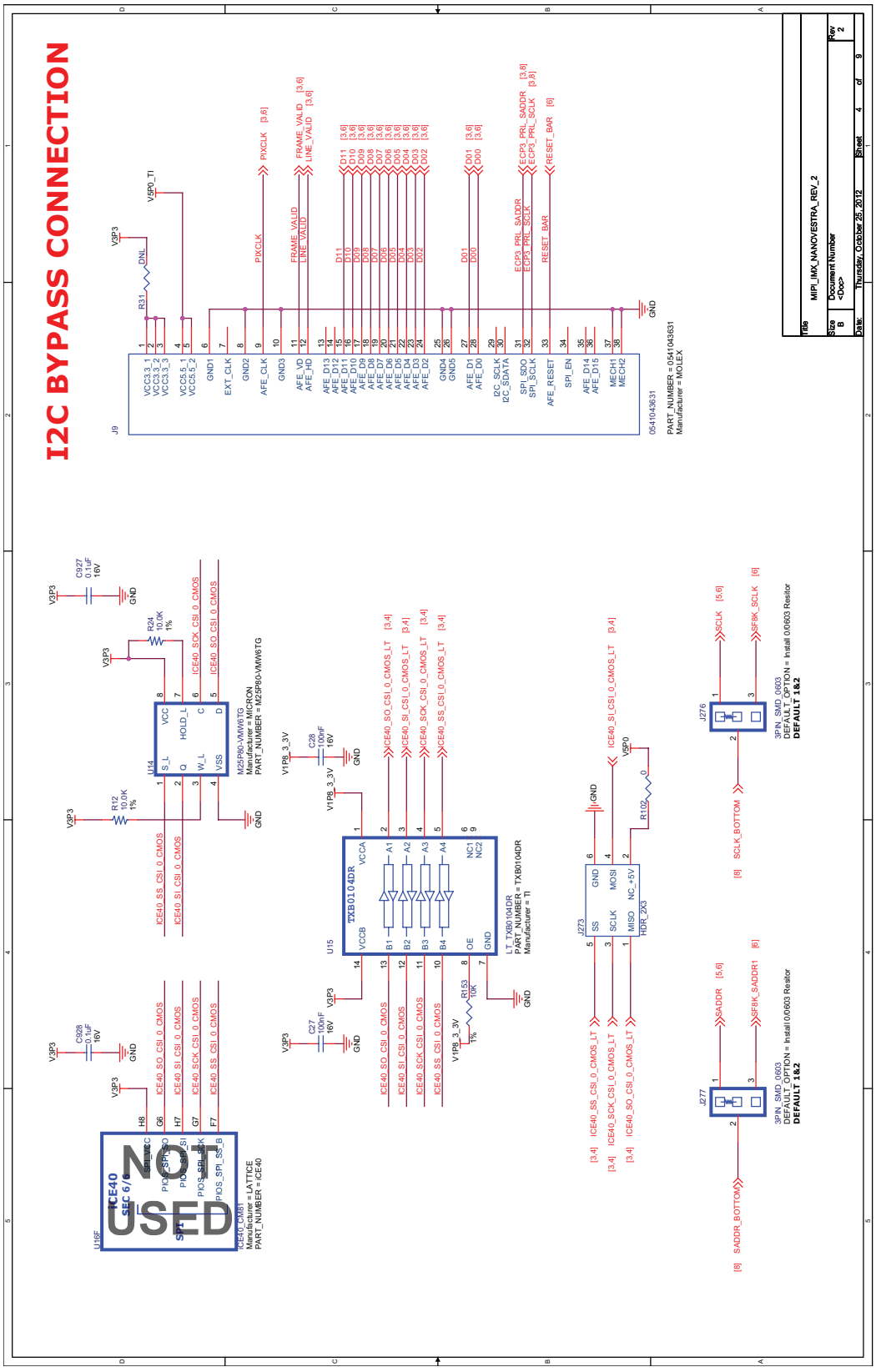
Block Diagram



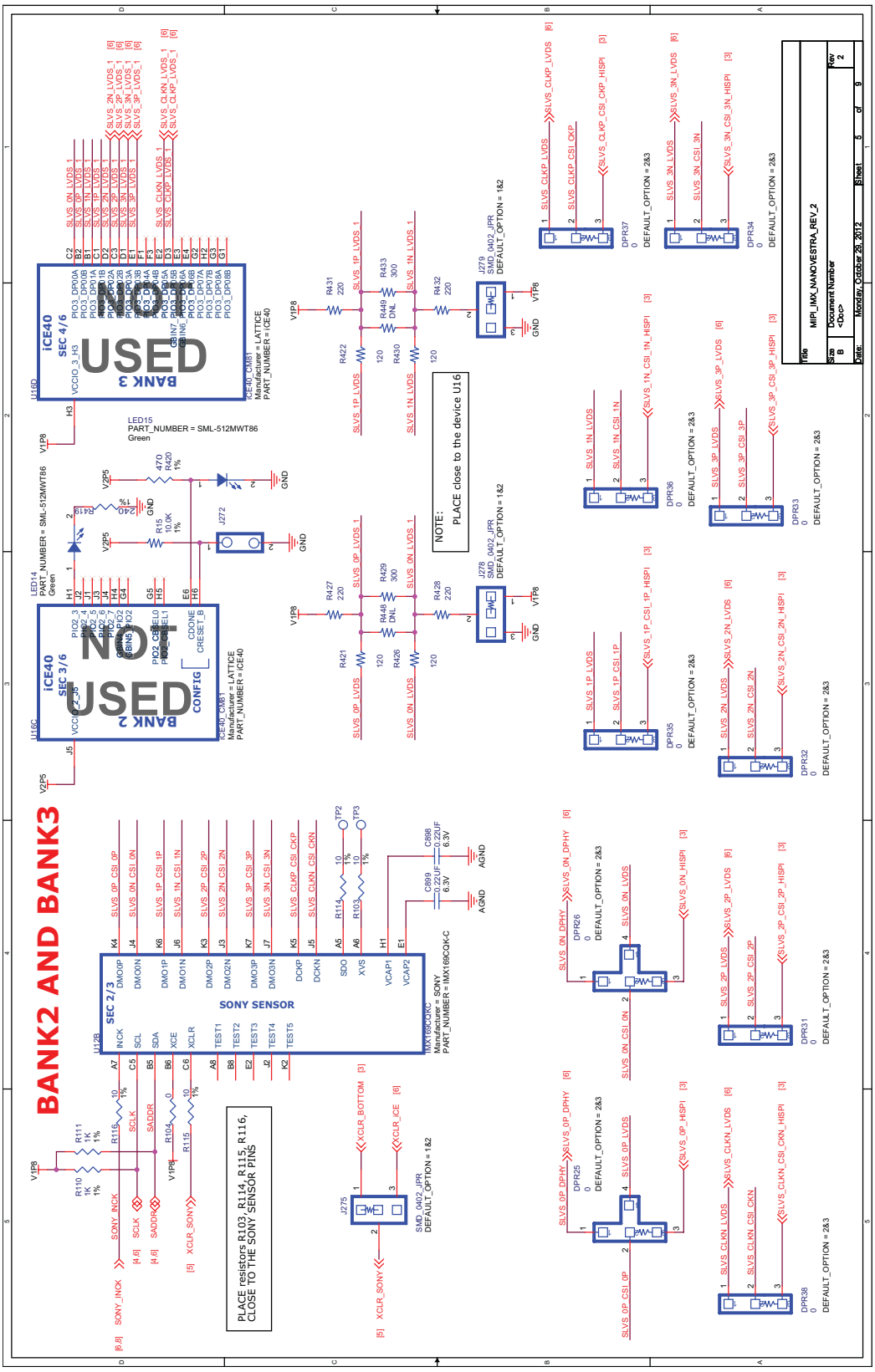
Bottom Conn Connections



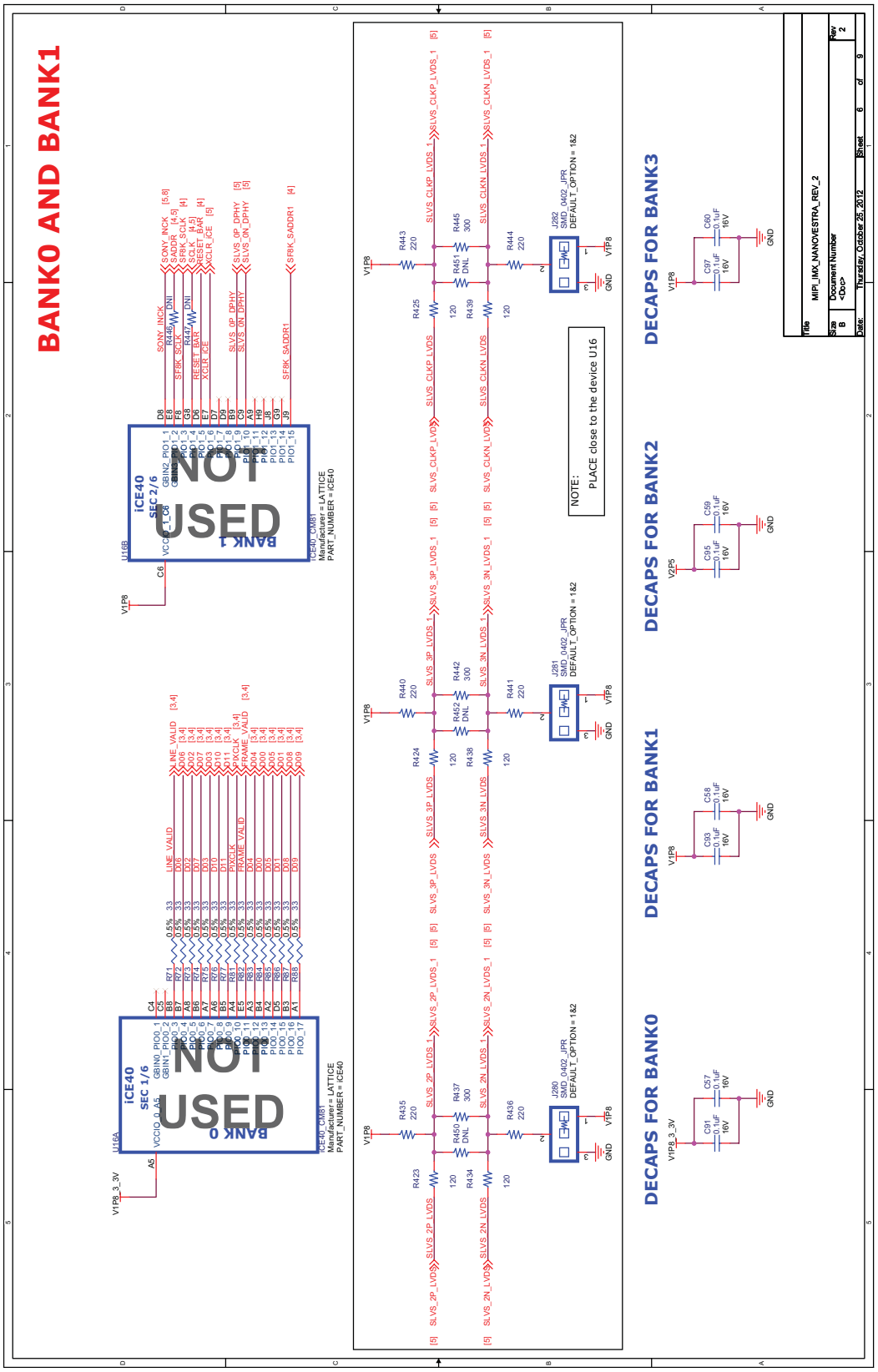
12C Bypass Connection



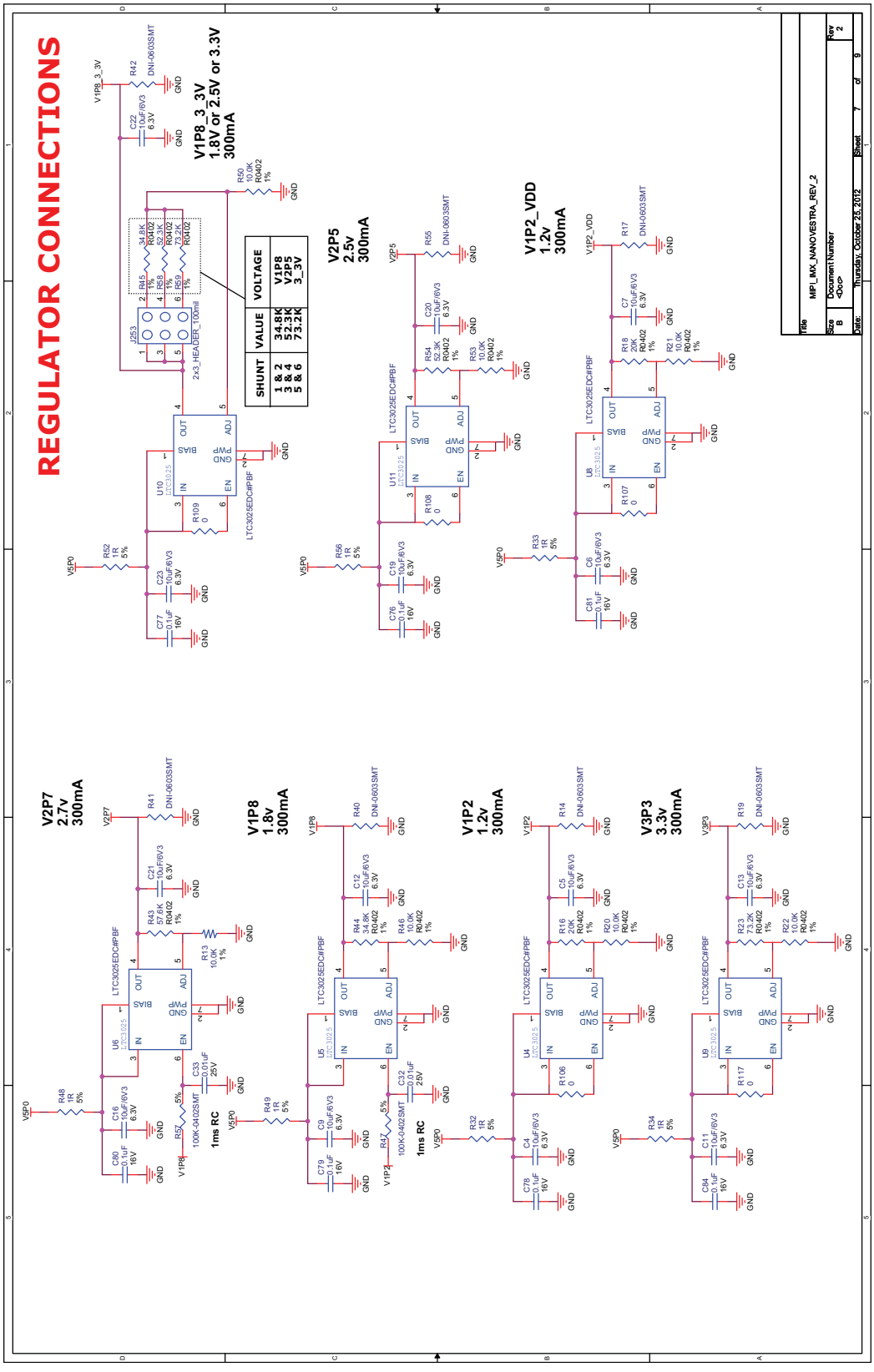
Bank2 and Bank3



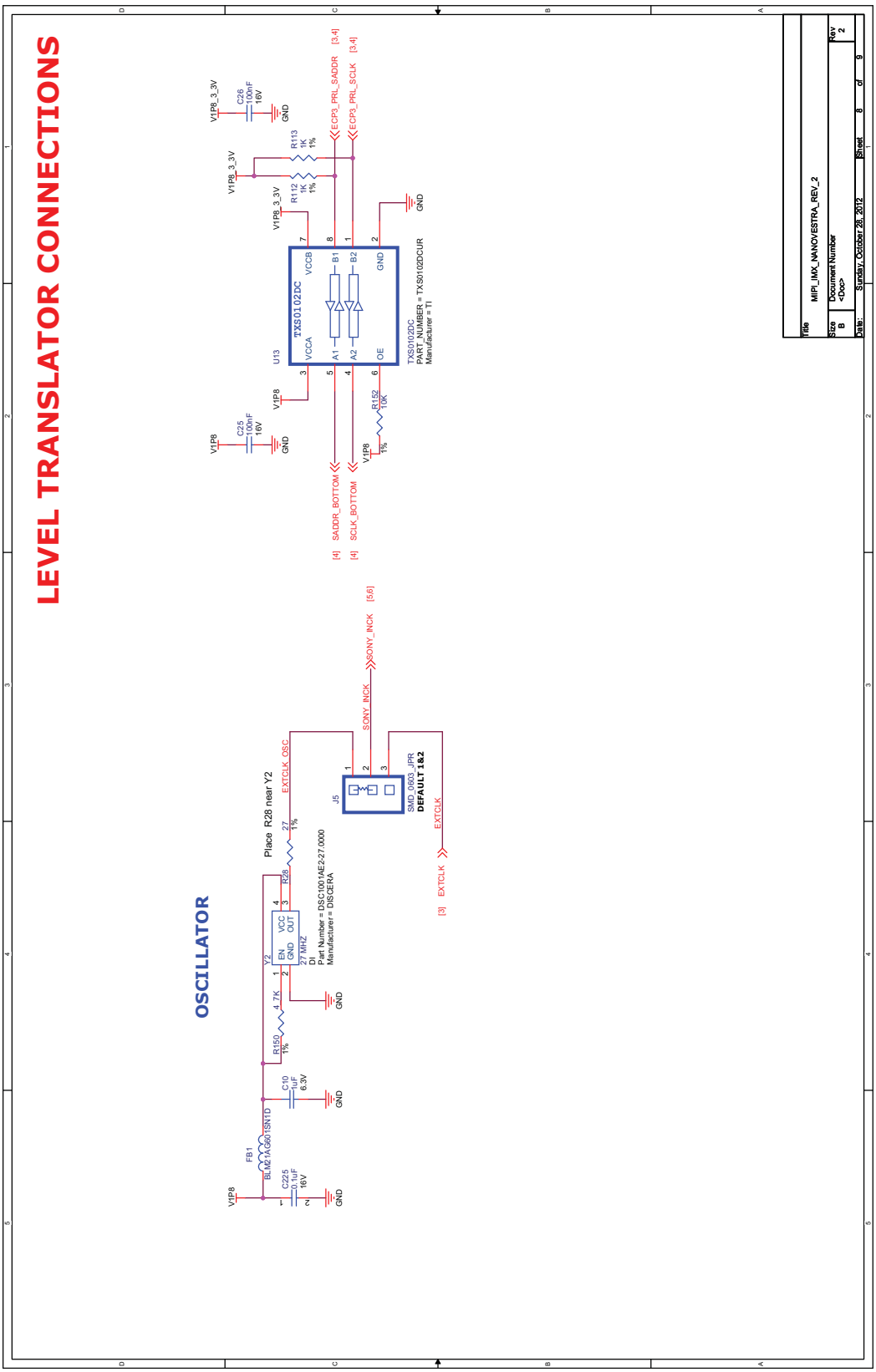
Bank0 and Bank1



Regulator Connections



Level Translator Connections



Sensor Power and Decaps