High Performance Dual PWM Microstepping Controller

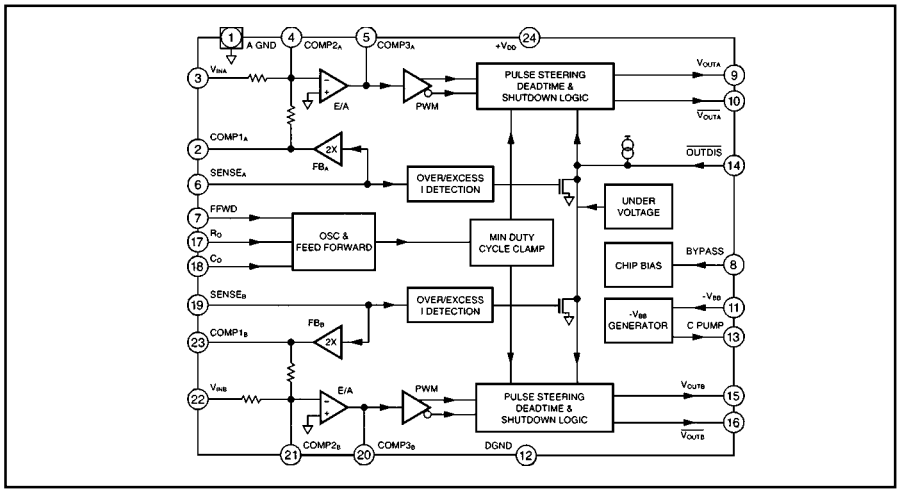
Type	Package	Temperature Range
IXMS150 PSI	24-Pin Skinny DIP	-40°C to +85°C

The IXMS150 is a high performance monolithic 2-channel PWM controller. Implemented in CMOS, the low power IXMS150 precisely controls the current in each of two separate power H-bridge drivers using unique sampling and signal processing techniques. Each channel contains an error amplifier, PWM, feedback amplifier, and protection circuitry. Protection features include over/excess current shutdown, min/max duty cycle clamp, under voltage lockout, dead time insertion, and a shutdown input for over-temp or other external fault circuitry. Other features include a common oscillator, feedforward circuit for motor supply compensation, and an onchip negative bias generator.

The IXMS150 has been optimized for microstep control of two phase step motors. Due to its high level of accuracy, the IXMS150 will allow a designer to implement a control system with a resolution in excess of 250 microsteps per step, or 50,000 steps per revolution with a 200 step per revolution step motor. The IXMS150 greatly improves positioning accuracy and virtually eliminates low speed velocity ripple and resonance effects at a fraction of the cost of a board level microstepping system.

Other applications which the IXMS150 is designed for include control of two single-phase (DC) motors or control of synchronous reluctance motors. The IXMS150 is ideal for robotics, printers, plotters, and x-y tables and can facilitate the construction of very sophisticated positioning control systems while significantly reducing component cost, board space, design time and systems cost.

Block diagram of IXMS 150



Symbol	Definition	Max. Ratings	
V_{DD}	Supply voltage	-0.3...15	V
	Operating range	10.8...13.2	V
	Common-mode-range	-15...15	V
	Differential Input voltage ✶	±30	V
V_{IN}	Input voltage ✶	-15...15	V
V_O	Output voltage	-0.3...V_{DD}+0.3	V
P_D	Maximum power dissipation	500	mW
T_A	Ambient temperature range	-40...85	°C
T_{stg}	Storage temperature range	-55...125	°C

✶ Input voltage may not exceed either supply rail by more than 0.3 V at any time.
IXYS reserves the right to change limits, test conditions and dimensions.

Features

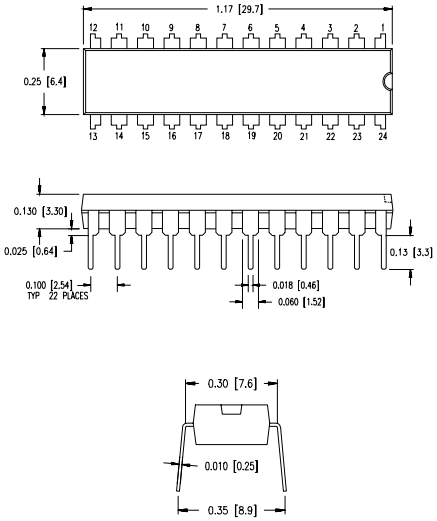
- Two complete, synchronous PWMs
- Command input range ±2.0 V full scale
- ±0.625 V full scale current feedback signal
- 1% gain matching between channels without external trim
- 1.6% gain linearity
- Feedforward to compensate for motor supply variations
- Only one sense resistor per H-bridge needed
- Onboard two level current limiting
- Undervoltage lockout assures proper behavior on power up and power down
- Enable input for external over temperature or fault circuit input
- Duty cycles limited for AC coupled gate drive
- Wide range of built in dead time.
- On board negative power supply generator
- Single +12 V supply operation
- 24-pin DIP package

Applications

- Full, half quarter, or microstepping 2-phase step motor position controller
- Dual DC servo motor torque controller
- Solenoid actuator force controller
- General 2-channel current-commanded PWM control

Symbol	Definition/Condition			Characteristic Values (V_{DD} = 12 V, T_A = 25°C unless otherwise specified) min.	typ.	max.	
Oscillator							
f_{OSC}	Frequency	C_o		10		400	kHz
$V_{A(p-p)}$	Amplitude		FFWD = OPEN		7		V
Z_{OUT}	Output Impedance		± I_{OUT} = 400 µA		2.5		mΩ
	Resistance Range	R_o		15		100	kΩ
	Capacitance Range	C_o		100		2000	pF
Feed Forward							
V_{FFWD}	Feedforward Voltage		FFWD = Open		3.5		V
Z_{INFF}	Impedance to AGND			25	45		kΩ
Analog Inputs							
V_{FS}	Input FullScale	V_{INA} V_{INB}	DC			±2	V
Z_{IN1}	V_{IN} to $Comp_2$ Impedance		DC	20	32		kΩ
Z_{IN2}	$Comp_1$ to $Comp_2$ Impedance		DC	12	20		kΩ
Sense Inputs		$SENSE_A$					
V_{SENSE}	Full Scale Input	$SENSE_B$	DC			±0.625	V
Z_{INS}	Input Impedance		DC	100	200		kΩ
Protection Circuit		$SENSE_A$					
V_{OV-1}	Over Current Voltage	$SENSE_B$		0.8	0.95	1.0	V
t_{OV-1}	Reset Pulse Width			0.5	1		µs
V_{EX-1}	Excess Current Voltage			3.45	3.6	3.75	V
t_{EX-1}	Reset Pulse Width				300		ns
Under Voltage							
V_{UV}	Minimum V_{DD}	$\overline{OUTDIS}$		7.5	8	8.5	V
I_{IH}	Input High Current		V_{IH} = 11.5 V		100		µA
I_{IL}	Input Low Current		V_{IL} = 0.5 V		1.8		mA
Outputs							
V_{OH}	Output High Voltage	V_{OUTA}, $\overline{V_{OUTA}}$	I_{OH} = -10 mA	8.0	11.2		V
V_{OL}	Output Low Voltage	V_{OUTB}, $\overline{V_{OUTB}}$	I_{OL} = 10 mA		0.8	1.1	V
t_r	Rise Time		C_L = 100 pF		35	50	ns
t_f	Fall Time		C_L = 100 pF		35	50	ns
T_{DT}	Dead-Time		C_o = 180 pF	200	300	450	ns
T_{MIN}	Minimum Pulse Width		C_p = 30 pF	0.6	0.8	1.5	µs
VBB Generator							
V_{BBmin}	Minimum Negative Bias	V_{BB}	$\overline{OUTDIS}$ = V_{DD}	-1.4	-1.9		V
V_{BB}	Negative Bias Voltage		I_{OUT} = -3 mA	-2.1	-2.4		V
V_{REG}	Load Regulation		f_{OSC} = 100 kHz		60		mV
V_{OH}	Output High Volt.	C_{PUMP}	I_{OH} = -10 mA		11.2		V
V_{OL}	Output Low Volt.		I_{OL} = 32 mA		0.8		V
Supply							
I_{DD1}	Idle Current	V_{DD}	V_{IN} = 0		16	26	mA
I_{DD2}	Operating Current		f_{OSC} = 100 kHz		15	45	mA
V_{BYPASS}	Bypass Voltage	BYPASS		5.9		16.1	V
Z_{INBP}	Impedance to AGND			9	16		kΩ

Dimensions in inch (1" = 25.4 mm)
24-Pin Skinny DIP



Pin Description IXMS 150

Nomenclature of Dual PWM Microstepping Controller

Sym. Pin Description

Sym.	Pin	Description
AGND	1	Analog Ground
COMP	2, 4, 5, 20, 21, 23	Analog Compensation (see application notes for recommendations).
VIN	3, 22	Analog Input: The analog input range is ± 2 V. A low output im pedance voltage source should drive these pins. The input is greater than 20 kΩ.
SENSE	6, 19	Analog Sense: Each of the phases sense resistors are connected to these pins. Input range is +0.625 V.
FFWD	7	FFWD, for Motor High Voltage Compensation: A voltage on this pin sets the oscillator amplitude. Input range = 0.9-4 V (see application notes for recommendations).
BY-PASS	8	Filter Cap: A capacitor on this pin provides filtering to the internal bias network.
VOUT	9, 10, 15, 16	Output Stage: To drive buffered power MOSFET H-Bridge.
VBB	11	Negative Bias Generator Output: For internal use by the IXMS 150.
DGND	12	Digital Ground
CPUMP	13	Charge Pump Capacitor: Used by the internal Negative Bias Generator.
$\overline{\text{OUTDIS}}$	14	Digital ENABLE input and STATUS output: Forcing this pin low causes pins 9, 10, 15, and 16 to go low, disabling the H-bridge. When uses as an output, a low state on this pin indicates an over current, excess current, or insufficient $+V_{DD}$ or V_{BB} error condition.
R_O, C_O	17, 18	Oscillator Frequency and Dead-time set: Independent adjustment can be made to the oscillator frequency and dead-time (see applications notes).
VDD	24	Positive Supply Voltage

* Pin numbers in parantheses are associated with channel B.

IXMS 150 PS I (Example)

IX — IXYS

MS 150 — Dual PWM Controller

Package Type

PS — Plastic Skinny DIP

Temperature Range

I — Industrial

Functional Description

Introduction

The IXMS150 is designed with monolithic CMOS technology. The IC is primarily intended for use with two-phase step motors in the microstepping mode but may also be used for control of two DC motors, audio amplifiers, or any application requiring two synchronized PWMs. The IXMS150 simultaneously controls the currents in each of two separate H-bridges. This device utilizes both analog and digital functions.

The IC has five fundamental sections: (1) oscillator and feedforward circuitry, (2) analog section for control of the motor currents, (3) a protection network to protect the H-bridges and the motor from abnormal conditions, (4) the digital PWM logic for the control signals, and (5) the power supply section which includes a negative bias generator.

Oscillator

The IXMS150 contains an internal oscillator which is controlled by adjusting the values of R_O and C_O. These two components determine the switching frequency, amount of dead time, and the minimum pulse width at output pins 9, 10, 15 and 16. The minimum and maximum values of R_O and C_O are given in the Electrical Characteristics.

The oscillator also sets the frequency of the charge pump circuit in the internal negative bias generator (V_{BB}). At lower frequencies (<40 kHz) the value of CPUMP must be increased to assure proper operation.

Feedforward Compansation

In all fixed frequency PWM control systems open loop gain, motor current slew rate, and motor current ripple are proportional to the motor supply voltage. Gain variations due to supply voltage changes complicate the design of such systems and restrict their bandwidth to the minimum worst case condition. For this reason, an advanced adaptive compensation scheme is built-in using a feedforward technique. This feature has been designed such that open loop gain is inversely proportional to the voltage applied to the FFWD pin, normally a fraction of the motor supply. As a result, open loop gain can be made independent of the high voltage supply and system bandwidth can be maximized.

Analog Section

The analog section of each channel of the IXMS150 consists of a signal processor and an error amplifier. The signal processor is required since the voltage developed across the sense resistor often contains transients associated with the switching characteristics of the power devices. These transients need to be properly filtered for the system to operate with the desired degree of precision. Because of this, the IXMS150 uses proprietary analog and digital signal processing techniques that sense the true average phase currents. Since this requires only one sense resistor per H-bridge it avoids mismatches in charge/discharge currents associated with two sense resistor per H-bridge topologies.

The instantaneous difference between the motor current and the control input is integrated via the E/A amp and fed to the PWM comparator to generate the appropriate signals for the H-bridges. External compensation of the input and sense signals is provided for via the comp1, comp2 and comp3 pins.

Protection Circuitry

The IC has a two-level Over/Excess Current protection circuit. Maximum current is represented as 0.625 V at the SENSE input. If the SENSE voltage exceeds 0.9 volts for more than one microsecond, the switching outputs (VOUT) and $\overline{\text{OUTDIS}}$ will be forced low. This represents a current that is 40 % beyond full scale. If the SENSE voltage exceeds 3.6 V, these outputs will be forced low immediately. This represents a current that is 500% beyond full scale. The time delay on the lower level of overcurrent avoids erroneous shutdowns as a result of noise spikes that are coupled from the motor's H-bridges. Note that the threshold voltages cited here assume a supply of +12 V.

Undervoltage Lockout

A third protection mechanism is the Under-Voltage Lockout. It assures proper behavior on power-up and power-down and avoids high power dissipation in the H-bridge due to insufficient gate voltage. It uses a zener for reference and has a trip point set at 8 V. It will also check to make sure there is sufficient negative bias to insure proper operation. This is typically -1.6 V. OUTDIS will be held low by the UV Lockout circuit until V_{BB} and V_{DD} reach these values.

Output Disable Feature

To enable external over-temperature protection, the output disable pin ($\overline{\text{OUTDIS}}$) is available on the IXMS150. When pulled low this disables the output by forcing all output pins low. The same output disable input pin is also used as a status output. When it is pulled low by the internal circuitry it indicates an error condition such as undervoltage (V_{DD}), insufficient negative bias voltage (V_{BB}) or over/excess current. This can be used as a status indicator in smart systems.

PWM Section

The PWM comparator generates two complementary signals based on the output of the error amplifier. Dead-time is then added which is adjusted by the selection of the external oscillator capacitor. There is also a minimum duty cycle clamp circuit that allows the use of an AC coupled H-bridge.

Supply Section

The main power supply (V_{DD}) is applied to pin 24. This is typically +12 V. Internal bias circuitry presents a $V_{DD}/2$ reference voltage at pin 8, BYPASS. A 0.1 µF capacitor should be connected from pin 8 to analog ground for noise immunity.

Negative Bias Generator

The IXMS150 samples both positive and negative voltages at the motor sense feedback resistor. In addition, since errors in the input current around zero are a major contributor to microstep positioning error, the input control range is bipolar and specified as ±2 V full scale. For these reasons it is desirable to have both positive and negative power supplies. In order to enable single 12 V supply operation, a negative voltage generator and regulator are built into the IC. This is a charge pump circuit whose frequency is that of the onboard oscillator. It utilizes an external pair of capacitors and diodes to generate a negative bias equal to $-V_{DD}/5$ or approximately -2.4 V for V_{DD} = 12 V.

Application Information

Introduction

The advantages of step motors are well known. They may be operated in an open loop fashion, the accuracy of which is mostly dependent on the mechanical accuracy of the motor. They move in quantized increments (steps) which lends them easily to digitally controlled motion systems. In addition, their drive signals are square wave in nature and are therefore easily generated with relatively high efficiency due to their ON/OFF characteristics.

But step motors are not free of problems. Their large pulse drive waveforms create mechanical forces which excite and aggravate the mechanical resonances in the system. These are load dependent and difficult to control since step motors have very little damping of their own. At resonance a step motor system is likely to lose synchronization and therefore skip or gain a step. Being an open loop system, this would imply loss of position information and would be unacceptable. A common method of solving this problem is to avoid the band of resonance frequencies altogether, but this might put severe limitations on system performance. Steppers have 200 steps per revolution or 1.8 degrees per step. The highest resolution commercially available steppers have 400 steps per revolution or 0.9 degrees per step.

Microstepping Mode

One way to circumvent the problems associated with step motors while still retaining their open loop advantages is to use them in the microstepping mode. In this mode each of the steps is subdivided into smaller steps or “microsteps". Applying currents to both phases of the motor creates a torque phaser which is proportional to the vector sum of both currents. When the phasor completes one “turn” (360 electrical degrees), the motor moves exactly four full steps or one torque cycle. Similarly, when that phasor moves 22.5 electrical degrees the motor will move (22.5/90) • 100 = 25 % of a full step. Thus the position of the motor is determined by the angle of the torque phasor. When used with an appropriate motor a positioning accuracy of 2 % of a full step can be achieved, equaling 0.036 degrees for a 200 full steps per revolution motor. In this manner the motor can be positioned to any arbitrary angle. A common way to control the angle of the torque phasor is by applying to the motor’s phases two periodic waveforms shifted by 90 electrical degrees.

Let the phase current equations be:

$i_A = I_O \cdot \cos \theta e$ (1)
$i_B = I_O \cdot \sin \theta e$ (2)

Note that θe is the electrical position.

The resulting torque generated by the corresponding phases would then be:

$T_A = K_0 \cdot i_A = K_0 \cdot I_0 \cdot \cos \theta e$ (3)
$T_B = K_0 \cdot i_B = K_0 \cdot I_0 \cdot \sin \theta e$ (4)

where K_0 is the torque constant of the motor. Substituting Eqs. (1), (2) into (3), (4) and doing vector summation the resulting total generated torque measured on the motor shaft is given by:

$T_g = K_0 \cdot I_0$ (5)

Note that in this case we have zero torque ripple.

Using this technique one can theoretically achieve infinite resolution with any step motor. Since the drive current waveforms are sinusoidal instead of square, the step to step oscillations are eliminated and the associated velocity ripple. This greatly improves performance at low rotational speeds and helps avoid resonance problems. In an actual application, the extent to which these things are true depends on how the two sinusoidal reference waveforms are generated.

Seemingly we have lost the quantized motion feature of a stepper when used in this mode. This can be regained by defining the term microsteps per step. Each full step is subdivided into microsteps by applying to the motor’s phases those intermediate current levels for which their vector sum tracks the circle of Fig. 2 and divides the full step (90 electrical degrees) into the require number of microsteps. An example of the required phase currents for full step and four microstep per step operation are shown in Fig. 1 and 2 respectively.

Phase Current Matching Requirements

Assuming microstepping is being used for resolution improvement and not as a resonance avoidance technique, a step motor can be selected knowing the torque needed, its specified step

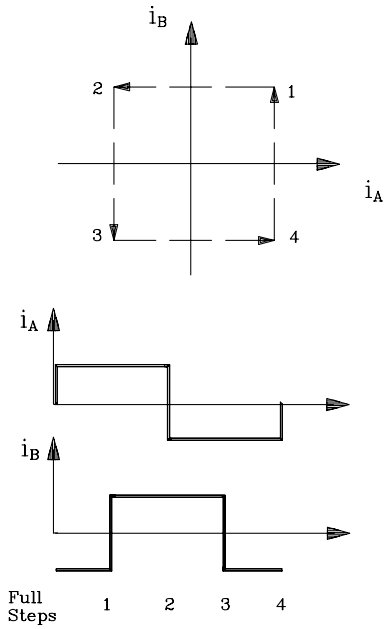


Fig. 1 Full Step Drive Waveforms

accuracy, and the required resolution or the number of microsteps per step. Next, one must determine the accuracy required of the phase currents to maintain the accuracy of the complete system. Equations (1) - (4) clearly indicate that errors in the absolute value or phase of the phase currents will impact positioning accuracy. Another observation is that by keeping the ratio of the phase currents i_A/i_B constant, errors in their value will result

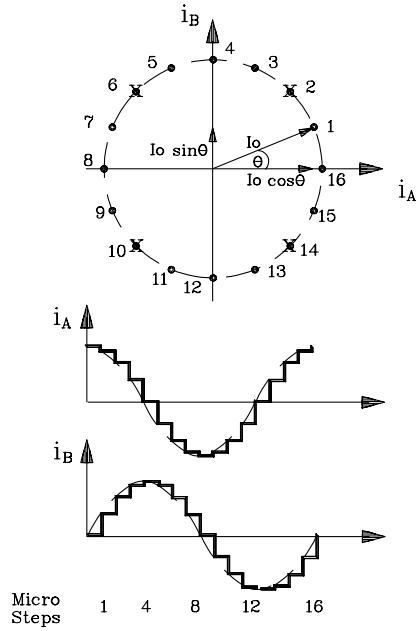


Fig. 2 Four Microstep per Step Drive Waveforms

in torque value errors but no positioning errors. The question is, what is the upper bound on the current errors in order to keep the position error within some given angle $\Delta\theta$.

Referring to Fig. 3, assume the required currents i_A, i_B are given by Equations (1), (2) respectively such that their vector sum points to position P. Let the phase currents vary by a small amount such that their vector sum lies within a circle centered at point P and having the radius i, as indicated in Fig. 3.

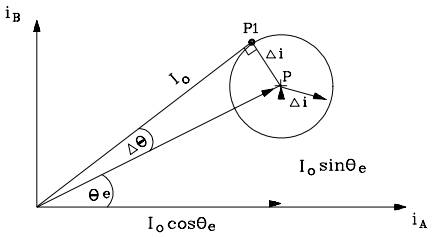


Fig. 3 Effect of Current Errors on Position

If follows that the worst case position error occurs for the cases where the vector sum is tangent to the circle such as point P_1, at which:

$\tan(\Delta\theta) = \Delta i / I_0$ (6)

For instance, to keep position error to less than 1% of a full step, the electrical angular error would be:

$\Delta\theta = 0.01 \cdot 90° = 0.9°$ (7)

This is assuming there are 90 electrical degrees for a full step. Therefore total current error must be:

$i/I_0 = \tan(\Delta\theta) = 0.016$ or 1.6 %) (8)

Thus the current error must be kept to less than 1.6 % of full scale or peak current at each phase for 1 % maximum position error. This upper bound on error includes all error sources such as zero offset errors and full scale matching errors. Another interesting observation is that in the vicinity of a full step (i.e., $\theta e = 0$), the phase having the bigger impact on position error is the one carrying the smaller current through it. This has a strong impact on input waveform generation.

Input waveform generation

It has been shown that the two input signals, VIN_A and VIN_B, are sinusoidal and 90° out of phase. This may be accomplished by using two look-up

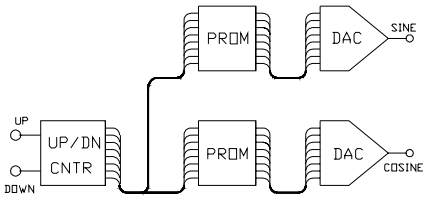


Fig. 4 Simple Reference Waveform Generator

tables stored in ROM and two DACs per Fig. 4. An up/down counter may be used to generate the appropriate address locations for the ROMs and the data outputs used to control the DACs. The user then need only supply up or down pulses to the counter to control the IXMS150 and hence the motor.

In higher performance systems a microprocessor may be used in place of the counter and the ROMs. The micro can perform the look-up function and calculate the appropriate system responses, velocity profiles, etc. necessary for total system operation. An example of this configuration is shown in Fig. 5.

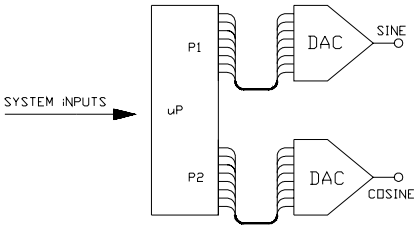


Fig. 5 Microprocessor Based Referenced Waveform Generator

Current Sensing Considerations

Most commercially available monolithic PWM controllers monitor and control the peak of the phase current by comparing the voltage across the sense resistor with a ramp voltage. This approach assumes that the ripple current is fixed in amplitude. Results shown later clearly indicate the variation of the ripple current with frequency. But even in fixed frequency systems the ripple current is directly proportional to the motor supply voltage and to the back EMF voltage of the motor. Ripple current is not insignificant compared to the full scale current and therefore cannot be neglected in a precision system. In addition, there are transients associated with the turn on and turn off characteristics of the power devices in the H-bridge that must be properly filtered if the system is to operate with the desired degree of precision.

This presents a significant engineering challenge that has been solved by IXYS's design team. Using proprietary analog and digital signal processing techniques, IXYS has developed a control system that measures the true average phase currents. Requiring only one sense resistor per H-bridge, this technique avoids errors due to mismatches in charge/discharge currents associated with using one sense resistor on each leg of the H-bridge. This improves system performance as well as minimizing component count. The sense resistor for each H-bridge should be selected based on the required peak motor current:

$R_S = 0.625\ V/I_{mpk}$ (9)

The voltage developed across this resistor is then applied to the corresponding sense input for each H-bridge.

Negative bias Generator

One of today's cost cutting trends is to minimize the number of power supplies, implying single supply operation for the control section. Yet the current feedback and reference inputs are bipolar signals. Level shifting has been used for the reference input in the past, but that can not be easily done for the feedback signal without impacting accuracy or efficiency. In practice one finds that in order to generate true zero voltage having low impedance drive there must be a negative power supply. Otherwise there will be a tradeoff sacrificing accuracy for simpler system design.

For these reasons the approach selected by IXYS was different. Taking advantage of our CMOS design, we opted to build into the chip a negative bias generator. This does put stringent demands on noise coupling but results in the most flexible system having the highest possible accuracy. The built in charge pump circuit requires two capacitors and two diodes to be added externally. The recommended component values for an oscillator frequency of 100 kHz are given below.

C1 = 0.047 µF
C2 = 100 µF
D1 = D2 = 1N4148
Note: $V_{BB} = -(V_{DD}/5)$

Use the formula
C2 = 100 µF · 100 kHz/f_{OSC}
for other frequencies.

With V_{DD} = 12 V and an oscillator frequency of 100 kHz, the bias generator should be able to source 3 mA at -2.4 V using these component values. This capability may be used to power other external circuitry as long as there is sufficient remaining negative bias to allow the IXMS150 to operate properly.

Impact of PWM Frequency on System Operation

PWM switching frequency has a pronounced effect on ripple current through the motor windings, the resulting eddy current losses in the motor, and system efficiency. As expected, motor current ripple goes down as frequency increases and therefore losses resulting from ripple currents are also reduced. Switching frequency also impacts losses in the power stage. These losses are associated with the energy necessary to turn on and off the power MOSFETs and are proportional to the switching frequency. In addition, the switching frequency has a limiting effect on maximum current loop bandwidth and therefore system bandwidth and therefore system bandwidth and maximum motor velocity.

Oscillator

The oscillator block diagram is shown in Fig. 6.

The frequency is set by the values of R_O and C_O:

$$f_{OSC} = 1/R_O \bullet (C_O + C_P)) \qquad (10)$$

Note: C_P is a 38 pF (typ.) internal parasitic capacitor.

Feedforward

The amplitude of the oscillator waveform and overall system gain are modulated by the voltage applied to the feedforward pin (FFWD). This is nominally 3.5 V which should be divided down from the motor high voltage supply. This will allow system bandwidth to be maximized by making overall system gain inversely proportional to the motor supply voltage. Refer to Fig. 7 for an example of how feedforward is connected to the motor supply. It is recommended that a filter capacitor be connected from FFWD to AGND to filter noise spikes from the motor supply. Its value should be chosen so that the time constant of the capacitor and the parallel combination of R_{ff1} and R_{ff2} is such that switching noise will be filtered but not variations in the motor supply such as 120 Hz ripple, etc.

Minimum Pulse Width

The minimum output pulse width can also be modified by adjusting the oscillator capacitor C_O. The relationship is:

$$t_{pw(min)} = R_{mp} \bullet (C_O + C_p) \qquad (11)$$

Note: R_{mp} is a 3.6 kΩ (typ.) internal resistor, and C_p is a 38 pF (typ.) internal parasitic capacitor.

Dead Time

Dead time is adjusted via the external oscillator capacitor C_O. There is an internal resistor in the dead time circuit as well. The relationship is:

$$t_{DT} = R_{DT} \bullet (C_O + C_p) \qquad (12)$$

Note: R_{DT} is a 1.4 kΩ (typ.) internal resistor and C_p is a 38 pF (typ.) internal parasitic capacitor.

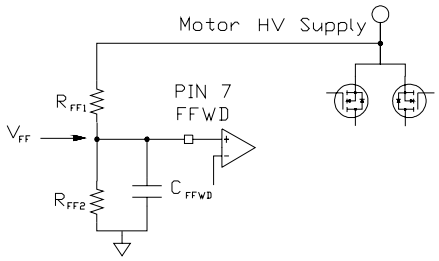


Fig. 7 Feedforward Connection Diagram

Motor Slew Rate Limitations

The maximum motor velocity in a microstepping application is determined by the maximum rate of change of the phase currents. Once this limit is reached the system is “slew rate limited,” at which point the peak undistorted phase current times the frequency of the input command is a fixed value. The theoretical limit for the maximum di/dt of the phase currents is determined by the motor supply voltage and the inductance of the motor:

$$di/dt\ (max) = V_{HV}/L_m \qquad (13)$$

The limit does not take into account the back EMF of the motor, the bandwidth of the current loop driving the motor, or the minimum pulse width. The motor’s back EMF will tend to reduce the voltage applied across the motor windings, effectively reducing the maximum slew rate. The bandwidth of the current loop must also be high enough so as not to degrade system performance.

Non-Circulating Operating Mode

The IXMS150 is designed to control an H-bridge in the non-circulating mode. The equivalent circuit for an H-bridge is shown in Fig. 8. In the non-circulating

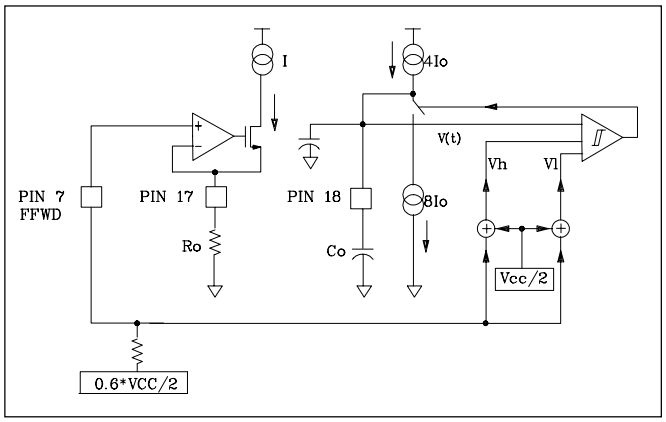


Fig. 6a: Oscillator Block Diagram

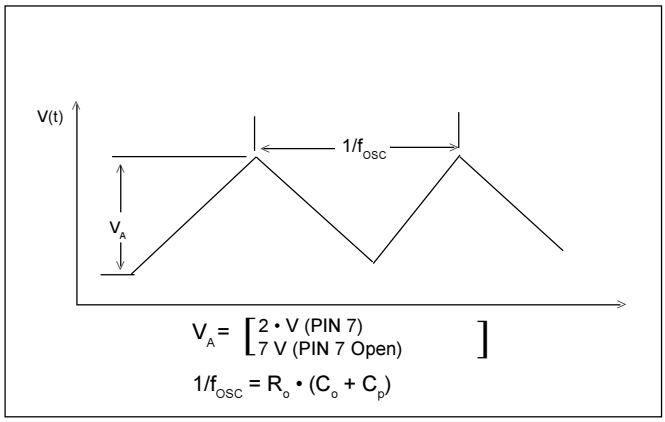


Fig. 6b: Oscillator Waveform Diagram

mode, either SW1 and SW4 are on ($V_m = V_{HV}$) or SW2 + SW3 are on ($V_m = -V_{HV}$). By appropriately controlling the duty cycle of SW1//4 vs. SW2/3, the average motor voltage can be controlled such that:

$V_{m(avg)} = 2 \cdot V_{HV}$ (0.5-DUTY)

Note: DUTY is defined as the duty cycle of V_{OUTA}.
The IXMS150 can now regulate the motor coil current by commanding the voltage level and polarity required.

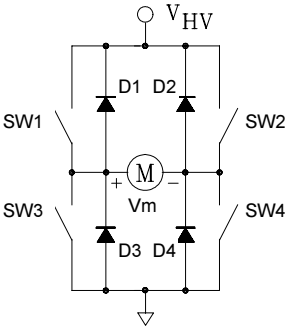


Fig. 8 Simplified H-Bridge Diagram

The Power Stage:
An AC Coupled H-Bridge

Fig. 9 shows the power driver selected for this application. Two of these are required to drive the two phase step motor. This circuit uses two N-channel and two P-channel power MOSFETs as opposed to an all N-channel architecture. The drawback of using P-channel transistors is that they are larger and therefore more expensive than similarly rated N-channel devices. But the advantages are much simplified drive and level shifting circuitry. This results in a lower component count and therefore higher reliability. It also lends itself easily to hybridization. Other advantages of this topology are: a) the high efficiency associated with level shifting by AC coupling since no power is dissipated in the capacitors, and b) the same circuit can be used for motor applications ranging from 12 V to several hundred volts, the only modification being appropriately rated power transistors and coupling capacitors.

A limitation of this circuit is that it cannot be used at duty cycle extremes. This would require one input to be continuously low while the other is continuously high. Eventually the coupling capacitors (C1, C2) would charge up to a voltage that would no longer fully enhance the MOSFETs, with the top two transistors (Q2, Q4) being destroyed due to excessive power dissipation. Therefore one has to limit the duty cycle excursions. The solution selected by IXYS limits the minimum output pulse-width to 0.5 ms, which translates to a duty cycle range of 5 % to 95 % when operating at 100 kHz, or wider at lower frequencies. There is a penalty of slightly limiting the maximum slew rate to (1-2 • Min Duty) of the unrestricted case, which translates to 90 % of the unrestricted maximum slew rate for 100 kHz operation.

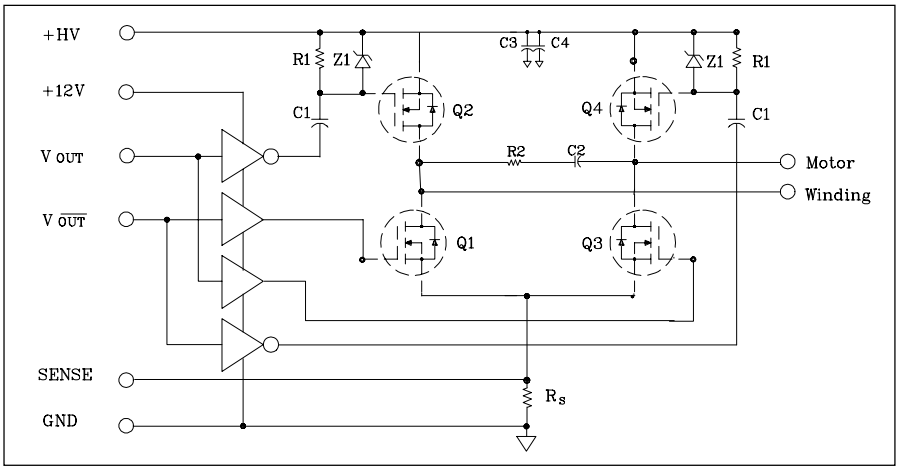


Fig. 9 AC Coupled H-Bridge Diagram

Loop Compensation Information

When used with the appropriate power stage, each channel of the IXMS150 acts as a closed loop transconductance amplifier. As such, it must be properly compensated to guarantee stable operation with a particular motor. The basic elements involved in the current loop are illustrated in Fig. 11a. Referring to Fig. 11b, the loop gain for this system (the product of the forward and feedback gain terms) can be expressed as:

$$G_{loop}(s) = G_{e/a}(s) \cdot K_{pwm} \cdot G_m(s) \cdot G_i(s) \quad (14)$$

where

$G_{e/a}(s)$ = error amplifier gain
K_{pwm} = cascade of pwm and output H-bridge gain

$G_m(s)$ = cascade of motor winding impedance and H-bridge parasitic resistance

$G_i(s)$ = current sense resistor and sampling amplifier gain

The value of each of these terms can be determined from the Laplace transform diagram in Fig. 11b:

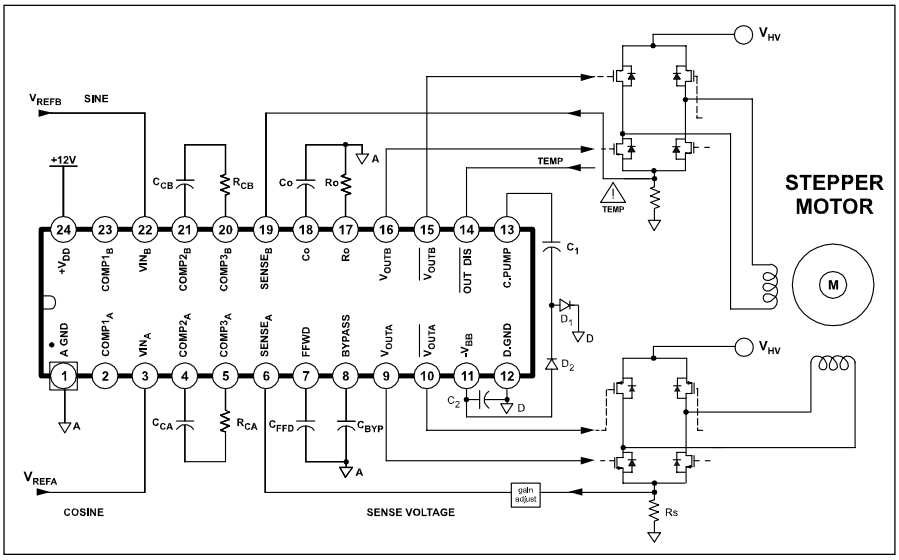


Fig. 10a Simplified Microstepping System

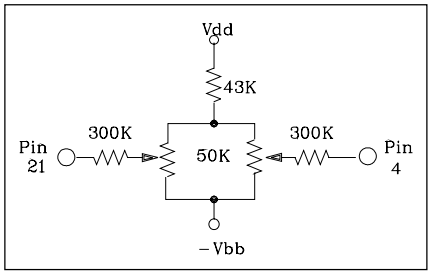


Fig. 10b Input Offset Adjust Circuit

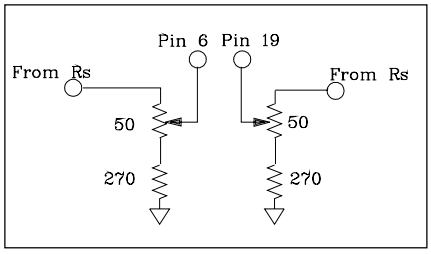


Fig. 10c Gain Adjust Circuit

$G_{e/a}(s) = (1 + sRC)/(sR_2C)$ (15)

$K_{pwm} = 2 \cdot V_{HV}/V_A$ (16)

$G_m(S) = 1/(sL_m + R_m + R_{sw} + R_s)$ (17)

$G_i(s) = 2 \cdot R_s$
(ignoring sampling effects) (18)

where:

R, C = external compensation components

R_2 = internal input resistor, typically 20 kΩ

V_{HV} = motor high voltage power supply

V_A = oscillator amplitude, typically 7 V

L_m = motor inductance

R_m = motor winding resistance

R_{sw} = power switch resistance

R_s = sense resistor

It is very important that the motor inductance value used in the analysis is not the value on the manufacturer's data sheet but rather the value observed in actual operation. The PWM action causes high frequency effects that can change the apparent small signal inductance significantly. These effects are dependent upon voltage as well as current and frequency. It is best to measure the observed current ripple at the motor supply voltage and switching frequency you expect to use and calculate the actual motor inductance using:

$L_m = V_{HV}/((2 \cdot F_{osc})(I_{max}-I_{min}))$ (19)

It is also important to note that both R_m and R_{sw} are temperature dependent. The motor winding resistance can increase by as much as 30 % at high temperatures, and if FETs are used as power devices, R_{sw} can increase to 2.2 times its value at room temperature.

Substituting equations 15 through 18 into equation 14 gives the expanded loop gain equation (eq. 20):

$$G_{loop}(s) = \frac{(1+sRC) \cdot 2Vhv \cdot 1 \cdot 2Rs}{sR_2C \cdot V_A \cdot (sL_m+R_m+R_s+R_{sw})}$$

which can be written as (eq.21):

$$G_{loop}(s) = \frac{4 \cdot V_{HV} \cdot R_s}{V_A(R_m+R_s \cdot R_{sw})} \cdot \frac{(1+RC)}{(sR_2 \cdot C)\,[1+sL_m/R_m+R_s+R_{sw})]}$$

Therefore the poles and zeros of the system are:

pole at DC, with a 0dB intercept of:

$4V_{HV}R_s/[V_AR_2C(R_m + R_s + R_{sw})]$

zero at $1/(R \cdot C)$

pole at $(R_m + R_s + R_{sw})/L_m$

A simple Bode analysis can be performed to provide the necessary information to guarantee the stability of the loop. A stable system will result when the gain crossover occurs at a point where the loop phase shift is less than -180 degrees. The gain crossover point is defined as the frequency where the magnitude of $G_{loop}(s) = 1$ (0dB).

The Bode plot will show two figures of merit that give an indication of the behavior of the closed loop system, gain margin and phase margin. Gain margin is the amount of loop signal attenuation at the point where the loop phase has reached -180 degrees. It is a qualitative measure of how susceptible the loop is to noise outside its bandwidth. Phase margin is the amount of

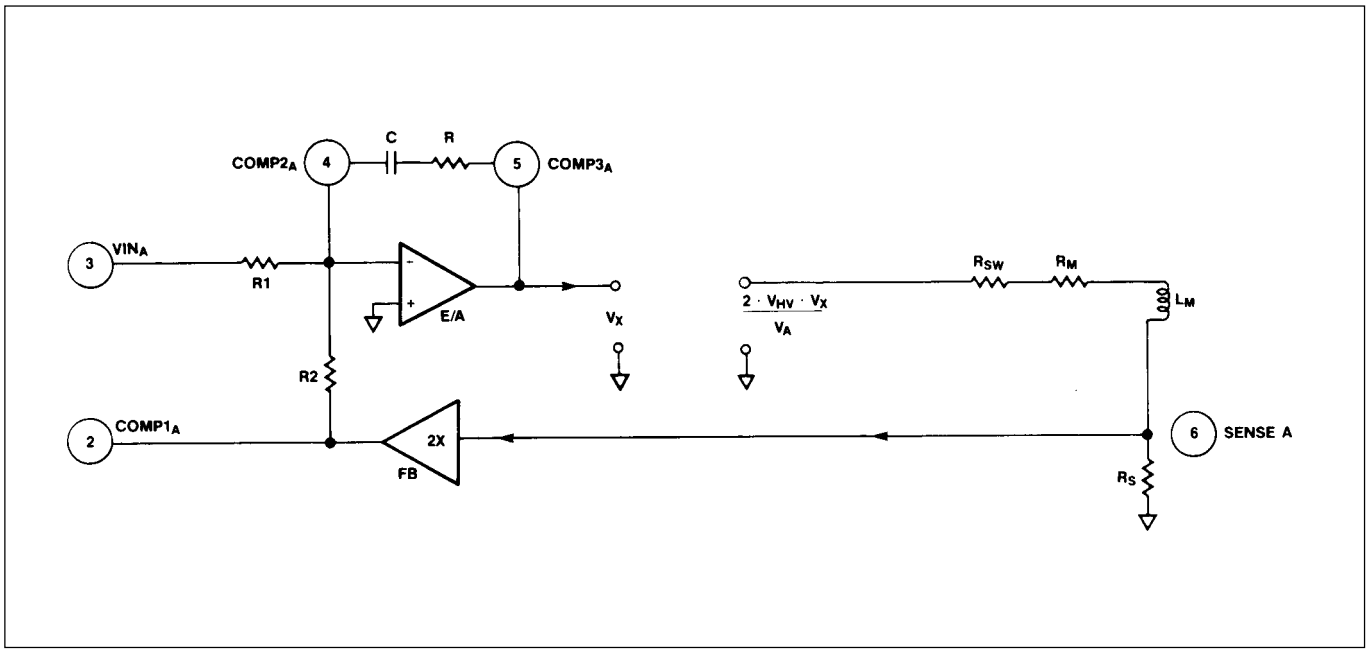


Fig. 11a Loop Compensation Block Diagram

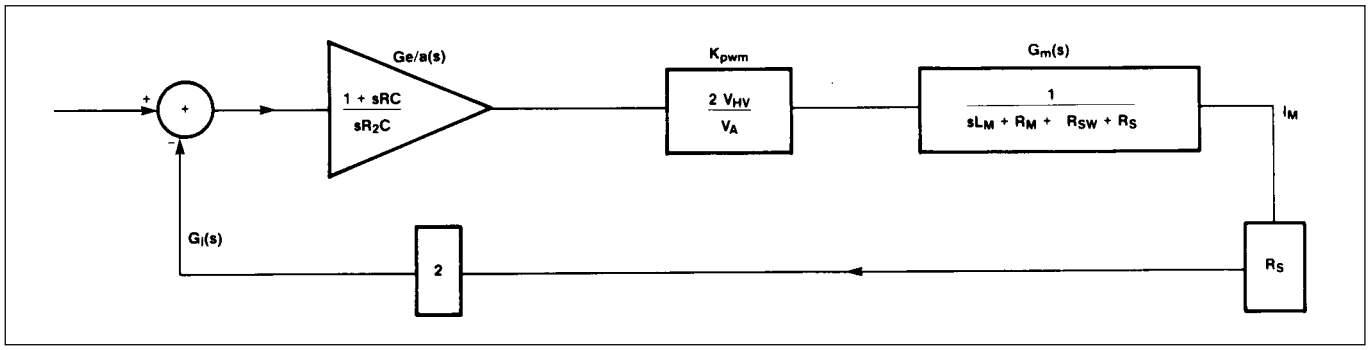
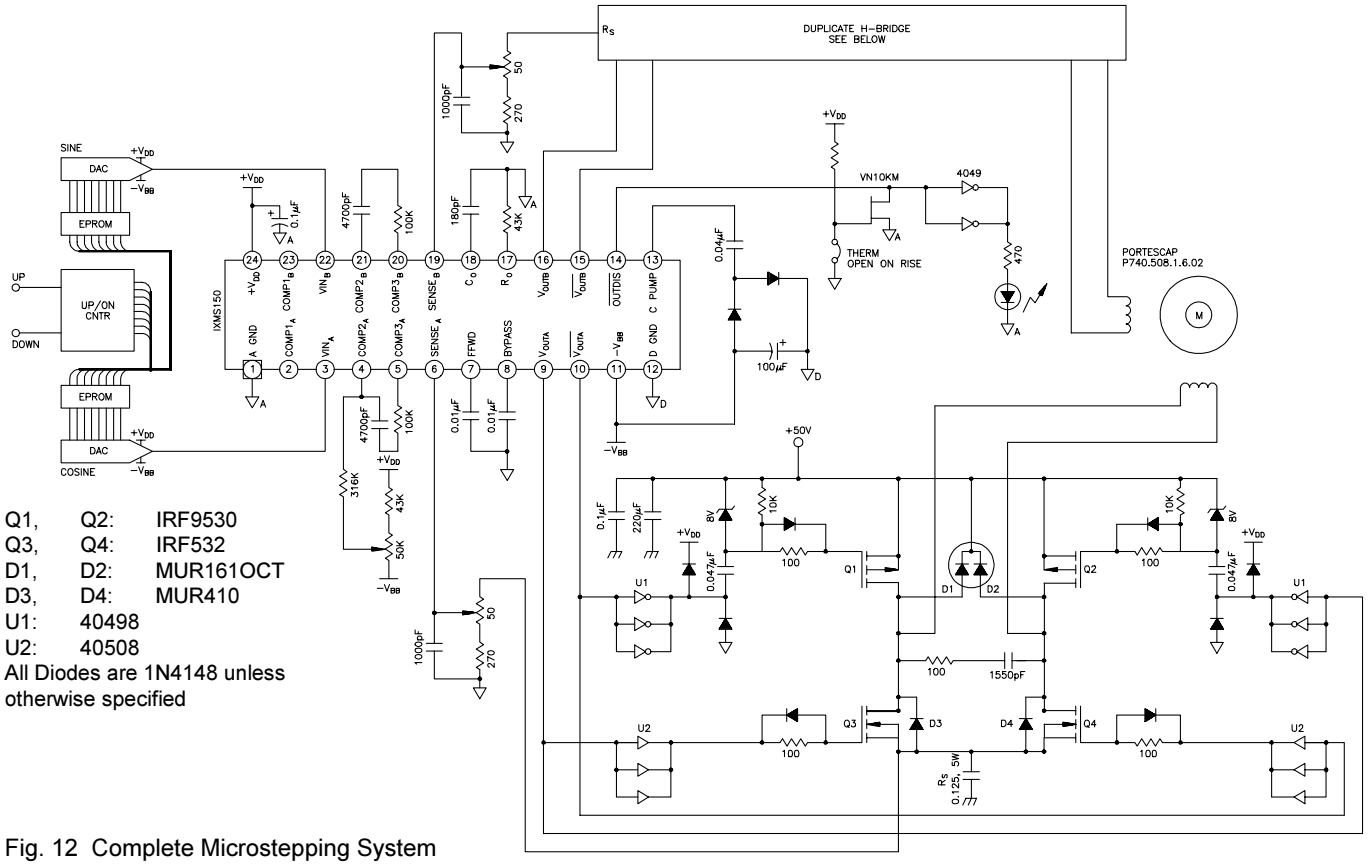


Fig. 11b Simplified laplace transform for stability analysis

phase shift left (i.e., 180 - (loop phase)) at the gain crossover. This number gives the most intuitive feeling for how the loop will respond to perturbations and variations in system parameters. Theoretically, a system with 1 degree of phase margin is stable. However, a step input to a system with small phase margin will cause an underdamped, ringly response or an oscillation that dies out after a long time.

In a step motor, this overshoot and ring in the current waveform is unacceptable. As the phase margin of a system is increased, the response to a step input slows down and the ringing is decreased. The response becomes more damped. In a practical system, the minimum acceptable phase margin is about 30 degrees. More than 90 degrees slows the system response with no significant improvement in stability. 60 degrees is usually considered optimal, if no other constraints exist.

In a PWM motor drive amplifier, there are several additional constraints that apply. Because the levels of voltage and current being switched are so high, synchronous noise appears everywhere and can degrade system performance. It is common to see apparent instabilities that are simply loop amplification of subharmonic switching transient noise. It is important to maintain at least 60 degrees of phase margin and to maintain as much gain margin as is practical. The PWM comparator delays, power stage gate drive delays, and the sampling technique used to generate the current feedback signal also account for significant phase delays when the switching frequency is high, or when the excitation approaches the switching frequency. For these reasons it is usually advisable to design for a calculated 60 to 90 degree phase margin because of the importance of the effects not accounted for in the linearized circuit model.



Q1, Q2: IRF9530
Q3, Q4: IRF532
D1, D2: MUR161OCT
D3, D4: MUR410
U1: 40498
U2: 40508
All Diodes are 1N4148 unless otherwise specified

Fig. 12 Complete Microstepping System