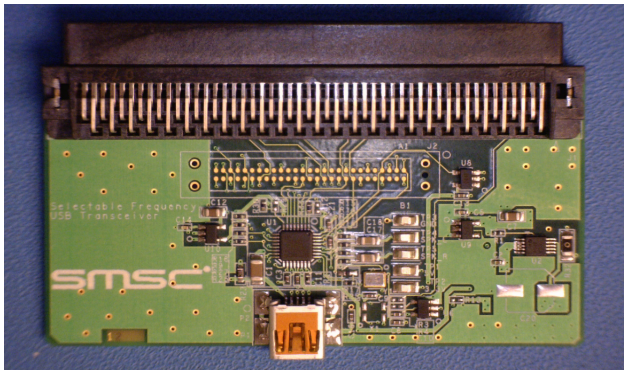
EVB-USB3320 USB Transceiver Evaluation Board User Manual



1 Introduction

This user manual is for the USB3320 USB Transceiver Evaluation Board (EVB) for use with USB3320 products with the integrated USB switch.

The USB3320 features a ULPI interface to support systems with USB Host, Device, or On-the-Go (OTG) capability. The integrated switch can be used to multiplex a Full Speed USB signal or audio signals over the HS USB DP/DM pins. SMSC supplies a complete family of transceiver products to meet the needs of many applications.

2 Overview

The EVB-USB3320 is a Daughter Card designed to plug into a user's test system using a T&MT connector. The card attaches to a USB link layer to create a USB Host, Device, or On-the-Go (OTG) system. The board edge connector meets the UTMI+ Low Pin Interface (ULPI) Standard requirements for the T&MT connector.

A link to the ULPI Working Group Page is available at www.smsc.com or may be obtained from your local FAE. The EVB-USB3320 includes USB3320 packaged silicon and all external components required for the USB transceiver function.

This manual describes PCB assembly PCB-7163AZ.

2.1 Supplying VBUS Voltage

In Host or OTG operation, the EVB-USB3320 must provide 5 Volts on V_{BUS} at the USB connector. The EVB-USB3320 includes a switch that can drive V_{BUS} using the 5 Volt supply that comes from pin 28 of the T&MT connector.

The VBUS switch is controlled by the CPEN signal from the USB3320. The USB controller dictates the state of CPEN by programming the ULPI register in the USB3320. The 5 Volt switch is backdrive protected when in the off state. The switch does not provide protection from reverse currents when it is on. See Section 2.9 and Section 2.10 for more information on configuring the EVB-USB3320 for OTG and Host operation.

2.2 1.8 Volt Power Supply

The EVB-USB3320 EVB has a Low Drop-Out (LDO) Regulator that drives the USB3320 VDD18 pins. This LDO requires a nominal 3.3 Volt supply capable of providing 80mA of current to be present at the T&MT connector (pins 8, 16, 57, or 69).

2.3 ULPI I/O Voltage

The USB3320 supports variable ULPI I/O voltage signaling. The ULPI I/O voltage is supplied in one of two ways. By default, the EVB is shipped with VDDIO supplied by the on-board LDO.

Resistor R18 is used to set VDDIO, the digital logic high voltage. To change the value of VDDIO, calculate a new value for R18 (ohms) as follows.

$$R18 = (VDDIO/1.225-1) \times 169000$$

VDDIO must be in the range of 1.8 Volts - 3.3 Volts nominal.

VDDIO can also be supplied to the USB3320 from the T&MT connector instead of using the LDO. To do this, the LDO (U10) must be removed.

The VDDIO voltage level that has been configured on the EVB-USB3320 must be the same as the ULPI I/O voltage level that the link is using.

2.4 Edge Connector for Digital I/O

The T&MT edge connector is compliant to the ULPI specification. Part numbers and manufacturers for this connector and it's mate are given in Table 2.1.

Table 2.1 Edge Connector on the EVB-USB3320

PART NUMBER	DESCRIPTION	MANUFACTURER
2-557101-5	100 pin edge connector on EVB-USB3320	AMP
2-557-101-5	Mating connector to the EVB-USB3320	AMP
1-1734037-0	Alternate 100 pin edge connector for EVB-USB3320	TYCO
1-1734099-0	Alternate mating connector to the EVB-USB3320	TYCO

2.5 REFCLK Frequency Selection

The EVB-USB3320 offers a user selectable reference clock frequency. R25 - R30 are used to configure the REFCLK[2:0] signals which will select the reference clock frequency desired on the EVB-USB3320. Ensure that the frequency of the reference clock or reference crystal being used matches the desired operation frequency configured based on Table 2.2 below. By default, the EVB-USB3320 is configured for 26MHz REFCLK operation.

Table 2.2 Reference Frequency Selection Resistor Configurations

R25	R26	R27	R28	R29	R30	REFCLK FREQUENCY
INSTALL	EMPTY	INSTALL	EMPTY	EMPTY	INSTALL	26.0 MHz (Default)
EMPTY	INSTALL	INSTALL	EMPTY	EMPTY	INSTALL	12.0 MHz
EMPTY	INSTALL	EMPTY	INSTALL	EMPTY	INSTALL	52.0 MHz
INSTALL	EMPTY	INSTALL	EMPTY	INSTALL	EMPTY	24.0 MHz
INSTALL	EMPTY	EMPTY	INSTALL	INSTALL	EMPTY	19.2 MHz
EMPTY	INSTALL	INSTALL	EMPTY	INSTALL	EMPTY	27.0 MHz
EMPTY	INSTALL	EMPTY	INSTALL	INSTALL	EMPTY	38.4 MHz
INSTALL	EMPTY	EMPTY	INSTALL	EMPTY	INSTALL	13.0 MHz

2.6 USB Connector

A standard Mini-AB connector is provided to attach a USB cable or connector. Provision is made on the PCB to accept a Micro-AB connector. See the bill of materials in Section 6 for connector part numbers. Do not substitute a different part number for the Mini-AB receptacle or a short circuit of the USB signals may result at the micro-AB connector PCB footprint.

2.7 VBUS Present Detection

The USB controller must detect VBUS when a USB cable is attached in device mode or when the USB controller turns on VBUS in host or OTG mode. The USB connector VBUS signal is connected to the VBUS pin of the USB3320. The USB3320 includes all of the comparators required to detect VBUS and report the state of VBUS to the USB controller via the ULPI bus.

2.8 ULPI Signal Test Points

Probe points at location J2, provide access to all ULPI signals. Install the Tektronix logic analyzer probe retention kit at J2 to probe these signals. Ordering information for the retention kit is provided in the bill of materials.

2.9 Converting the EVB to an OTG System

“Out of the box”, the EVB-USB3320 is delivered as a USB Device system. To convert it to be a USB OTG development board, the following modifications must be made:

1. Install R13 (zero ohm resistor). This connects the VBUS 5V switch to the VBUS signal.
2. Remove R23. This is the R_{VBUS} value required for a USB Device.
3. Install R10 (1.0K, 1W resistor). This is the R_{VBUS} value required for a USB OTG Device.

Since the USB3320 is designed to accommodate up to 30V on VBUS, R10 is rated at 1W to accommodate this entire voltage range. Refer to the USB3320 datasheet for more information on sizing this resistor.

2.10 Converting the EVB to a Host System

“Out of the box”, the EVB-USB3320 is delivered as a USB Device System. To convert it to be a USB Host development board, the following modifications must be made:

1. Install R13 (zero ohm resistor). This connects the VBUS 5V switch to the VBUS signal.
2. Install C20 (150uF capacitor). This increases the value of C_{VBUS} to be USB 2.0 Host compliant.

2.11 Converting the EVB to Support ULPI Clock Input Mode

“Out of the box”, the EVB-USB3320 uses a crystal (Y1) as the clock reference, and is configured for ULPI Clock Output Mode where CLKOUT sources a 60MHz clock. To convert the EVB to support ULPI Clock Input Mode, the following changes must be made:

1. Install R12 (zero ohm resistor). This shorts CLKOUT to VDD18.
2. Install R3 (zero ohm resistor). This shorts REFCLK to the System Clock pin on the T&MT connector.
3. Confirm that R4 is not populated.
4. Remove the following components to remove the crystal circuit: Y1, R17, C23

Refer to the USB3320 datasheet for more information on ULPI Clock Input Mode.

2.12 T&MT Pin Description

The T&MT signal names, pin number and function are described in Table 43 and Table 44 of the ULPI Specification rev 1.1.

The EVB-USB3320 fully implements a ULPI compliant interface to the T&MT connector, including support for ULPI Clock Input Mode. This EVB supports a 1.8V ULPI I/O voltage. All signals are described in Table 2.3.

Table 2.3 T&MT Connector Pin Definitions

PIN	NAME	DESCRIPTION	DIRECTION
86, 36, 85, 34, 83, 33, 82, 31	DATA[7:0] Refer to Schematic for Connector Pin Assignment	ULPI Data Bus	IN/OUT
96	STP	ULPI STP Signal	INPUT TO EVB
70	DIR	ULPI DIR Signal	OUTPUT FROM EVB
71	NXT	ULPI NXT Signal	OUTPUT FROM EVB
90	CLKOUT	ULPI Clock Signal	OUTPUT FROM EVB
55	VBUS_FAULT_N	Driven low by the VBUS switch (U2) in the event of a switch fault condition.	OUTPUT
15	SPKR_L	In USB Audio mode, SPKR_L is connected to the DP pin via an analog switch in the USB3320.	IN/OUT
45	SPKR_RM	In USB Audio mode, SPKR_RM is connected to the DP pin via an analog switch in the USB3320.	IN/OUT
17	RESET	Asserting RESET will place the USB3320 in a low power state. Upon exiting this state (RESET=0), all ULPI registers will contain power-on reset values.	INPUT
47	VBUS_IN	This pin is not connected	NO CONNECT
28	VBUS_OUT	+5V from the T&MT connector	INPUT TO EVB
8, 16, 57, 69	VDD	+3.3V from the T&MT connector	INPUT TO EVB
52	SYSTEM_CLOCK	Optional clock input to EVB. EVB is built with the USB3320 REFCLK provided by a crystal. See Section 2.11 for more information on configuring the EVB-USB3320 for ULPI Clock Input mode.	NO CONNECT (input to EVB if R3 is installed)
100	PSU_SHD_N	This pin is driven low indicating that +3.3V must be sourced from the link through the T&MT connector pins 8, 16, 57, 69 and +5.0V must be sourced from the link through the T&MT connector pin 28.	OUTPUT FROM EVB
49	DC_PSNT_N	This pin is driven low indicating a daughter card is present.	OUTPUT FROM EVB

3 Getting Started

The block diagram in Figure 3.1 gives a simplified view of the EVB-USB3320 EVB. The EVB-USB3320 is ready for device operation. To modify the board for OTG or Host applications, refer to Section 2.9 or Section 2.10, respectively.

It is required to provide +5V to T&MT connector pin 28 and +3.3V on T&MT pins 8,16,57,69 to power the EVB-USB3320.

The EVB-USB3320 is built with a USB Mini-AB receptacle. Do not substitute a Mini-AB receptacle different from the one specified in the bill of materials, or a short circuit may occur on the USB signals at the Micro-AB connector PCB footprint.

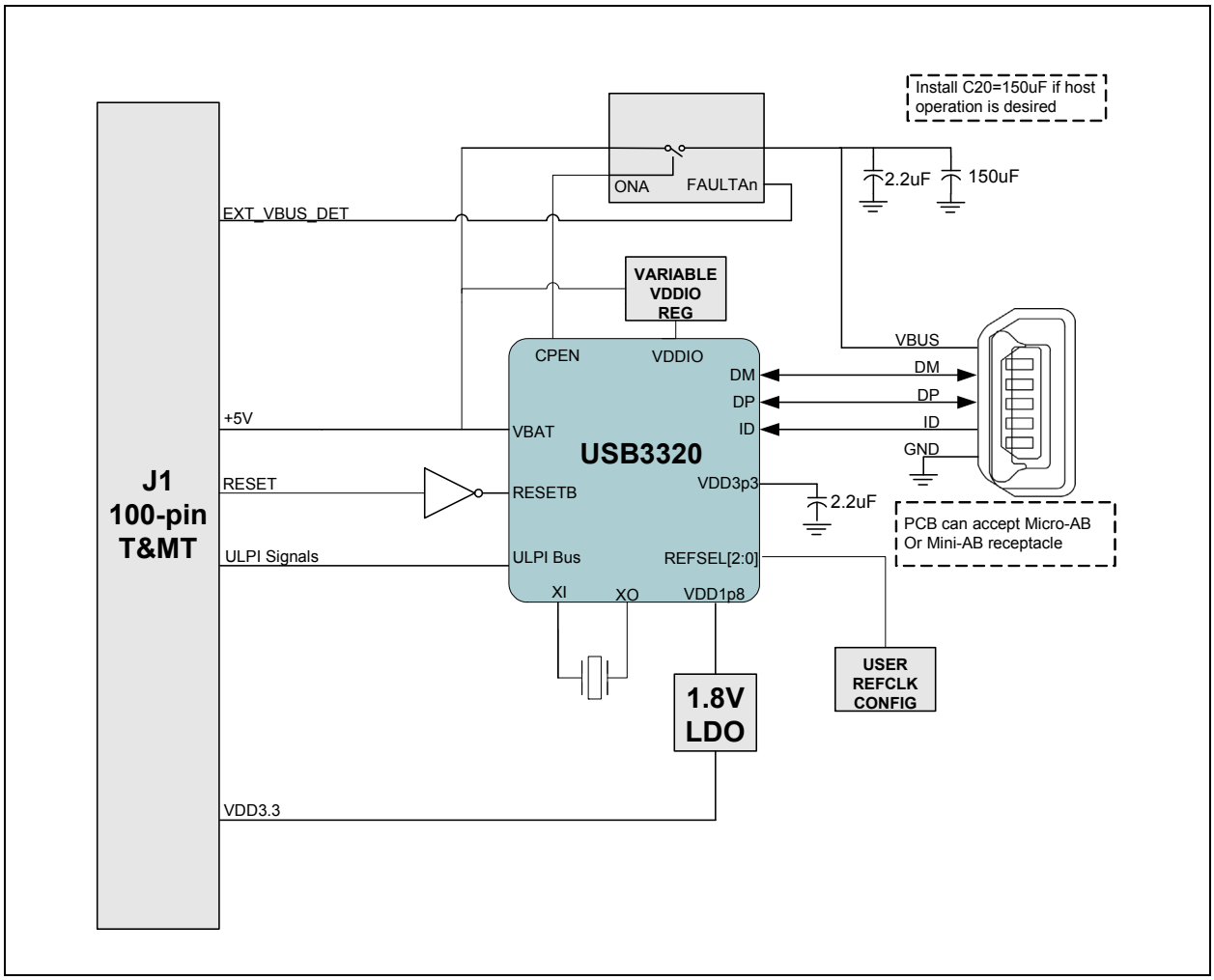


Figure 3.1 Block Diagram of EVB-USB3320

When the EVB-USB3320 is powered on, check the following things to be certain the board is functioning normally:

- RESET should be de-asserted (logic low at the T&MT connector and RESETB at the USB3320 should be logic high = VDD18). If RESETB=0, the USB3320 will be in a low power state.
- The voltage at R2 (RBIAS) should be 0.8V DC. If this voltage is not present, the USB3320 is in a low power state.
- There should be a digital 60 MHz square wave signal at T&MT connector pin 90. The amplitude should be approximately VDDIO. This is the CLKOUT signal of the USB3320.

- The voltage at C3 should be approximately 3.3V. This is the USB3320 internal 3.3V voltage regulator output.
- The voltage at C7 should be 1.8V. This is the 1.8V regulator output.

4 Protecting VBUS from Non-Compliant VBUS Voltages

The USB3320 is fully tolerant to VBUS voltages up to 30V. An external resistor on the VBUS line (R_{VBUS}) is required for the integrated overvoltage protection circuit in the USB3320. R_{VBUS} is either R10 or R23 on the EVB-USB3320. For peripheral and host applications, R_{VBUS} is 10K (install R23, remove R10). For OTG applications, R_{VBUS} is 1K (install R10, remove R23).

5 EVB-USB3320 Schematic

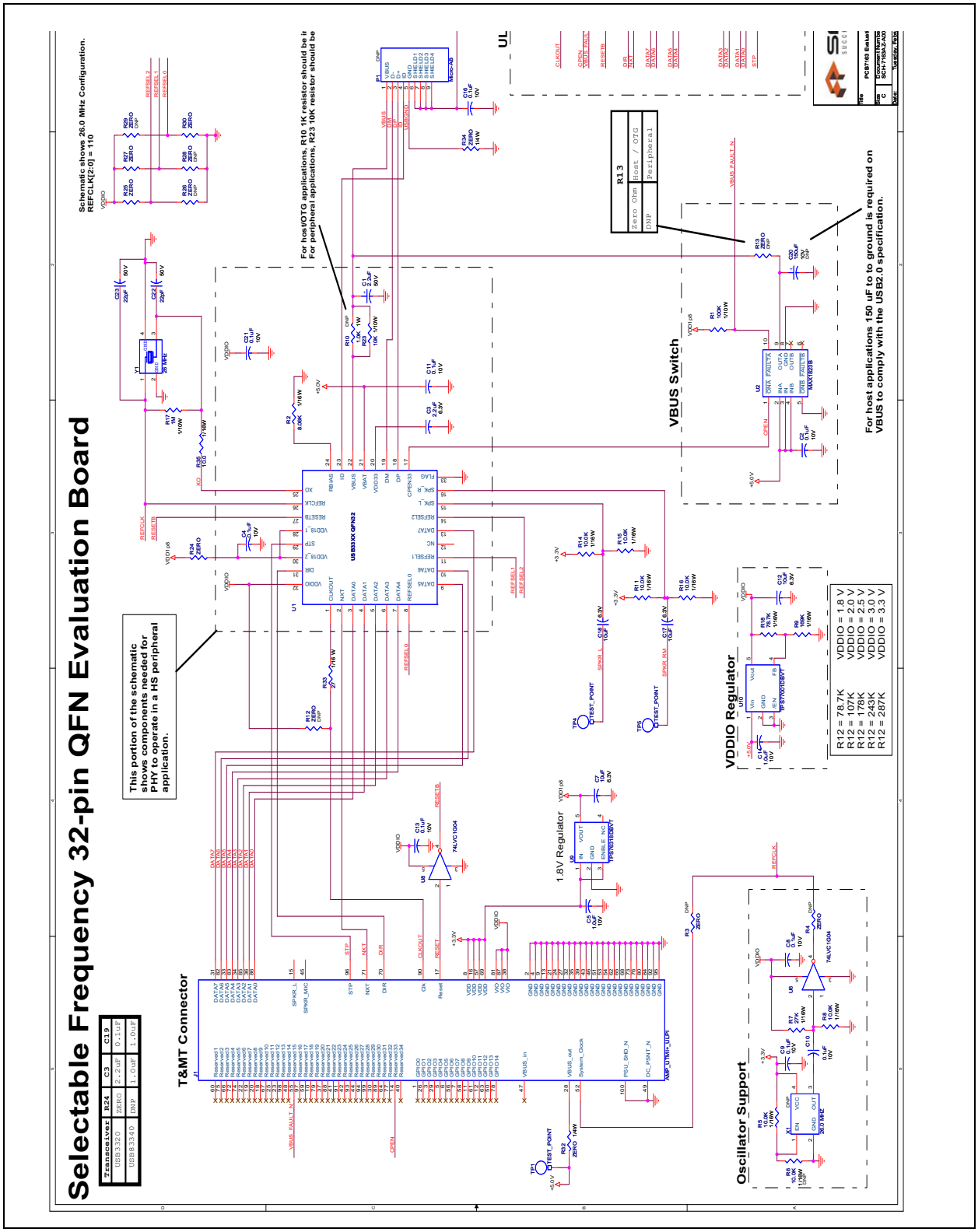


Figure 5.1 EVB-USB3320 Schematic

6 EVB-USB3320 Bill of Materials

Item Number	Ref Des	QTY	Value	Tolerance	Description	Manufacturer	Manufacturer Part Number	Digikey Part Number
10	C1	1	2.2µF, 50V	±10%	CAP CER 2.2UF 50V X7R 1206	Murata Electronics North America	GRM31CR71H225KA88L	490-3367-1-ND
20	C17, C18	2	10.0µF,10V	±10%	CAP CER 10UF 10V X5R 0805	Murata Electronics North America	GRM21BR61A106KE19L	490-1709-1-ND
30	C2, C4, C8, C9, C10, C11, C13, C16, C21	9	0.1µF, 10V	20%	CAP CER .1UF 10V X5R 0402	Kemet	C0402C104K8PACTU	399-3027-1-ND
40	C20	DNP	150.0µF,16V	±20%	CAP 150UF 16V ELECT FK SMD	PANASONIC	EEV-FK1C151XP	PCE3512CT-ND
50	C3	1	2.2µF, 6.3V	20%	CAP CER 2.2UF 6.3V X5R 0402	Murata Electronics North America	GRM155R60J225ME15D	490-4519-1-ND
60	C5, C14	2	1.0µF, 10V	±10%	CAP CER 1UF 10V X5R 0402	Murata Electronics North America	GRM155R61A105KE15D	490-3890-1-ND
70	C7, C12	2	10.0µF, 10V	-20%/+80%	CAP 10UF 10V CERAMIC F 0805	KEMAT	ECJ-2FF1A106Z	PCC2233CT-ND
80	C22, C23	2	22pF, 50V	±5%	CAP 22PF 50V CERAMIC 0402 SMD	Panasonic - ECG	ECJ-0EC1H220J	PCC220CQCT-ND
90	J1	1			RCPT ASSY,R/A,CHAMP 050,100 P	TYCO ELECTRONICS/AMP	1-1734037-0	A33470-ND
100	J2	DNP			Retention Kit for P6960/P6980 Logic analyzer Probe	Tektronix	020-2539-00	
110	P1	DNP			CONN RCPT MICRO USB AB SMD R/A	Hirose Electric Co Ltd	ZX62-AB-5P	H11495CT-ND
120	P2	1			USB-OTG, Mini AB Receptacle, Surface Mount Right Angle	Molex/Waldom Electronics Corp	56579-0576	WM17122CT-ND
130	R1	1	100K	±5%	RES 100K OHM 1/16W 5% 0402 SMD	Vishay/Dale	CRCW0402100KJNED	541-100KJCT-ND
140	R10	DNP	1K	1%	RES 1K OHM 1W 2512 SMD	PANASONIC	ERJ-1TYF102U	PT1KAECT-ND
150	R18	1	78.7K	1%	RES 78.7K OHM 1/16W 1% 0402 SMD	PANASONIC	ERJ-2RKF7872X	P78.7KLCT-ND
160	R17	1	1M	5%	RES 1M OHM 1/10W 5% 0402 SMD	Vishay/Dale	CRCW04021M00JNED	541-1.0MJCT-ND
170	R2	1	8.06K	±1%	RES 8.06K OHM 1/16W 1% 0402 SMD	Vishay/Dale	CRCW04028K06FKED	541-8.06KLCT-ND
180	R23	1	10K	1%	RES 10.0K OHM 1/10W 0603 SMD	YAGEO	RC0603FR-0710KL	311-10.0KHRCT-ND
190	R32, R34	2	ZERO	±5%	RES ZERO OHM 1/4W 5% 0402 SMD	Vishay/Dale	CRCW12060000Z0EA	541-0.0ECT-ND
200	R24, R25, R27, R30	4	ZERO	±5%	RES ZERO OHM 1/16W 5% 0402 SMD	PANASONIC	ERJ-2GE0R00X	P0.0JCT-ND
210	R3, R4, R12, R13, R26, R28, R29	DNP	ZERO	±5%	RES ZERO OHM 1/16W 5% 0402 SMD	PANASONIC	ERJ-2GE0R00X	P0.0JCT-ND
220	R33	1	27	1%	RES 27 OHM 1/16W 1% 0402 SMD	Vishay/Dale	CRCW040227R0FKED	541-27.0LCT-ND
230	R5, R8, R11, R14, R15, R16	8	10K	±5%	RES 10K OHM 1/16W 5% 0402 SMD	PANASONIC	ERJ-2GEJ103X	P10KJCT-ND
240	R6	DNP	10K	±5%	RES 10K OHM 1/16W 5% 0402 SMD	PANASONIC	ERJ-2GEJ103X	P10KJCT-ND
250	R7	1	27K	1%	RES 27K OHM 1/16W 1% 0402 SMD	PANASONIC	ERJ-S02F2702X	ERJ-S02F2702X-ND
260	R9	1	169K	1%	RES 169K OHM 1/16W 1% 0402 SMD	PANASONIC	ERJ-2RKF1693X	P169KLCT-ND
270	R35	1	10	1%	RES 27 OHM 1/16W 1% 0402 SMD	Vishay/Dale	CRCW040210R0FKED	541-10.0LCT-ND
280	TP1, TP2, TP3, TP4, TP5	5			PC TEST POINT MINIATURE SMT	Keystone Electronics	5015	5015KCT-ND
290	U1	1			USB PHY with ULPI Interface	SMSC	USB3320C-EZK	
300	U10	1			IC ADJ 50MA LDO REG SOT-23-5	TEXAS INSTRUMENTS	TPS77001DBVT	296-2762-1-ND
310	U2	1			IC SW USB DUAL W/FB 10-UMAX	Maxim Integrated Products	MAX1823BEUB+	MAX1823BEUB+-ND
320	U6, U8	2			IC SINGLE INVERTER-GATE SOT-23-5	TEXAS INSTRUMENTS	SN74LVC1G04DBVR	296-11599-1-ND
330	U9	1			IC REG LDO 1.8V 150MA SOT-23-5	TEXAS INSTRUMENTS	TPS76318DBVT	296-2700-1-ND
340	X1	DNP	Note 1		OSCILLATOR PROG 3.3V +-50PPM SMD, 26.0MHz	ABRACON CORPORATION	AP3S-BLANKS	AP3S3EC-ND
350	Y1	1	Note 2	+/-30ppm	CRYSTAL 26.000 MHZ 20PF SMD	CTS-Frequency Controls	403C35E26M00000	CTX733CT-ND

Note 1 Oscillator frequency depends on frequency selected by U1 pins REFSEL[2:0]. Frequency must be specified at time of order.

Note 2 Crystals may not available in all frequencies supported by U1.

Figure 6.1 EVB-USB3320 Bill of Materials

7 Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (02-09-10)		Replaced all references of “CRB” with “EVB” throughout document.
Rev. 1.0 (05-01-09)	Initial Release	