LTC3625/LTC3625-1: 1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing

DESCRIPTION

Demonstration circuit 1583A is a 1A high efficiency 2- Cell supercapacitor charger with automatic cell balancing featuring the LTC3625/LTC3625-1. The LTC3625/LTC3625-1 are programmable supercapacitor chargers designed to charge two supercapacitors in series to a fixed voltage of 5.3V/4.8V (LTC3625) or 4.5V/4.0V (LTC3625-1) from a 2.7V to 5.5V input supply. Automatic cell balancing is achieved during the charging phase, preventing overvoltage damage to either supercapacitor while maximizing charge rate.

High efficiency, high charging current, low quiescent current and low minimum external parts count make the LTC3625/LTC3625-1 ideally suited for small form factor backup or high peak power systems.

Charging current/maximum input current level is programmed with an external resistor. When the input supply is removed and/or the EN pin is low, the LTC3625/LTC3625-1 automatically enters a low current state, drawing less than 1μA from the supercapacitors.

The LTC3625/LTC3625-1 are offered in a 12-lead (3mm × 4mm × 0.75mm) DFN package.

Design files for this circuit board are available at http://www.linear.com/demo

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PERFORMANCE SUMMARY

Typical Specifications (25°C) LTC3625	
Input Voltage Range: V_{CC}	2.7V to 5.5V
Charge Current	1.0A
V_{OUT}	4.8V or 5.3V Dependant on JP1 Setting
Typical Specifications (25°C) LTC3625-1	
Input Voltage Range: V_{CC}	2.7V to 5.5V
Charge Current	1.0A
V_{OUT}	4.0V or 4.5V Dependant on JP1 Setting

OPERATING PRINCIPLES

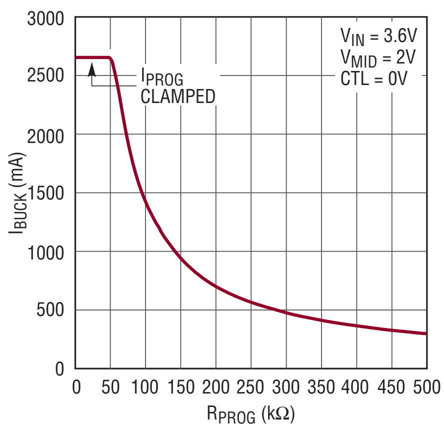
The LTC3625/LTC3625-1 are dual cell supercapacitor chargers. Their unique topology charges two series connected capacitors to a fixed voltage with programmable charging current preventing overvoltage damage to either of the cells, even if they are severely mismatched. No balancing resistors are required. The LTC3625/LTC3625-1 include an internal buck converter between V_{IN} and V_{MID} to regulate the voltage on C_{BOT} (the bottom capacitor) as well as an internal boost converter between V_{MID} and V_{OUT} to regulate the voltage on C_{TOP} (the top capacitor). The output current of the buck converter is user-programmed via the PROG pin while the input current of the boost converter is set to 2A (typical).

OPERATING PRINCIPLES

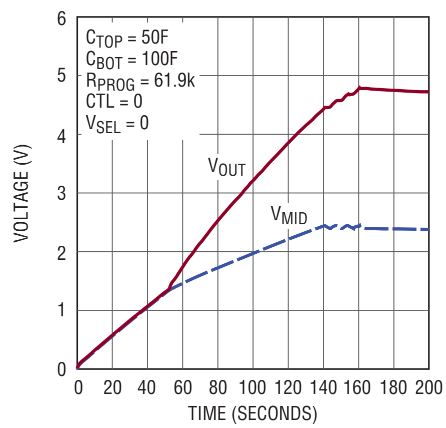
The LTC3625/LTC3625-1 contains various functions that are digitally controlled. The CTL pin is a control function that sets the device into a two inductor mode (low) or a single inductor mode (high). The CTL pin must be hard tied to either V_{IN} or GND. A logic high on the V_{SEL} pin sets V_{OUT} to 5.3V/4.5V while a logic low sets V_{OUT} to 4.8V/4.0V. The EN pin will enable the device with a logic high while a logic low disables the device and V_{OUT} becomes high impedance.

An internal undervoltage lockout (UVLO) circuit monitors V_{IN} and keeps the LTC3625/LTC3625-1 disabled until V_{IN} rises above 2.90V/2.63V if V_{SEL} is high or 2.63V/2.63V if V_{SEL} is low. Hysteresis on the UVLO turns off the LTC3625/LTC3625-1 if V_{IN} drops approximately 100mV below the UVLO rising threshold. When in UVLO, only current needed to detect a valid input will be drawn from V_{IN} or V_{OUT}.

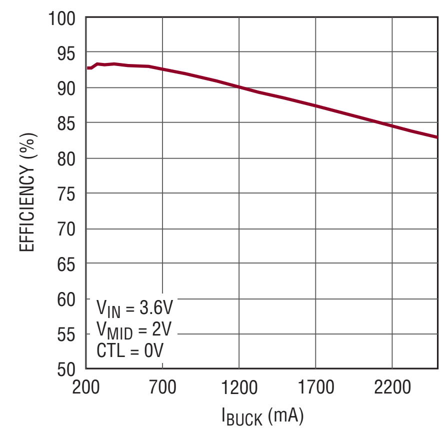
Buck Output Current vs R_{PROG}



Charging Two 2:1 Mismatched Supercapacitors



Buck Efficiency vs I_{BUCK}



QUICK START PROCEDURE

Using short twisted pair leads for any power connections and with all loads and power supplies off, refer to Figure 1 for the proper measurement and equipment setup.

Jumper and Load Settings to start:

Connect Jumper from V_{OUT} to V_{PULLUP}

JP1 (V_{SEL}) = 5.3V/4.5V

JP2 (ENABLE) = OFF

LOAD1 = OFF

1. Set V_{IN} to 3.3V and verify that the input current is less than 10mA. Verify that V_{OUT} is less than 2.0V indicating that the supercapacitor is in a low charge state.
2. Set JP2 to the ON position. Verify that V_{OUT} is less than 3.5V and that PGOOD is low.
3. Monitor PGOOD and V_{OUT}. When PGOOD goes high, verify V_{OUT} is ~5.0V/4.1V.
4. Verify V_{OUT} when the input current drops to less than 10mA indicating a fully charged capacitor. Monitor PFO, verify PFO is high. Verify V_{OUT} is ~5.3V/4.5V.
5. Turn on Load1 and set to 950mA. Monitor PGOOD and V_{OUT}. When PGOOD goes low, verify V_{OUT} is ~5.0V/4.1V.
6. Set JP2 to OFF, monitor PFO and PGOOD, verify both are low. Allow the supercapacitor to discharge to 1.5V, then turn off Load1.

Note: Once JP2 is placed in the OFF position, V_{OUT} will drop quickly.

7. Set JP1 to 4.8V/4.0V. Set JP2 to the ON position. Verify that V_{OUT} is less than 3.0V and that PGOOD is low.

QUICK START PROCEDURE

8. Monitor PGOOD and V_{OUT}. When PGOOD goes high, verify V_{OUT} is ~4.5V/3.7V.
9. Verify V_{OUT} when the input current drops to less than 10mA indicating a fully charged capacitor. Verify V_{OUT} is ~4.8V/4.0V.
10. Turn on Load1 and set to 950mA. Monitor PGOOD and V_{OUT}. When PGOOD goes low, verify V_{OUT} is ~4.3V/3.5V.
11. Set JP2 to OFF and allow the supercapacitor to discharge to 1.0V, then turn off Load1.

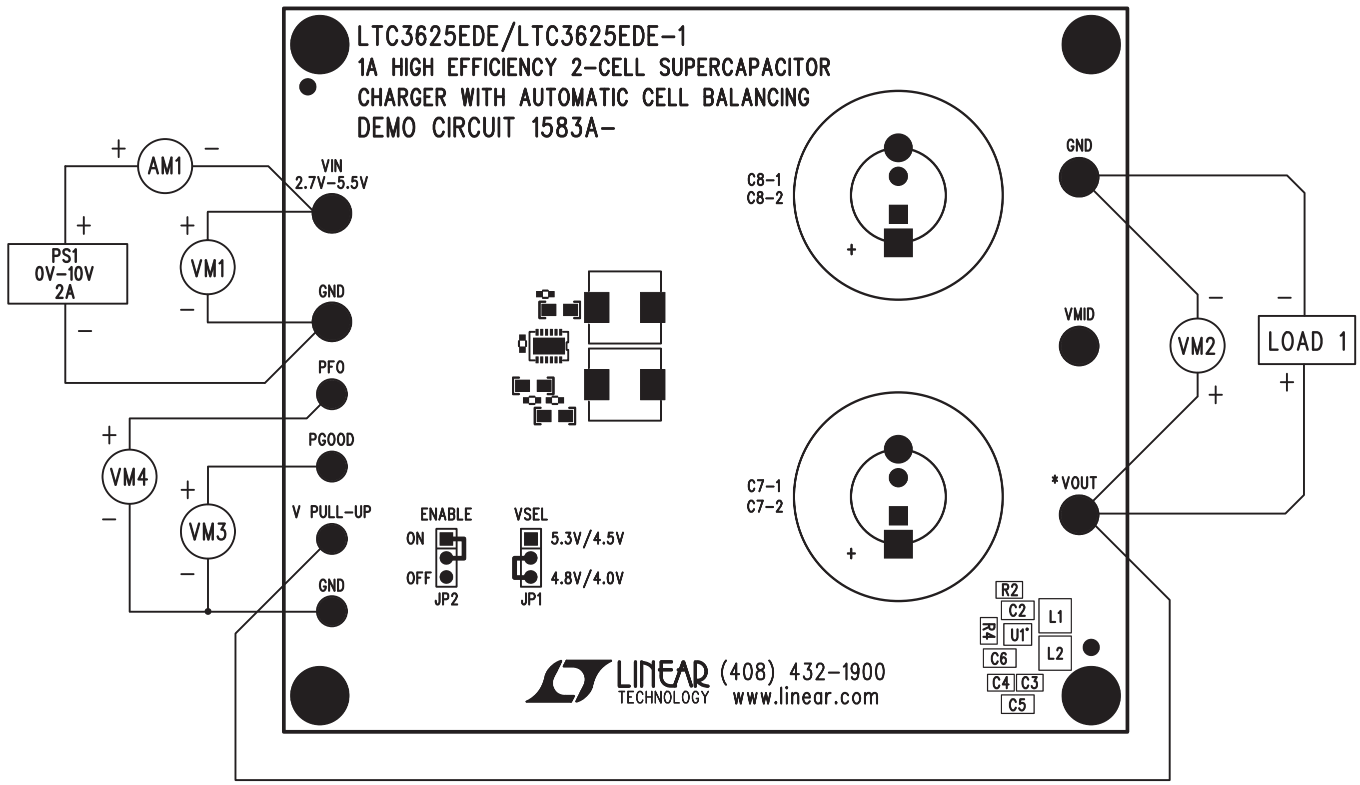


Figure 1. Proper Measurement Equipment Setup

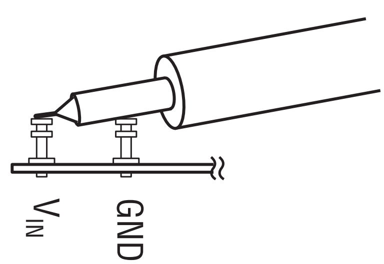
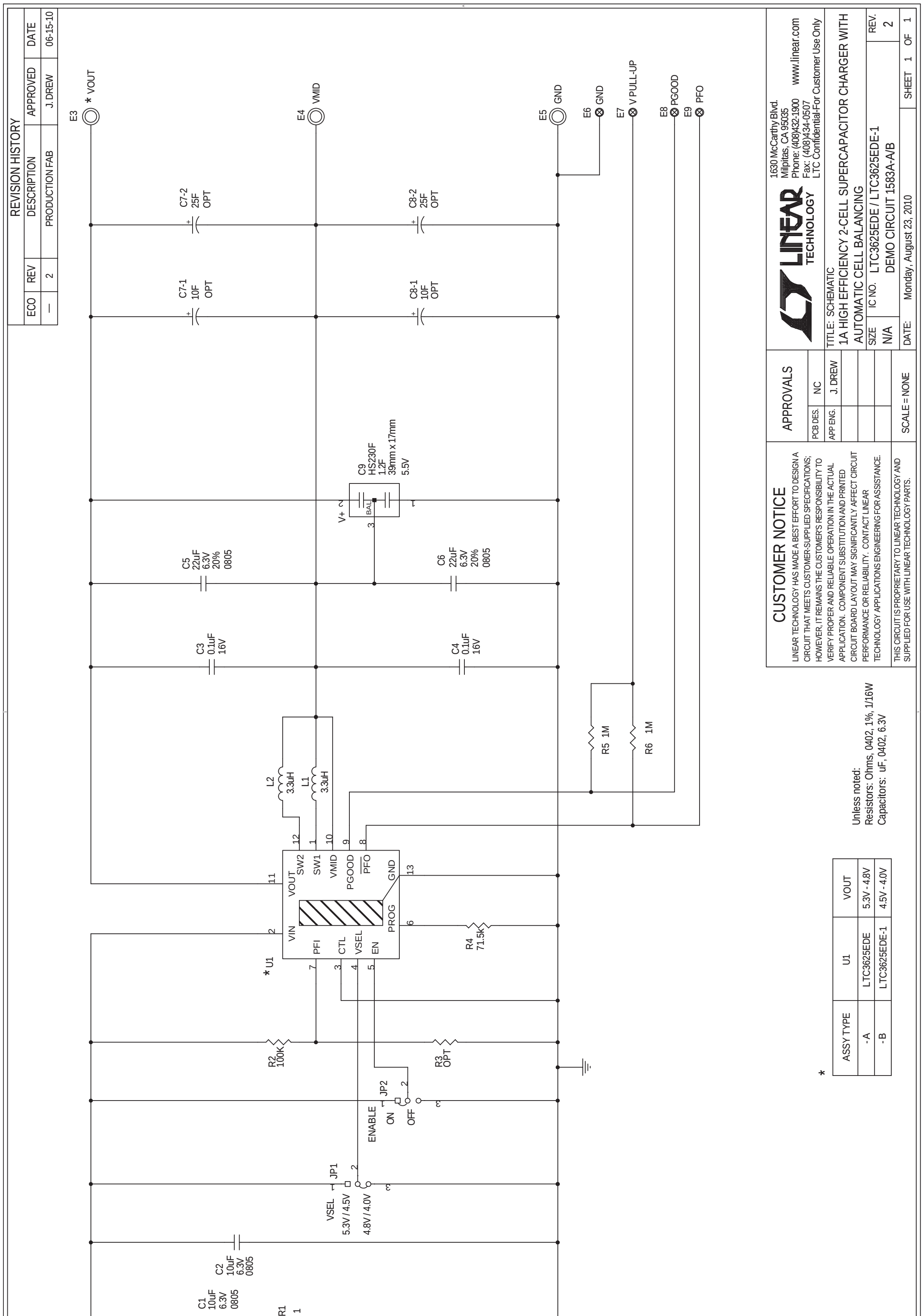


Figure 2. Measuring Input or Output Ripple

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURERS/PART NUMBER
Required Circuit Components				
1	2	C1, C2	CAP, CHIP, X5R, 10µF, 20%, 6.3V, 0805	Murata, GRM21BR60J106E39L
2	2	C5, C6	CAP, CHIP, X5R, 22µF, 20%, 6.3V, 0805	Murata, GRM21BR60J226ME39L
3	2	C3, C4	CAP, CHIP, X7R, 0.1µF, 10%, 16V, 0402	Murata, GRM155R71C104KA88D
4	1	C9	Supercapacitor, 1.2F, 5.5V, 39mm × 17mm	CAP-XX, HS230F
5	2	L1, L2	Inductor, 3.3µH, 3.0A, 20mΩ, 7mm × 7mm	Coiltronics, DR73-3R3-R
6	1	R1	Res., CHIP, 1Ω, 1/16W, 1%, 0402	Vishay, CRCW04021R00FKED
7	1	R2	Res., CHIP, 100k, 1/16W, 1%, 0402	Vishay, CRCW0402100KFKED
8	1	R4	Res., CHIP, 71.5k, 1/16W, 1%, 0402	Vishay, CRCW040271K5FKED
9	2	R5, R6	Res., CHIP, 1M, 1/16W, 1%, 0402	Vishay, CRCW04021M00FKED
10	1	U1	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	LTC3625EDE
Optional Demo Board Circuit Components				
1	0	C7-1 - C8-1 (OPT)	Supercapacitor, 10.0F, 2.7V, 10mm × 30mm	Illinois CAP, 106DCN2R7Q
2	0	C7-2 - C8-2 (OPT)	Supercapacitor, 25.0F, 2.7V, 16mm × 25mm	Illinois CAP, 256DCN2R7Q
3	0	R3 (OPT)	RES., CHIP, 1/16W, 1%, 0402	User Selectable
4	0	U1	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	LTC3625EDE-1
Hardware For Demo Board Only				
1	5	E1 - E5	Turret, 0.09 DIA	MILL-MAX, 2501-2
2	4	E6 - E9	Turret, 0.061 DIA	MILL-MAX, 2308-2
3	2	JP1, JP2	Header, 3 PINS, 2mm	Samtec, TMM-103-02-L-S
4	2	JP1, JP2	Shunt, 2mm	Samtec, 2SN-BK-G

SCHEMATIC DIAGRAM



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LT 1110 • PRINTED IN USA

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