EVBUM2262/D

KAI-0330 Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code described in this document is intended for use in the AD 984X Timing Board. The code is written specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit:	PN
Timing Generator Board	Board Model 3E8180 (AD9845 30 MHz)
KAI−0330 Imager Board	Board Model 3E8210
Framegrabber Board	National Instruments model PCI−1424

ALTERA CODE FEATURES / FUNCTIONS

The Altera Programmable Logic Device (PLD) has three major functions:

Timing Generator

The PLD serves as a state machine based timing generator whose outputs interface to the KAI−0330, the AD9845 Analog Front End (AFE), and the PCI−1424 Framegrabber. The behavior of these output signals is dependent upon the current state of the state machine. External digital inputs, as well as jumpers on the board can be used to set the conditions of certain state transitions (See Table 1). In this manner, the board may be run in any of the following operating modes:

- Single Output Mode Operation
- Dual Output Mode Operation
- 2 x 2 Binning Mode Operation (in Single Output Mode Only)
- Fifteen different Integration Mode Options (Sub−frame Integration Times utilizing Electronic Shuttering as well as Multi−frame Integration Times)
- Fast Dump Mode Operation
- Four different Optical Black Clamp (AD9845 CLPOB) Modes

Delay Line Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the 10 silicon delay IC's on the Timing Generator Board to their default delay settings via a 3 wire serial interface. See Table 10 for details.

AFE Register Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via a 3 wire serial interface. See Table 11 for details.

ALTERA CODE I/O

Table 2. INPUTS

Symbol	Description
POWER_ON_DELAY	The rising edge of this signal clears and re−initializes the PLD
SYSTEM_CLK	60 MHz clock, 2X the desired pixel clock rate
INTEGRATE_CLK	(Not used for KAI−0330 operation)
JMP0	Output mode select (High = Dual / Low = Single)
JMP1	Fast Dump Mode select control line (High = Enable / Low = Disable)
JMP2	Binning select control line (High = 2x2 binning / Low = no binning)
JMP3	(Not used for KAI−0330 operation)
DIO[5..0]	(Not used for KAI−0330 operation)
DIO[8..6]	Electronic shutter mode control lines (See Table 14)
DIO[11..9]	Multi frame integration mode control lines (See Table 12 and Table 13)
DIO[13..12]	AD9845 CLPOB MODE control lines (See Table 9)
DIO[19..14]	(Not used for KAI−0330 operation)

Table 3. OUTPUTS

Symbol	Description
V1_CLK	KAI−0330 V1 Clock
V2_CLK	KAI−0330 V2 Clock
H1_CLK	KAI−0330 H1BL, H1SL, H1SR Clocks
H1BR_CLK	KAI−0330 H1BR Clock
H2_CLK	KAI−0330 H2BL, H2SL, H2SR, Clocks
H2BR_CLK	KAI−0330 H2BR Clock
R_CLK	KAI−0330 Reset Clock
FDG	KAI−0330 Fast Dump Gate
V3RD	KAI−0330 V2 Third Level Control Signal
V_SHUTTER	Electronic Shutter Control Signal
SHP	AD9845 Sample CCD Reset Level
SHD	AD9845 Sample CCD Data Level
DATACLK	AD9845 A/D Convert Clock
PBLK	AD9845 Pixel Blanking
CLPOB	AD9845 Black Level Clamp
CLPDM	AD9845 Dc Restore Input Clamp
VD	AD9845 Optional Vertical Drive Sync
HD	AD9845 Optional Horizontal Drive Sync
PIX	PCI−1424 Frame Grabber Pixel Rate Synchronization
FRAME	PCI−1424 Frame Grabber Frame Rate Synchronization
LINE	PCI−1424 Frame Grabber Line Rate Synchronization
CH1_SLOAD	Serial Load Enable, Ch1 AD9845 AFE
CH2_SLOAD	Serial Load Enable, Ch2 AD9845 AFE
SLOAD	Serial Load Enable, Delay Line IC’s
SCLOCK	Serial Clock (AD9845, Delay Line IC’s)

Table 3. OUTPUTS

Symbol	Description
SDATA	Serial Data (AD9845, Delay Line IC's)
SERIAL_ENA	Tri−State Control Of PLD/External Enable Of Serial Interface
INTEGRATE	High During CCD Integration Time

KAI−0330 TIMING CONDITIONS

Table 4. SYSTEM TIMING CONDITIONS

Description	Symbol	Time	Notes
System Clock Period	Tsys	16.67 ns	60 MHz system clock
Unit integration time	Uint	10 ms	
Power stable delay	Tpwr	30 ms	Typical
Default Serial Load Time	Tsload	112.5 μs	Typical

Table 5. CCD TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
H1, H1L, H2, RESET period	Tpix	33.33 ns	1	30 MHz clocking of H1, H1L, H2, RESET
Photodiode Transfer setup	T3P	10.03 μs	301	
Photodiode Transfer Time	TV3rd	4.0 μs	120	
Photodiode Readout delay	T3D	10.03 μs	301	
VCCD delay	Tvd	66.66 μs	2	
VCCD transfer time	TVCCD	2.066 μs	62	From V2_START to V2_STOP
HCCD Delay	Thd	2.066 μs	62	
Vertical Transfer period	Vperiod	4.2 μs	126	Vperiod = Tvd + TVCCD + Thd
Shutter Pulse Time	Ts	25.0 μs	750	
Shutter Pulse Delay	Tsd	5.0 μs	150	
Pixels per line	PIX_X		708	694 CCD pixels plus 14 overlock
Lines per frame	PIX_Y		496	484 active CCD lines plus 12 dark lines Single Output; 248 CCD lines (242 active) per channel Dual Output
RESET clock pulse width	Tr	5 ns		Tr is set by hardware on imager board

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
SHP,SHD,DATACLK period	Tpix	33.3 ns	1	30 MHz clocking of SHP,SHD,DATACLK
SHP pulse width	Tshp	7.5 ns		Tshp is set by hardware on timing board
SHD pulse width	Tshd	7.5 ns		Tshd is set by hardware on timing board
CLPOB1 line start	CLPOB1_ls		2	Line transfer counter, CLPOB modes 0,2 only
CLPOB1 line end	CLPOB1_le		3	Line transfer counter, CLPOB modes 0,2 only
CLPOB1 start pixel	CLPOB1_ps		100	Line transfer counter, CLPOB modes 0,2 only
CLPOB1 end pixel	CLPOB1_pe		600	Line transfer counter, CLPOB modes 0,2 only
CLPOB2 start pixel	CLPOB2_ps		696	Line transfer counter, CLPOB modes 0,1 only
CLPOB2 end pixel	CLPOB2_pe		706	Line transfer counter, CLPOB modes 0,1 only

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
CLPDM start pixel	CLPDM_ps		2	Horizontal transfer counter
CLPDM end pixel	CLPDM_pe		12	Horizontal transfer counter
PBLK start pixel	PBLK_ps		1	Vertical transfer counter
PBLK end pixel	PBLK_pe		110	Vertical transfer counter

Table 7. PCI−1424 TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
Pixel period	Tpix	33.3 ns	1	30 MHz clocking of PIX sync signal

MODES OF OPERATION

The following modes of operation are available to the user.

Output Modes

The output mode is selected by setting the JMP0, JMP1 and JMP2 inputs to the appropriate level. Binning overrides Fast Dump Mode, and Dual Output Mode overrides Binning.

Table 8. OUTPUT MODE JUMPER SETTINGS

JMP2 (Binning)	JMP1 (FDG)	JMP0 (Output)	Output Mode
LOW	LOW	LOW	Single Output Mode (496 lines)
LOW	LOW	HIGH	Dual Output Mode (248 lines)
LOW	HIGH	LOW	Single Output FDG Mode (496−100−100 = 296 lines)
LOW	HIGH	HIGH	Dual Output FDG Mode ((496−200) / 2 = 148 lines)
HIGH	LOW	LOW	Single Output 2x2 Bin Mode (248 lines)
HIGH	LOW	HIGH	Not Supported; Dual Output Mode Occurs (248 lines)
HIGH	HIGH	LOW	Not Supported; Single Output 2x2 Bin Mode Occurs (248 lines)
HIGH	HIGH	HIGH	Not Supported; Dual Output FDG Mode Occurs (148 lines)

Dual Output Mode

The KAI−0330 device features dual horizontal registers and output amplifiers, to allow a nearly 2X improvement in frame rate. Setting the JMP0 jumper to high causes two Vertical Transfers to occur before each Horizontal Transfer. One line of video is transferred into each horizontal register, allowing simultaneous readout of two lines.

Fast Dump Gate Mode

When FDG Mode is selected, 100 lines of video are rapidly dumped at the start of the frame, and another 100 lines are dumped at the end of the frame. In this way only the middle 296 lines of the image are read out.

Binning Mode (2x2)

Utilizing the JMP2 input, the timing can be set to accumulate 2 lines of charge in the horizontal register before clocking the charge down the horizontal register; 2 registers of charge are then accumulated in the output structure floating diffusion before clocking the charge out of the device. In this way, the total charge of a 2x2 pixel area is summed into one measurement.

Multi−Frame Integration Modes

Integration times of more than a frame time can be achieved by varying the time between transfer of charge from the photodiodes. In Multi−frame integration mode, the Integration time can be set from 1X to 8X the frame time via the DIO interface (See Table 12 and Table 13).

Electronic Shutter Modes

Integration times less than one frame time can be achieved by electronic shuttering of the device. In electronic shutter mode, the integration time can be set from 1X to 1/8X frame time via the DIO interface.

Black Clamp Modes

One of the features of the AD9845 AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. Several options for operating this black clamp are provided and are controlled by the digital inputs D[13..12]. The default CLPOB mode is 0.

Table 9. BLACK CLAMP MODES

CLPOB Mode DIO[13..12]	Black Clamp Operation	Notes
0	Several dark pixels at the end of each line	Default Mode
1	Several dark lines at the beginning of each frame	
2	Several dark lines per frame, and several dark pixels per line	
3	Off, CLPOB always held high	

PIXEL RATE CLOCKS GENERATION

The pixel rate clocks are derived from the system clock. They operate at 1/2 the frequency of the system clock. The PIXEL_CLK signal is generated from the rising edge of the system clock. The DELAYED_PIX_CLK signal is generated from the falling edge of the system clock. By utilizing both edges of the system clock, 4 start positions for the pixel rate clocks are achieved.

1. The PIXEL_CLK signal
2. The DELAYED_PIX_CLK signal occurs 25% later than the PIXEL_CLK signal
3. The inverse of the PIXEL_CLK signal occurs 50% later than the PIXEL_CLK signal
4. The inverse of the DELAYED_PIX_CLK signal occurs 75% later than the PIXEL_CLK signal

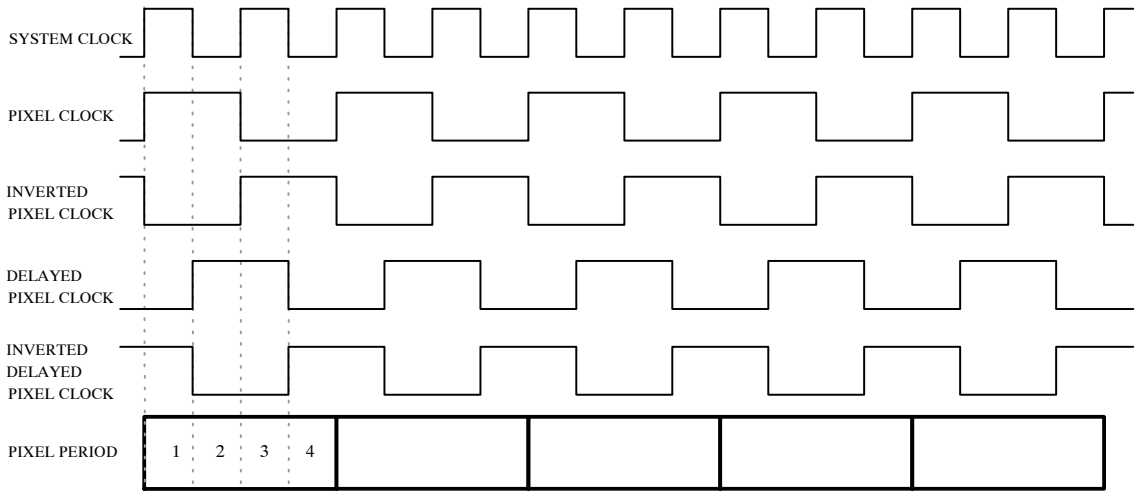

Figure 1. Pixel Clock Generation Timing

One of these four signals is chosen to be the input signal source for a particular pixel rate signal, and then the position of the signal is optimized using a programmable delay line IC.

TIMING GENERATOR STATE MACHINE DESCRIPTION

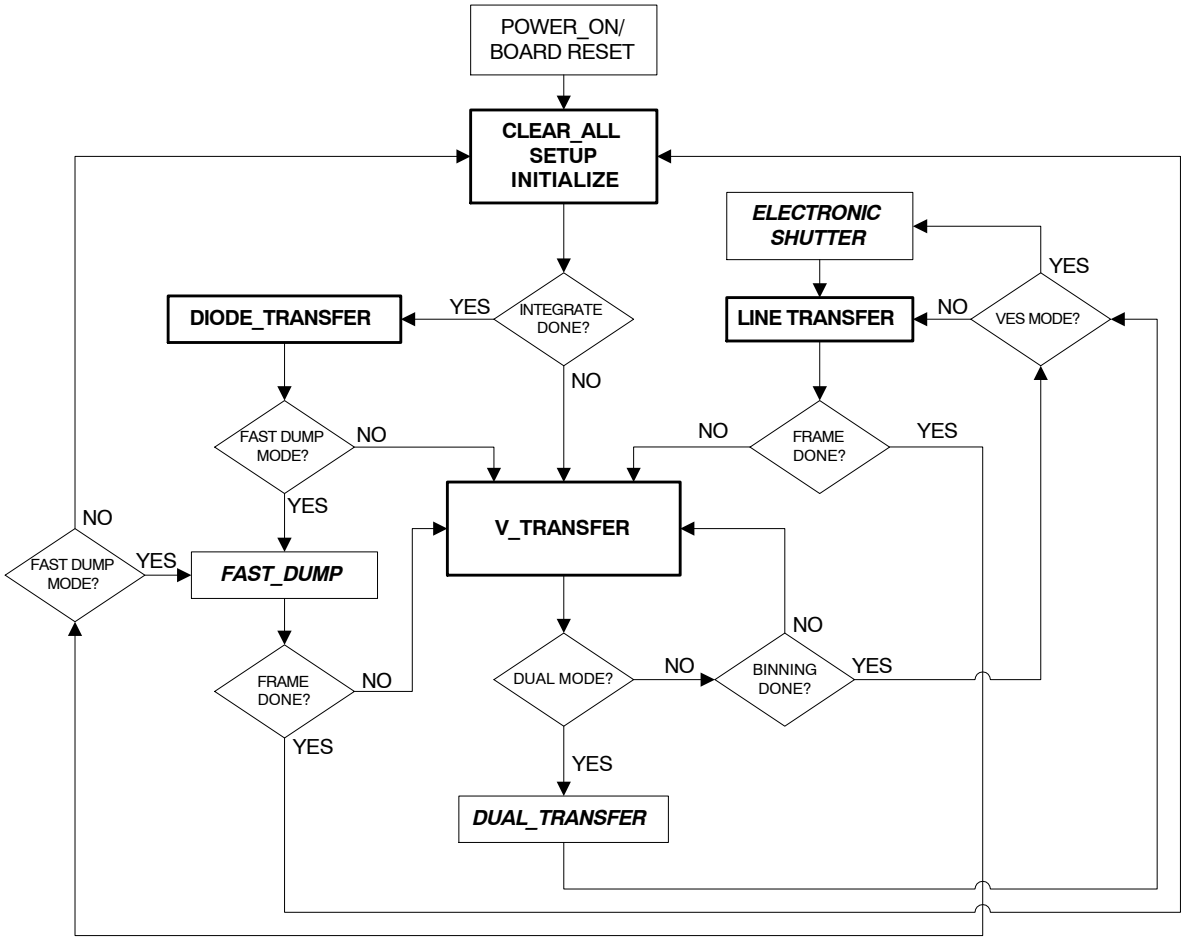

Figure 2. Timing Generator State Machine

Power−On / Board Reset Initialize State

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the ten delay line IC's on the board, and then serially load the initial default values into the AFE registers. Upon completion of the serial load of the AFE, the board will be ready to proceed according to the output mode selected.

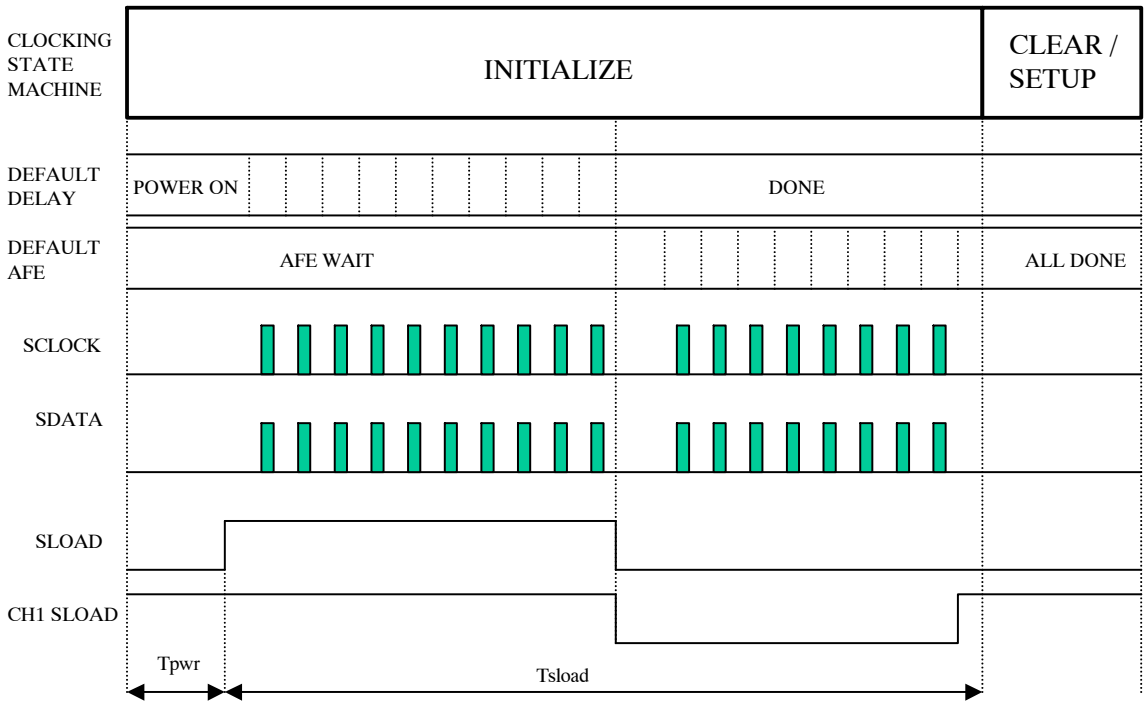

Figure 3. Power−On Initialization Timing

Delay Register Initialization

The DS1020 Programmable Silicon Delay Lines allow the Horizontal Clocks, Reset Clock, Clamp, Sample, and Data Clock signals to be adjusted within the sub−pixel timing. On Power−Up or Board Reset, the delay lines are programmed with values stored in the Altera device. These values are chosen to conform to the timing requirements of the CCD image sensor and to achieve optimum device performance (See Reference 1 for details). The delay values shown in Table 9 are typical values, and may vary on an individual Evaluation Board set.

For programming purposes, the silicon delay lines are cascaded, i.e., the serial output pin of device 1 is tied to the serial input pin of device 2 and so on. Therefore, when making an adjustment to one or more delay lines, all the delay lines must be reprogrammed. The total number of serial bits must be eight times the number of units daisy−chained and each group of 8 bits must be sent in MSB−to−LSB order (See Reference 3). The total delay on each output signal is calculated as:

$$Delay = 10.0 + 0.25 * [Delay\ Code]\ (ns)$$

Refer to the Dallas Semiconductor DS1020 Programmable Silicon Delay Line Specification Sheet (Reference 3) for details.

Table 10. DEFAULT DELAY IC PROGRAMMING

Delay IC Programming Order	Delay IC Output Signal	Delay IC Input Signal Source	Delay Code (Typical)	Delay (ns) (Typical)
1	AD9845 DATACLK	INVERTED PIXEL CLK	20	15.0
2	CH2 AD9845 SHP	INVERTED PIXEL CLK	24	16.0
3	CH1 AD9845 SHP	INVERTED PIXEL CLK	24	16.0
4	CH2 AD9845 SHD	PIXEL CLK	16	14.0
5	CH1 AD9845 SHD	PIXEL CLK	16	14.0
6	H1 CLOCK	INVERTED PIXEL CLK	20	15.0
7	H1BR CLOCK	INVERTED PIXEL CLK	26	16.5
8	H2 CLOCK	PIXEL CLK	20	15.0
9	H2BR CLOCK	PIXEL CLK	26	16.5
10	RESET CLOCK	PIXEL CLK	0	10.0

On power up or board−reset, the AFE registers are programmed to the default levels shown in Table 11. See the AD9845 specifications sheet (Reference 2) for details.

Table 11. DEFAULT AD9845 AFE REGISTER PROGRAMMING

Register	Description	Value (decimal)	Notes
0	Operation	128	
1	VGA Gain	418	Corresponds to a VGA stage gain of 12.6 dB
2	Clamp	96	The output of the AD9845 will be clamped to code 96 during the CLPOB period
3	Control	10	PXGA gain registers enabled
4	PXGA gain0	43	Corresponds to a CDS stage gain of 0 dB
5	PXGA gain1	43	Corresponds to a CDS stage gain of 0 dB
6	PXGA gain2	43	Corresponds to a CDS stage gain of 0 dB
7	PXGA gain3	43	Corresponds to a CDS stage gain of 0 dB

Clear / Setup State

The timing generator state machine is free running. It cycles through the states depending on the jumper settings and DIO inputs, and then returns back to the clear state to begin the next frame. At the beginning of each frame, the internal PLD counters are reset.

DIODE TRANSFER State

During the DIODE_TRANSFER state, the V1_CLK is brought to the high level and charge is transported from the photodiodes to the Vertical CCD's.

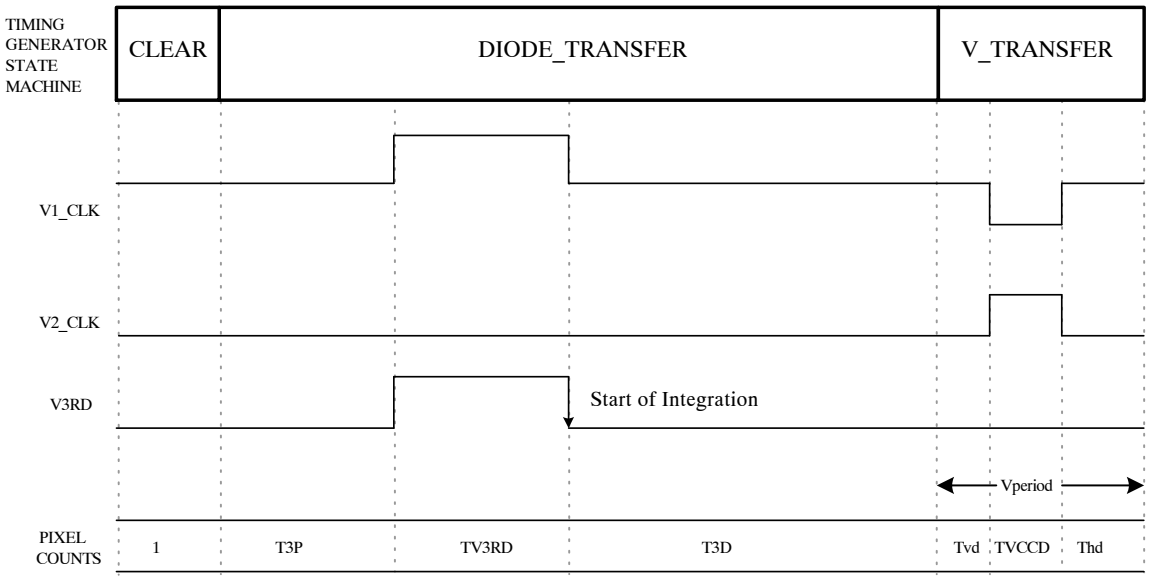

Figure 4. Diode Transfer Timing

The integration time can be adjusted to multiple frame times by prolonging the time between photodiode charge transfer using the input control lines D[11..9]. The effective integration time is the time between the transfer of charge from the photodiodes. The default integration mode is INT_MODE = 0, a single frame between photodiode transfer. In single output mode, multiple frame integration time is equal to:

$$T3P + TV3rd + T3D + [(Vperiod + PIX\_X * Tpix) * PIX\_Y] * (INT\_MODE + 1)$$

Table 12. SINGLE OUTPUT MULTI−FRAME INTEGRATION TIMES

INT_MODE DIO[11..9]	Integration Time (Frames)	Integration Time (ms)	Frame Rate (Fps)	Notes
0	1	13.812	72.4	Default
1	2	27.599	36.2	
2	3	41.387	24.2	
3	4	55.174	18.1	
4	5	68.962	14.5	
5	6	82.749	12.1	
6	7	96.537	10.4	
7	8	110.324	9.1	

In dual output mode, multiple frame integration time is equal to:

$$T3P + TV3rd + T3D + [(2 * Vperiod - 4 + PIX\_X * Tpix) * ½ PIX\_Y] * (INT\_MODE + 1)$$

Table 13. DUAL OUTPUT MULTI−FRAME INTEGRATION TIMES

INT_MODE DIO[11..9]	Integration Time (Frames)	Integration Time (ms)	Frame Rate (Fps)	Notes
0	1	7.9263	126.2	Default
1	2	15.8286	63.2	
2	3	23.7308	42.1	
3	4	31.633	31.6	
4	5	39.5353	25.3	
5	6	47.4375	21.1	
6	7	55.3398	18.1	
7	8	63.242	15.8	

V_TRANSFER State

During the V_TRANSFER state, each line (row) of charge is transported towards the horizontal CCD register using the Vertical clocks. A vertical transfer counter in the PLD is used to determine when the vertical clocks are forced high and low and when the vertical transfer time and horizontal delay time (Thd) are completed (Figure 5).

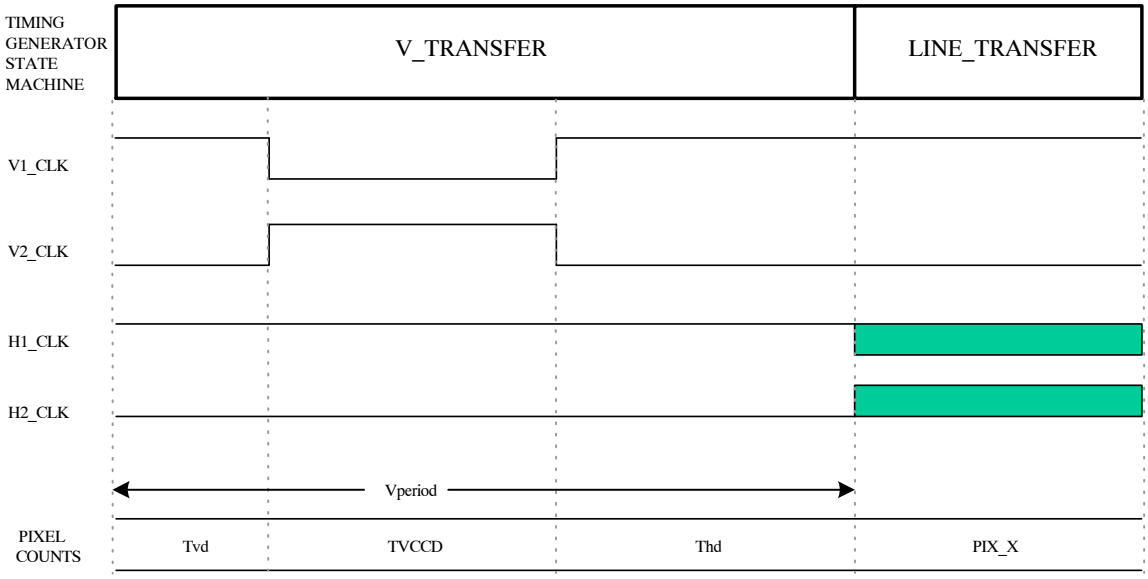

Figure 5. Vertical Transfer Timing

Dual Output Mode Option

When operating in Dual Output mode, two lines of charge are transferred into the horizontal CCD registers. During the second line transfer, the H1A_CLK is asserted low to transfer the first line into the CCD Horizontal Register B. The two lines are then clocked out in parallel to achieve an almost twofold increase in frame rate (Figure 6).

Binning Mode Option

When operating in 2x2 binning mode, two lines of charge are transferred into the CCD Horizontal Register A and allowed to accumulate before being clocked towards the output (Figure 7).

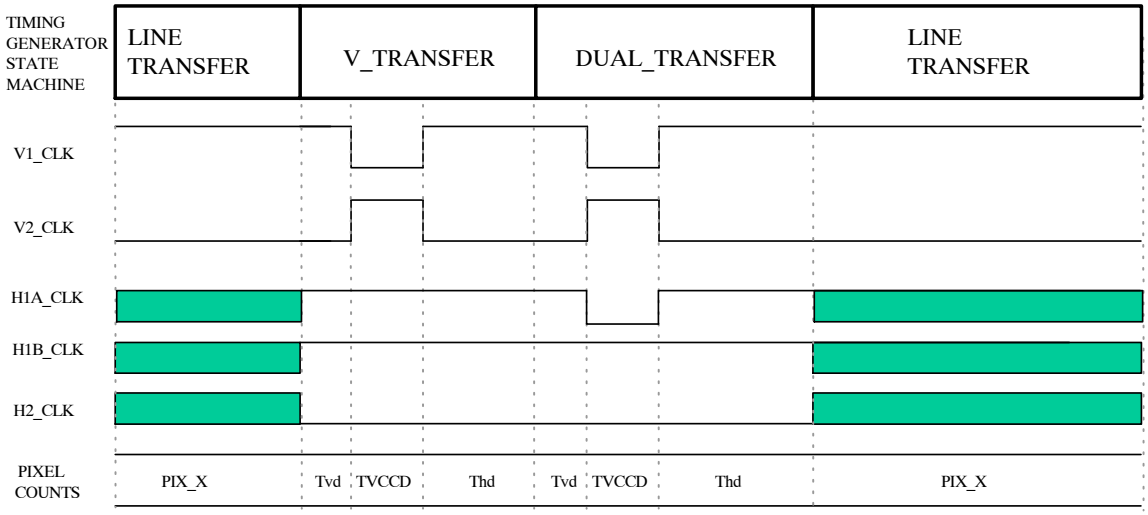

Figure 6. Vertical Transfer Timing – Dual Output Mode

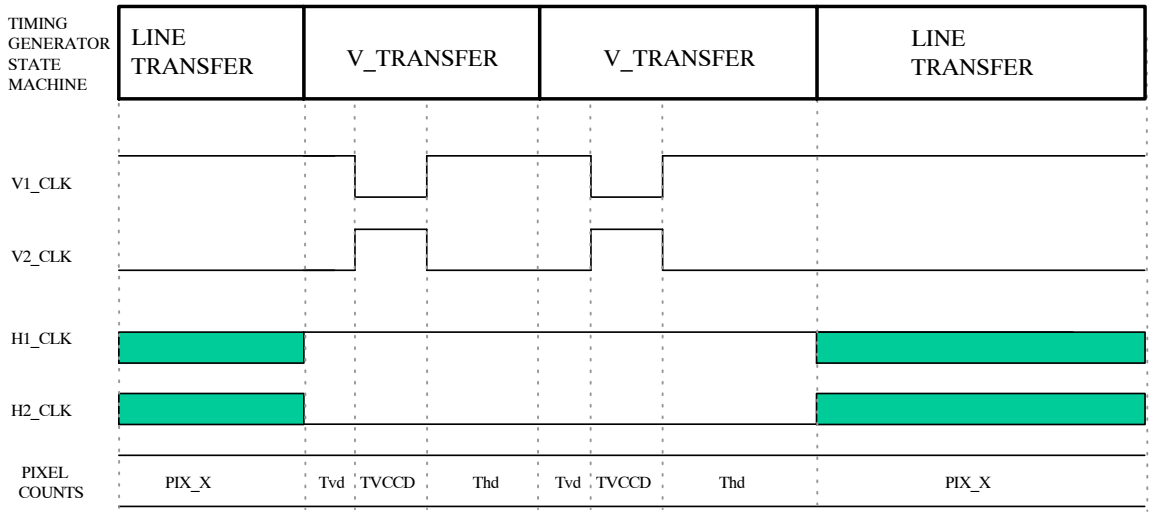

Figure 7. Vertical Transfer Timing – 2x2 Binning Mode

Fast Dump Mode Option

When operating in Fast Dump Mode, horizontal clocks are suspended while 100 lines of charge are rapidly dumped to the CCD's horizontal register at the start of the frame, and another 100 lines are dumped at the end of the frame. In this way only the middle 296 lines of the image are read out (Figure 8).

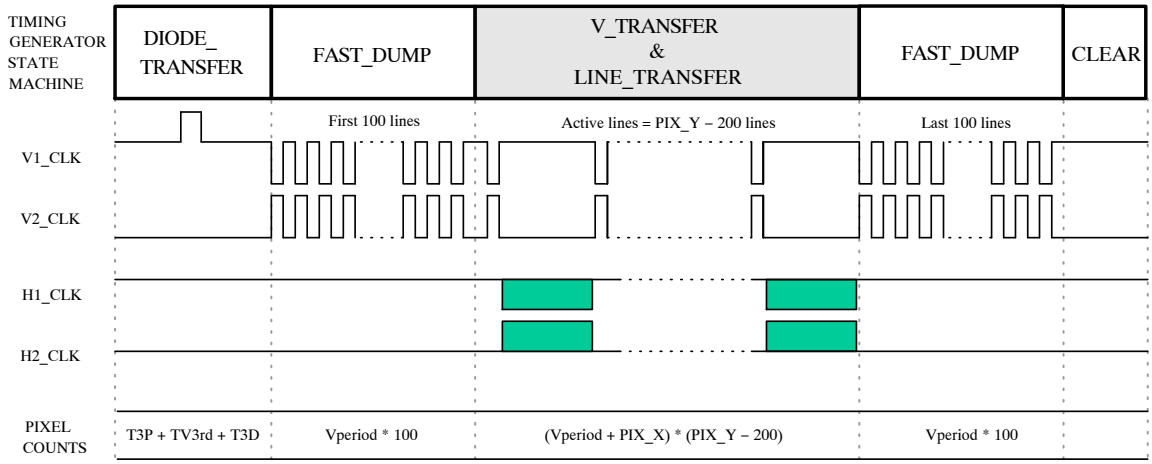

Figure 8. Fast Dump Gate Timing

Electronic Shutter State

The integration time can be adjusted to be smaller than one frame time by electronic shuttering of the device. Using the input control lines D[8..6], the line on which the electronic shutter will occur can be selected. The effective integration time is then the time between when the electronic shutter occurred and the next transfer of charge from the photodiodes. The default electronic shutter mode is 0, no electronic shutter.

In Single Output mode, Electronic Shutter Mode integration time is equal to:

$$Tsd + [(Vperiod + PIX\_X * Tpix) * (PIX\_Y - VES\_LINE)] - Vperiod + T3P + TV3rd$$

Table 14. SINGLE OUTPUT ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE DIO[8..6]	VES_LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0		1	13.812	Default
1	62	0.875	12.08	
2	124	0.75	10.36	
3	186	0.625	8.63	
4	248	0.5	6.91	
5	310	0.375	5.19	
6	372	0.25	3.46	
7	434	0.125	1.74	

In Dual Output mode, Electronic Shutter Mode integration time is equal to:

$$Tsd + [(2 * Vperiod + PIX\_X * Tpix) * (½\ PIX\_Y - VES\_LINE)] - 2 * Vperiod + T3P + TV3rd$$

Table 15. DUAL OUTPUT ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE DIO[8..6]	VES_LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0		1	7.9263	Default
1	62	0.75	5.94	
2	124	0.5	3.96	
3	186	0.25	1.99	
4	248	1	7.9263	1
5	310	1	7.9263	1
6	372	1	7.9263	1
7	434	1	7.9263	1

1. No Electronic Shutter, the VES_LINE number is greater than the number of lines per channel in Dual Output Mode.

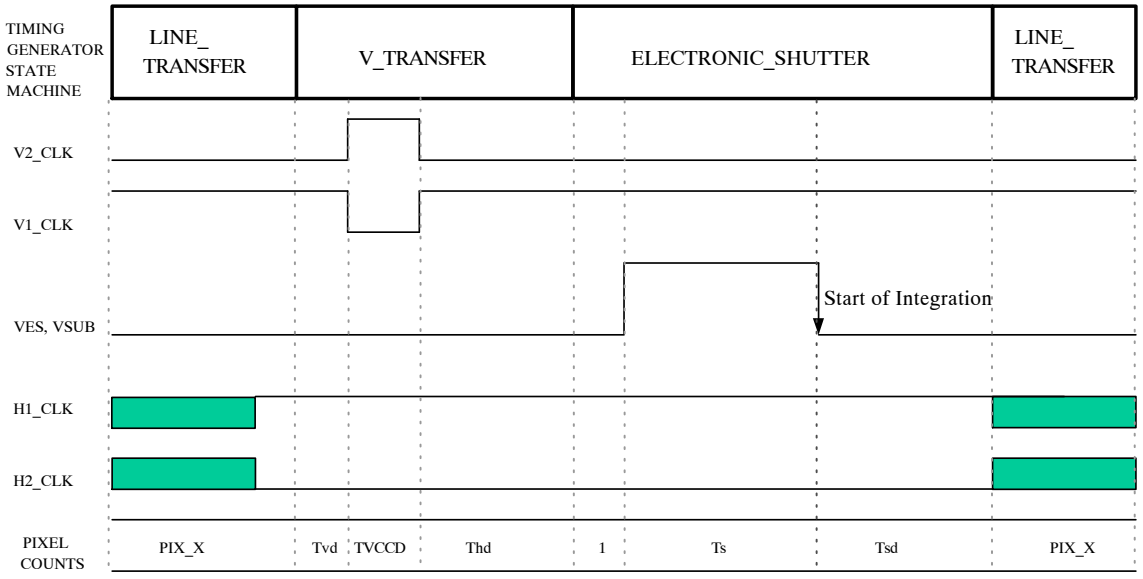

Figure 9. Electronic Shutter Timing – Single Output

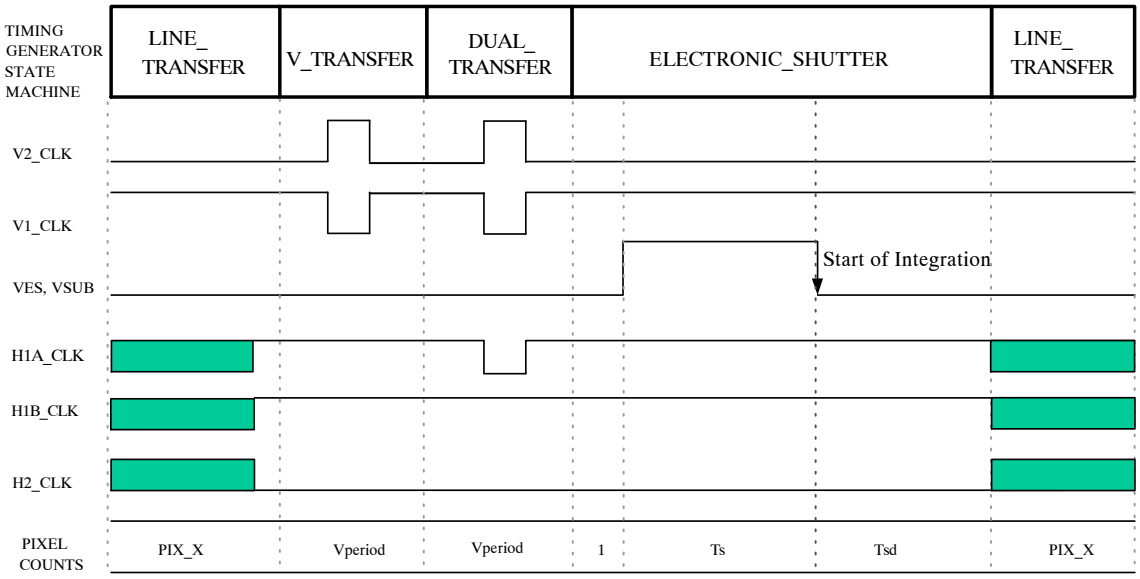

Figure 10. Electronic Shutter Timing − Dual Output

LINE_TRANSFER State

During the LINE_TRANSFER state, charge is transported to the CCD output structure pixel by pixel. A line transfer counter in the PLD is used to keep track of how many pixels have been transported, and to synchronize the AD9845 timing signals and the PCI−1424 timing signals with the appropriate pixels (dark pixels for black clamping, for example).

At the end of each line transfer, the Line counter is incremented. If all of the lines have been clocked out of the CCD., the state machine goes back to the CLEAR / SETUP state, if not, the state machine goes back and transfers another line of charge into the horizontal register.

In 2x2 binning mode, two registers of charge, each containing two pixels, are summed in the CCD's floating diffusion before being clocked out of the device. The 2x2 binning mode can be selected using output control jumpers (See Table 7). When using a horizontal binning mode other that the default setting (no binning), the pixel rate delays may have to be re−adjusted and re−synchronized to achieve optimal performance.

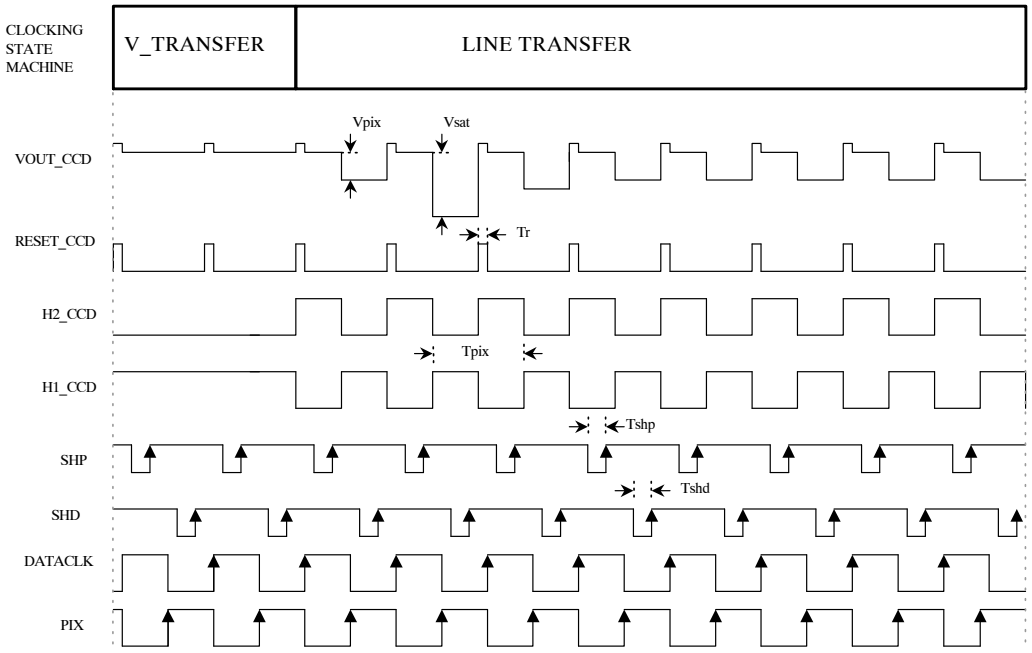

Figure 11. Horizontal Timing − Line Transfer

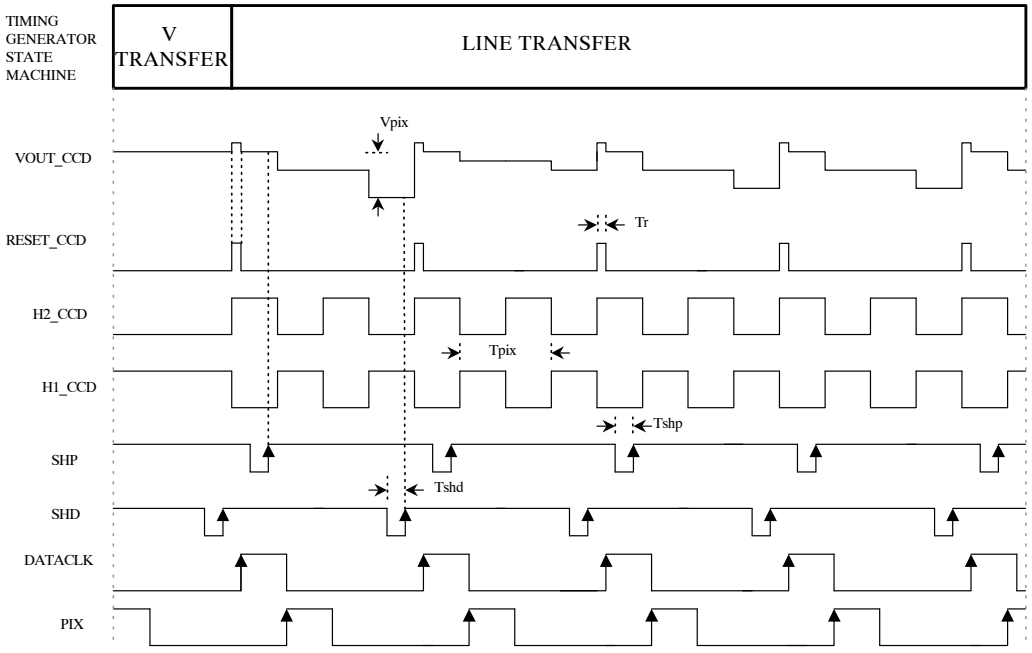

Figure 12. Horizontal Timing − 2x2 Binning Mode Line Transfer

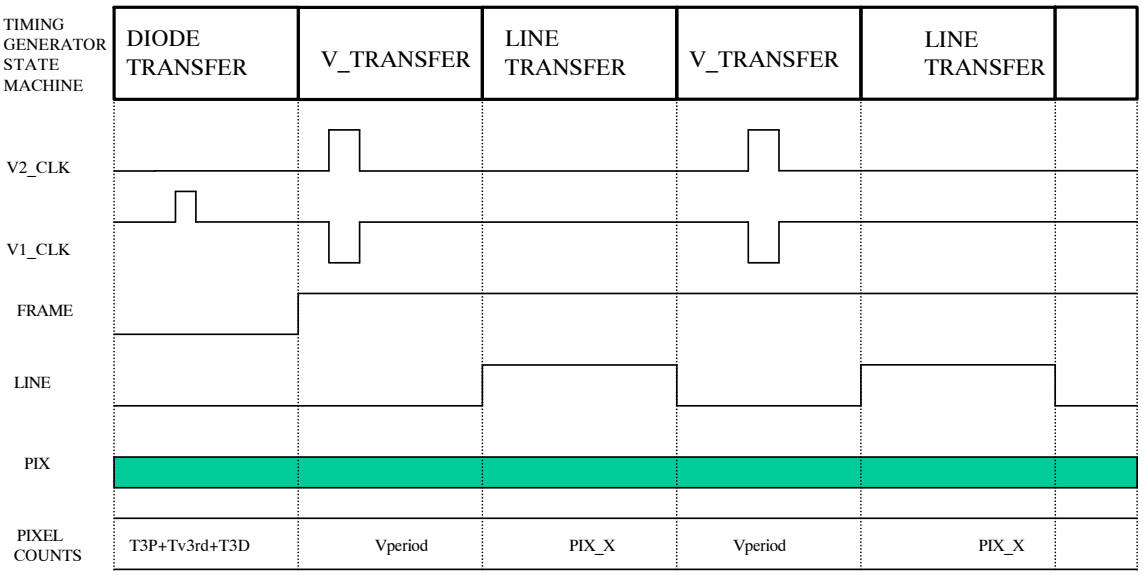

Figure 13. PCI−1424 Frame Grabber Timing

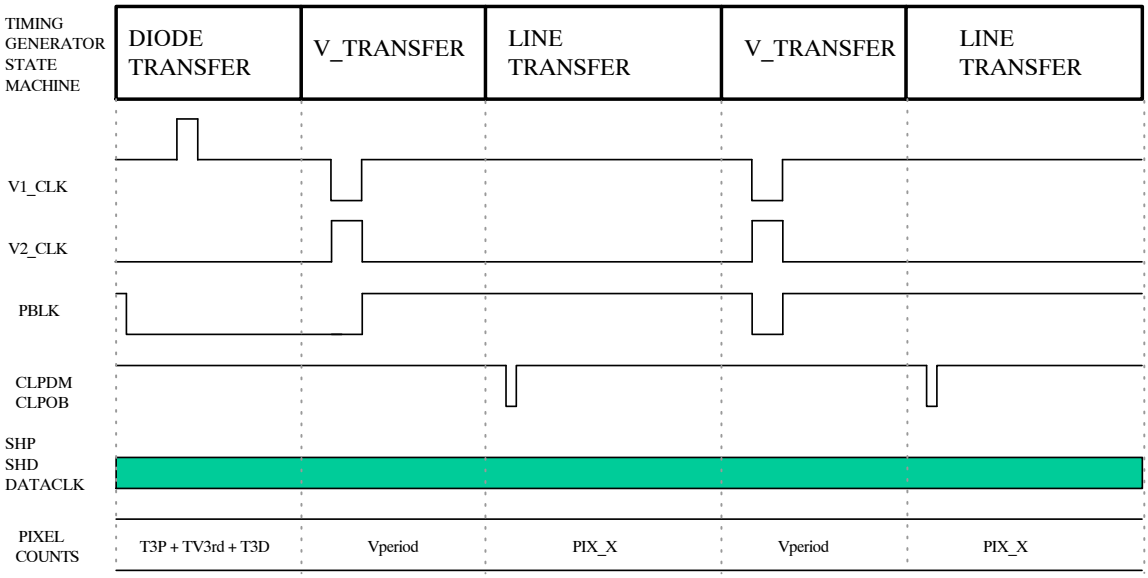

Figure 14. AD9845 Timing

Warnings and Advisories

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
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References

- KAF−0330 Device Specification
- KAF−0330 Imager Board User Manual
- KAF−0330 Imager Board Schematic
- AD984X Timing Generator Board User Manual
- AD984X Timing Generator Board Schematic
- Analog Devices AD9845 Product Data Sheet (28 and 30 MHz operation)

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