



# +3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

MAX3627

## General Description

The MAX3627 is a low-jitter, precision clock generator optimized for network applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) to generate high-frequency clock outputs for Ethernet applications.

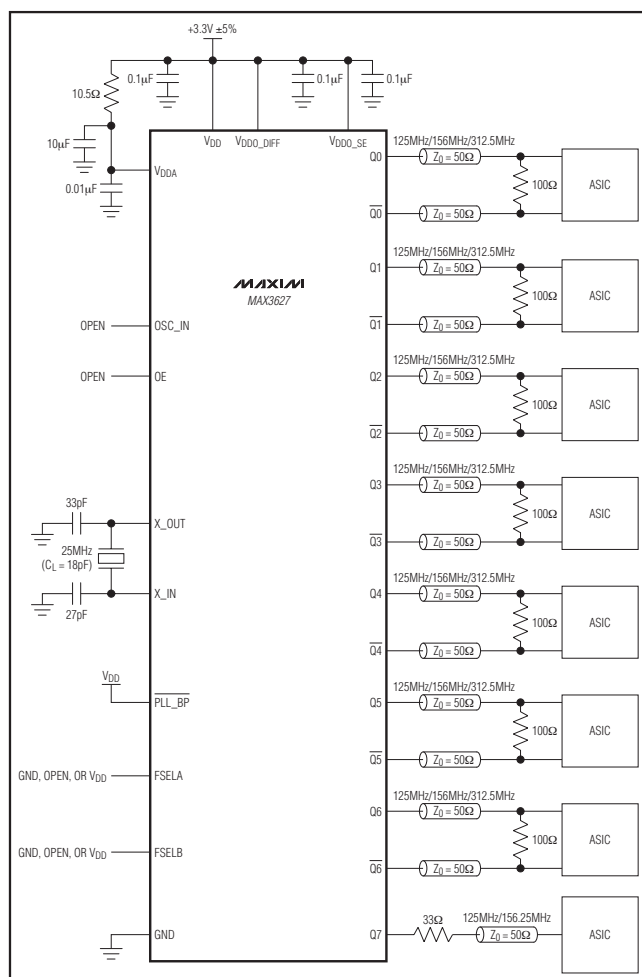
Maxim's proprietary PLL design features ultra-low jitter (0.4psRMS) and excellent power-supply noise rejection (PSNR), minimizing design risk for network equipment.

The MAX3627 contains seven LVDS outputs and one LVCMOS output. The output frequencies are selectable among 125MHz, 156.25MHz, and 312.5MHz.

## Applications

Ethernet Networking Equipment

## Typical Operating Circuit



## Features

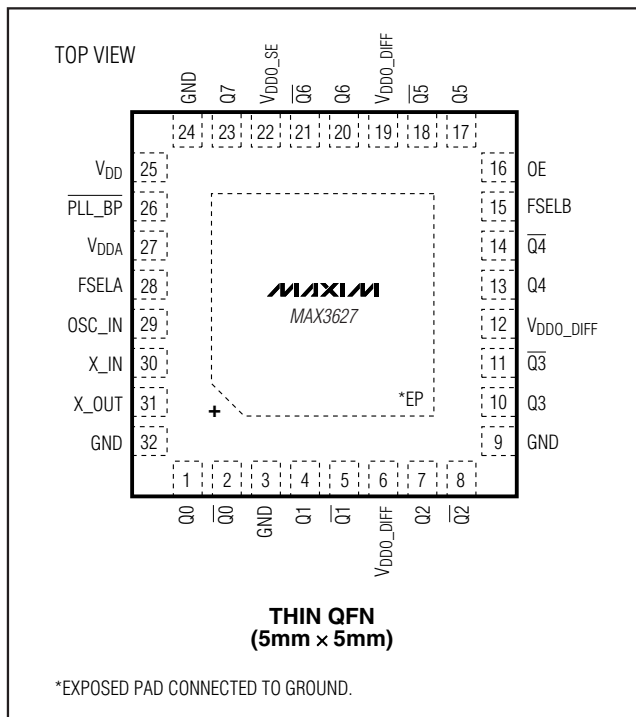
- ◆ **Crystal Oscillator Interface: 25MHz**
- ◆ **OSC\_IN Interface**  
 PLL Enabled: 25MHz  
 PLL Disabled: 20MHz to 320MHz
- ◆ **Outputs**  
 One LVDS Output at 125MHz/156.25MHz/  
 312.5MHz (Selectable with FSELA)  
 Six LVDS Outputs at 125MHz/156.25MHz/  
 312.5MHz (Selectable with FSELB)  
 One LVCMOS Output at 125MHz/156.25MHz  
 (Selectable with FSELB)
- ◆ **Low Phase Jitter**  
 0.4psRMS (12kHz to 20MHz)  
 0.2psRMS (1.875MHz to 20MHz)
- ◆ **Excellent PSNR: -64dBc at 156.25MHz with  
 40mVp-p Supply Noise at 100kHz**
- ◆ **Operating Temperature Range: 0°C to +70°C**

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3627CTJ+	0°C to +70°C	32 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.  
 \*EP = Exposed pad.

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range at V<sub>DD</sub>, V<sub>DDA</sub>,  
 V<sub>DDO\_SE</sub>, V<sub>DDO\_DIFF</sub> .....-0.3V to +4.0V  
 Voltage Range at Q0, Q0, Q1, Q1, Q2, Q2,  
 Q3, Q3, Q4, Q4, Q5, Q5, Q6, Q6, Q7,  
 PLL\_BP, FSELA, FSELB, OE, OSC\_IN ...-0.3V to (V<sub>DD</sub> + 0.3V)  
 Voltage Range at X\_IN .....-0.3V to +1.2V

Voltage Range at X\_OUT .....-0.3V to (V<sub>DD</sub> - 0.6V)  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 32-Pin TQFN-EP (derate 34.5mW/°C above +70°C)..2759mW  
 Operating Junction Temperature Range .....-55°C to +150°C  
 Storage Temperature Range .....-65°C to +160°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +3.0V to +3.6V, T<sub>A</sub> = 0°C to +70°C, unless otherwise noted. Typical values are at V<sub>DD</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted. When using X\_IN, X\_OUT input, no signal is applied at OSC\_IN. When PLL is enabled, PLL\_BP = high-Z or high. When PLL is bypassed, PLL\_BP = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current (Note 2)	I <sub>DD</sub>	PLL enabled		190	256	mA
		PLL bypassed		175		
<b>LVDS OUTPUTS (Q0, Q0, Q1, Q1, Q2, Q2, Q3, Q3, Q4, Q4, Q5, Q5, Q6, Q6)</b>						
Output High Voltage	V <sub>OH</sub>				1.475	V
Output Low Voltage	V <sub>OL</sub>		0.925			V
Differential Output Voltage Amplitude	V <sub>ODI</sub>	Figure 1	250		400	mV
Change in Magnitude of Differential Output for Complementary States	Δ V <sub>ODI</sub>				25	mV
Output Offset Voltage	V <sub>OS</sub>		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	Δ V <sub>OS</sub>				25	mV
Differential Output Impedance			80	105	140	Ω
Output Current		Shorted together		5		mA
		Short to ground (Note 3)		8		
Clock Output Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>	20% to 80%, R <sub>L</sub> = 100Ω	100	200	330	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 4)	46	50	54	
<b>LVC MOS/LVTTL OUTPUT (Q7)</b>						
Output Frequency					160	MHz
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -12mA	2.6		V <sub>DD</sub>	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12mA			0.4	V
Output Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>	20% to 80% at 125MHz (Note 5)	0.15	0.4	0.8	ns
Output Duty-Cycle Distortion		PLL enabled	46	50	54	%
		PLL bypassed (Note 4)	45	50	55	
Output Impedance	R <sub>OUT</sub>			15		Ω

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. When using X\_IN, X\_OUT input, no signal is applied at OSC\_IN. When PLL is enabled,  $\overline{PLL\_BP} = \text{high-Z}$  or high. When PLL is bypassed,  $\overline{PLL\_BP} = \text{low}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT SPECIFICATIONS (FSELA, FSELB, PLL_BP, OE)</b>						
Input-Voltage High	$V_{IH}$		2.0		$V_{DD}$	V
Input-Voltage Low	$V_{IL}$		0		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			80	$\mu A$
Input Low Current	$I_{IL}$	$V_{IN} = 0$	-80			$\mu A$
<b>LVCOS/LVTTL INPUT SPECIFICATIONS (OSC_IN) (Note 6)</b>						
Input Clock Frequency		PLL enabled		25		MHz
		PLL bypassed	20		320	
Input Amplitude Range		(Note 7)	1.2		3.6	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			80	$\mu A$
Input Low Current	$I_{IL}$	$V_{IN} = 0$	-80			$\mu A$
Reference Clock Duty Cycle			40	50	60	%
Input Capacitance	$C_{IN}$			1.5		pF
<b>CLOCK OUTPUT AC SPECIFICATIONS</b>						
VCO Center Frequency				625		MHz
Output Frequency with PLL Enabled (Q0)		FSELA = GND		125		MHz
		FSELA = $V_{DD}$		156.25		
		FSELA = high-Z		312.5		
Output Frequency with PLL Enabled (Q1 to Q7)		FSELB = GND		125		MHz
		FSELB = $V_{DD}$		156.25		
		FSELB = high-Z (Note 8)		312.5		
Output Frequency with PLL Disabled		LVDS outputs	20		320	MHz
		LVCOS output	20		160	
Integrated Phase Jitter	$R_{JRMS}$	12kHz to 20MHz, $\overline{PLL\_BP} = \text{high}$ (Note 9)		0.4	1.0	psRMS
		12kHz to 20MHz, $\overline{PLL\_BP} = \text{high-Z}$ (Note 10)		0.4		
Power-Supply Noise Rejection (Note 11)	PSNR	LVDS outputs		-64		dBc
		LVCOS output		-49		
Deterministic Jitter Due to Supply Noise (Note 12)		LVDS outputs		2.5		psp-P
		LVCOS output		18		
Nonharmonic and Subharmonic Spurs		(Note 13)		-70		dBc
LVDS Clock Output SSB Phase Noise at 125MHz (Note 14)		$f = 100\text{Hz}$		-115		dBc/Hz
		$f = 1\text{kHz}$		-124		
		$f = 10\text{kHz}$		-126		
		$f = 100\text{kHz}$		-130		
		$f = 1\text{MHz}$		-143		
		$f > 10\text{MHz}$		-149		

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. When using X\_IN, X\_OUT input, no signal is applied at OSC\_IN. When PLL is enabled,  $\overline{PLL\_BP} = \text{high-Z}$  or high. When PLL is bypassed,  $\overline{PLL\_BP} = \text{low}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS Clock Output SSB Phase Noise at 125MHz (Note 14)		f = 100Hz		-113		dBc/Hz
		f = 1kHz		-123		
		f = 10kHz		-126		
		f = 100kHz		-130		
		f = 1MHz		-144		
		f > 10MHz		-151		

- Note 1:** A series resistor of up to  $10.5\Omega$  is allowed between  $V_{DD}$  and  $V_{DDA}$  for filtering supply noise when system power-supply tolerance is  $V_{DD} = 3.3V \pm 5\%$ . See Figure 4.
- Note 2:** All outputs unloaded.
- Note 3:** The current when an LVDS output is shorted to ground is the steady-state current after the detection circuitry has settled. It is expected that the LVDS output short to ground condition is short-term only.
- Note 4:** Measured with OSC\_IN input with 50% duty cycle.
- Note 5:** Measured with a series resistor of  $33\Omega$  to a load capacitance of  $3.0pF$ . See Figure 2.
- Note 6:** The OSC\_IN input can be DC- or AC-coupled.
- Note 7:** Must be within the absolute maximum rating of  $V_{DD} + 0.3V$ .
- Note 8:** AC characteristics of LVCMOS output (Q7) are only guaranteed up to 160MHz.
- Note 9:** Measured with 25MHz crystal (with OSC\_IN left open).
- Note 10:** Measured with 25MHz reference clock applied to OSC\_IN.
- Note 11:** Measured with  $40mV_{P-P}$  sinusoidal signal on the supply at 100kHz. For LVDS the output frequency is 156.25MHz; for LVCMOS the output frequency is 125MHz. Measured with a  $10.5\Omega$  resistor between  $V_{DD}$  and  $V_{DDA}$ .
- Note 12:** Parameter calculated based on PSNR.
- Note 13:** Measurement includes XTAL oscillator feedthrough, crosstalk, intermodulation spurs, etc.
- Note 14:** Measured with 25MHz XTAL oscillator.

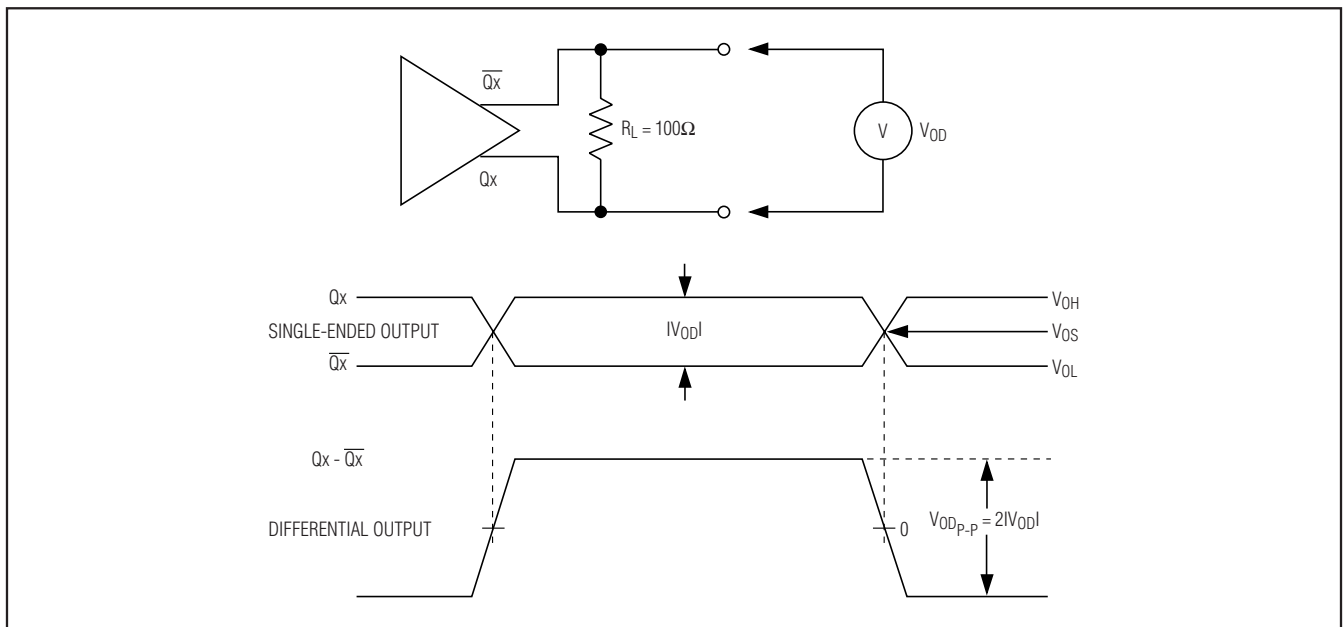


Figure 1. Driver Output Levels

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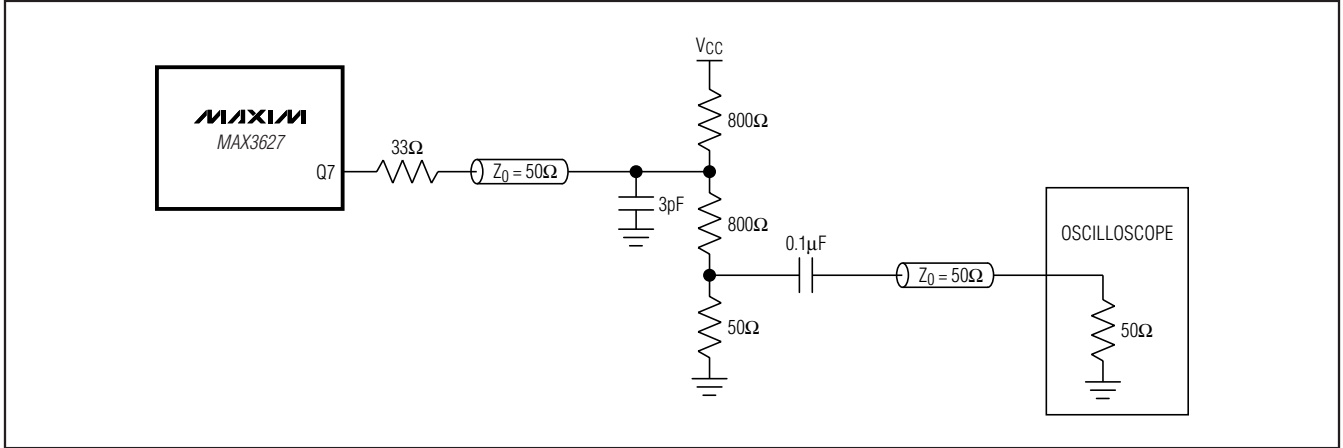
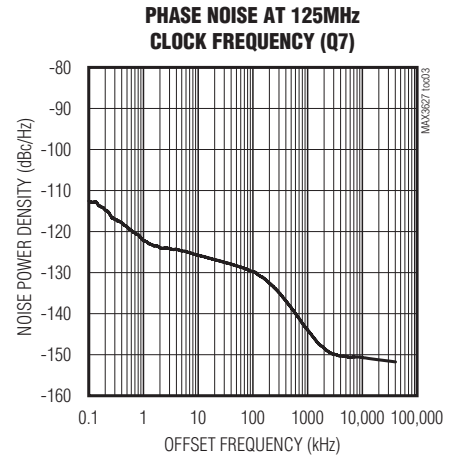
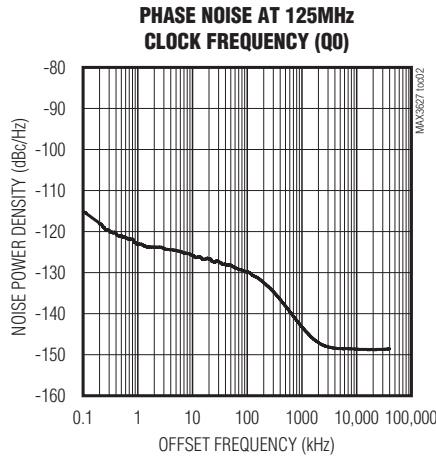
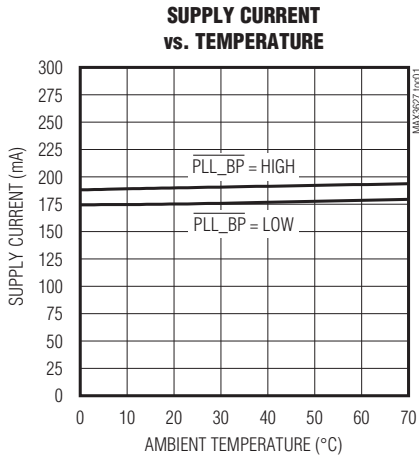


Figure 2. LVC MOS Output Measurement Setup

## Typical Operating Characteristics

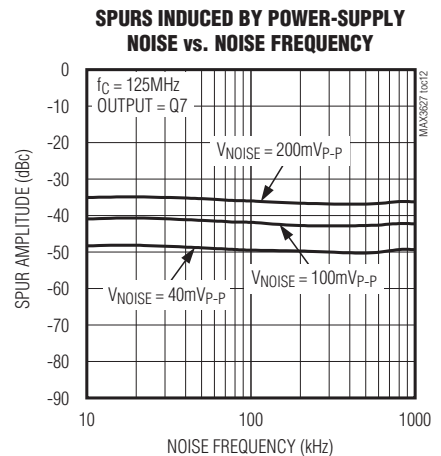
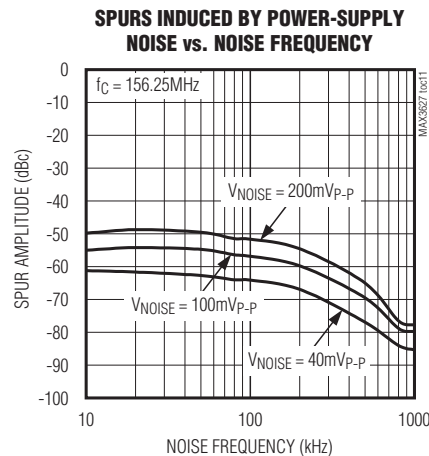
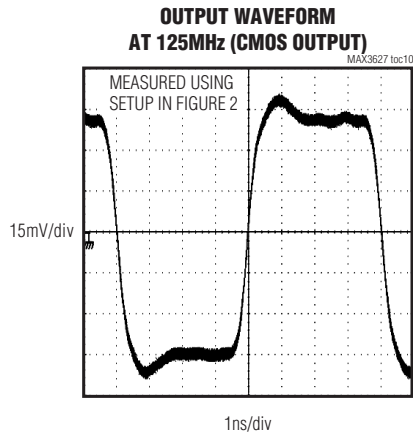
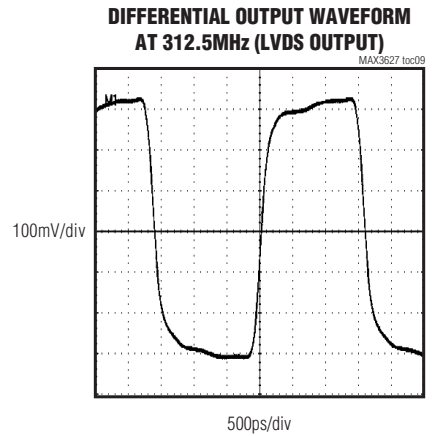
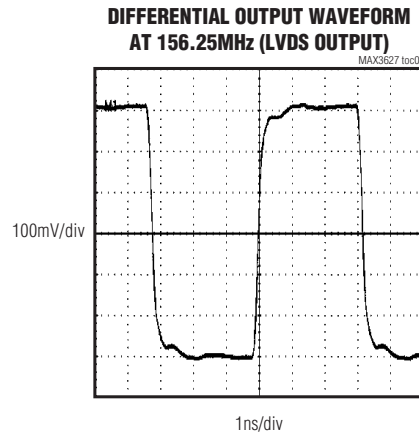
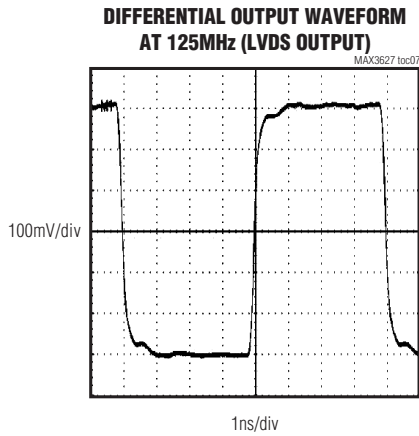
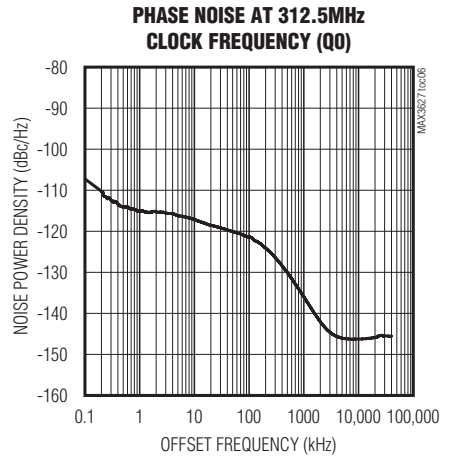
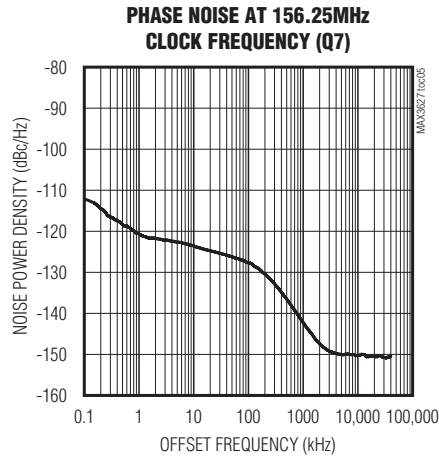
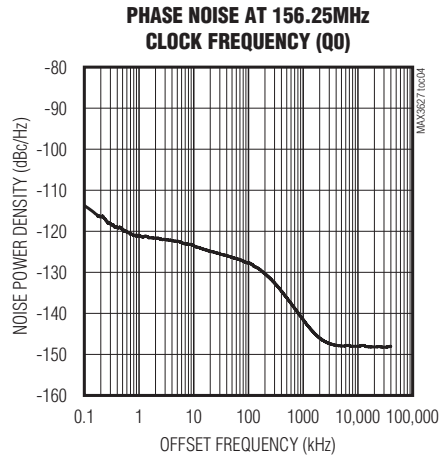
(Typical values are at  $V_{DD} = +3.3V$ ,  $T_A = +25^\circ C$ , crystal frequency = 25MHz.)



# +3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

## Typical Operating Characteristics (continued)

(Typical values are at  $V_{DD} = +3.3V$ ,  $T_A = +25^\circ C$ , crystal frequency = 25MHz.)



# +3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

## Pin Description

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PIN	NAME	FUNCTION
1	Q0	LVDS, Noninverting Clock Output
2	$\overline{Q0}$	LVDS, Inverting Clock Output
3, 9, 24, 32	GND	Supply Ground
4	Q1	LVDS, Noninverting Clock Output
5	$\overline{Q1}$	LVDS, Inverting Clock Output
6, 12, 19	VDDO_DIFF	Power Supply for Q0, Q1, Q2, Q3, Q4, Q5, and Q6 Clock Outputs. Connect to +3.3V.
7	Q2	LVDS, Noninverting Clock Output
8	$\overline{Q2}$	LVDS, Inverting Clock Output
10	Q3	LVDS, Noninverting Clock Output
11	$\overline{Q3}$	LVDS, Inverting Clock Output
13	Q4	LVDS, Noninverting Clock Output
14	$\overline{Q4}$	LVDS, Inverting Clock Output
15	FSELB	Three-State LVCMOS/LVTTL Input. Controls the Q1 to Q7 output divider. When connected to logic-low, the output frequency is 125MHz. When connected to logic-high, the output frequency is 156.25MHz. When left open (high-Z), the output frequency is 312.5MHz. For the Q7 LVCMOS output, the output specification is only valid up to 160MHz.
16	OE	LVCMOS/LVTTL Input. Enable/disable control for the Q4, Q5, and Q6 outputs. The OE pin has an internal 75k $\Omega$ pullup resistor. When OE is connected to V <sub>DD</sub> or left open, Q4, Q5, and Q6 are enabled. When OE is connected to GND, Q4, Q5, and Q6 are disabled to reduce power consumption. When disabled, Q4, Q5, and Q6 are high impedance.
17	Q5	LVDS, Noninverting Clock Output
18	$\overline{Q5}$	LVDS, Inverting Clock Output
20	Q6	LVDS, Noninverting Clock Output
21	$\overline{Q6}$	LVDS, Inverting Clock Output
22	VDDO_SE	Power Supply for Q7 Clock Output. Connect to +3.3V.
23	Q7	LVCMOS Clock Output
25	VDD	Core Power Supply. Connect to +3.3V.
26	$\overline{PLL\_BP}$	Three-State LVCMOS/LVTTL Input (Active Low). When connected to logic-high, the PLL locks to the crystal interface (25MHz typical at X_IN and X_OUT). When left open (high-Z), the PLL locks to the OSC_IN input (25MHz typical). When connected to logic-low, the PLL is bypassed and the OSC_IN input is selected. When bypass mode is selected, the VCO/PLL is disabled to save power and eliminate intermodulation spurs.
27	VDDA	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can be connected to V <sub>DD</sub> through a 10.5 $\Omega$ resistor as shown in Figure 4.
28	FSELA	Three-State LVCMOS/LVTTL Input. Controls the Q0 output divider. When connected to logic-low, the output frequency is 125MHz. When connected to logic-high, the output frequency is 156.25MHz. When left open (high-Z), the output frequency is 312.5MHz.
29	OSC_IN	LVCMOS Input. Self-biased to allow AC- or DC-coupling. When $\overline{PLL\_BP}$ is open, the OSC_IN input frequency should be 25MHz. When the PLL is in bypass mode ( $\overline{PLL\_BP}$ = low), the OSC_IN input frequency can be between 20MHz and 320MHz. When $\overline{PLL\_BP}$ is high, the OSC_IN should be disconnected.
30	X_IN	Crystal Oscillator Input
31	X_OUT	Crystal Oscillator Output
—	EP	Exposed Pad. Connect to GND for proper electrical and thermal performance.

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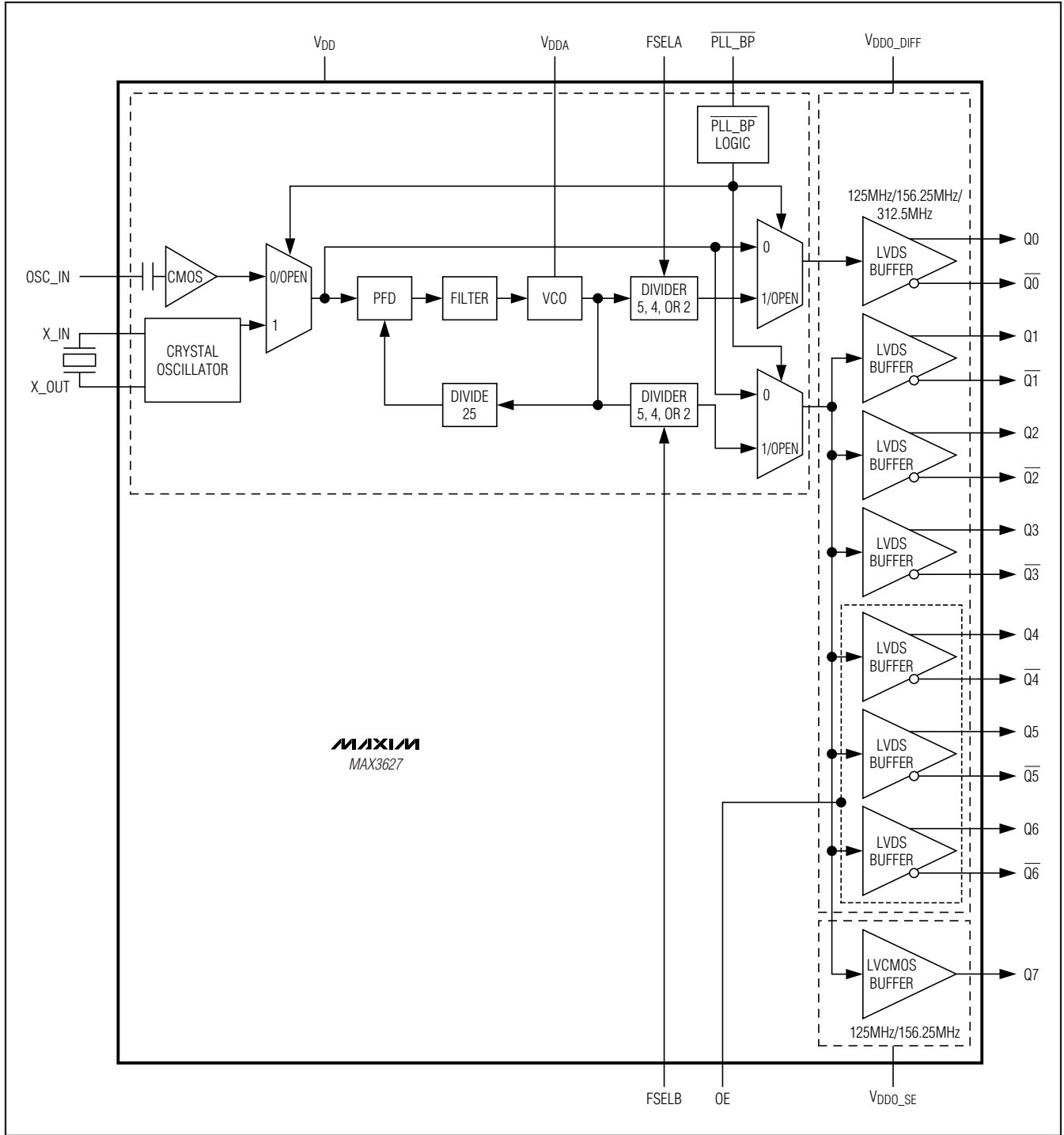


Figure 3. Functional Diagram



# +3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

## Detailed Description

The MAX3627 is a frequency generator designed to operate at Ethernet frequencies. It consists of an on-chip crystal oscillator, PLL, LVCMOS output buffer, and LVDS output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance. The outputs can be switched among 125MHz, 156.25MHz, and 312.5MHz.

### Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X\_IN and X\_OUT. The crystal frequency is 25MHz. See the *Applications Information* section for more information.

### OSC\_IN Buffer

The LVCMOS OSC\_IN buffer is internally biased to allow AC- or DC-coupling. This input is internally AC-coupled, and is designed to operate at 25MHz when the PLL is enabled (PLL\_BP is left open). When the PLL is bypassed (PLL\_BP is set low), the OSC\_IN buffer can be operated from 20MHz to 320MHz.

### PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO) that operates at 625MHz. The PLL bandwidth is tuned to 150kHz typical to optimize both phase noise and power-supply noise rejection (PSNR). The VCO output is connected to the PFD input through a feedback divider that divides the VCO frequency by 25 to lock onto the 25MHz reference clock or oscillator. For output Q0, the FSELA pin is used to select among 125MHz, 156.25MHz, and 312.5MHz. For outputs Q1 to Q6, the FSELB pin is used to select among 125MHz, 156.25MHz, and 312.5MHz. For the Q7 output, the FSELB pin is used to select between 125MHz and 156.25MHz. To minimize the jitter induced by power-supply noise, the VCO supply (VDDA) is isolated from the core logic and output buffer supplies.

### LVDS Drivers

The high-frequency outputs—Q0, Q1, Q2, Q3, Q4, Q5, and Q6—are differential LVDS buffers designed to drive 100Ω.

### LVCMOS Driver

LVCMOS output Q7 is provided on the MAX3627. It is designed to drive single-ended high-impedance loads. The output specifications are only valid up to 160MHz.

## Applications Information

### Power-Supply Filtering

The MAX3627 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation, in addition to excellent on-chip power-supply rejection, this part provides a separate power-supply pin, VDDA, for the VCO circuitry. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. Figure 4 illustrates the recommended power-supply filter network for VDDA. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins and placed as close as possible to the pins for best performance.

### Crystal Input Layout and Frequency Stability

The MAX3627 features an integrated on-chip crystal oscillator to minimize system implementation cost. The integrated crystal oscillator is a Pierce-type that uses the crystal in its parallel resonance mode. It is recommended to use a 25MHz crystal with a load specification of  $C_L = 18\text{pF}$ . See Table 1 for the recommended crystal specifications.

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X\_IN and X\_OUT pins to minimize the board parasitic capacitance and prevent active signals from coupling into the oscillator.

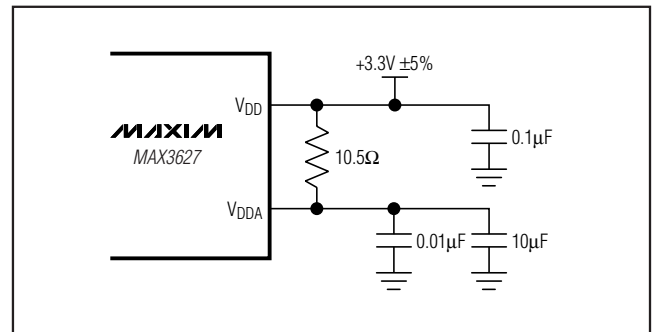


Figure 4. Analog Supply Filtering

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Table 1. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	$f_{osc}$		25		MHz
Shunt Capacitance	$C_0$			7.0	pF
Load Capacitance	$C_L$		18		pF
Equivalent Series Resistance (ESR)	$R_s$			50	$\Omega$
Maximum Crystal Drive Level				300	$\mu W$

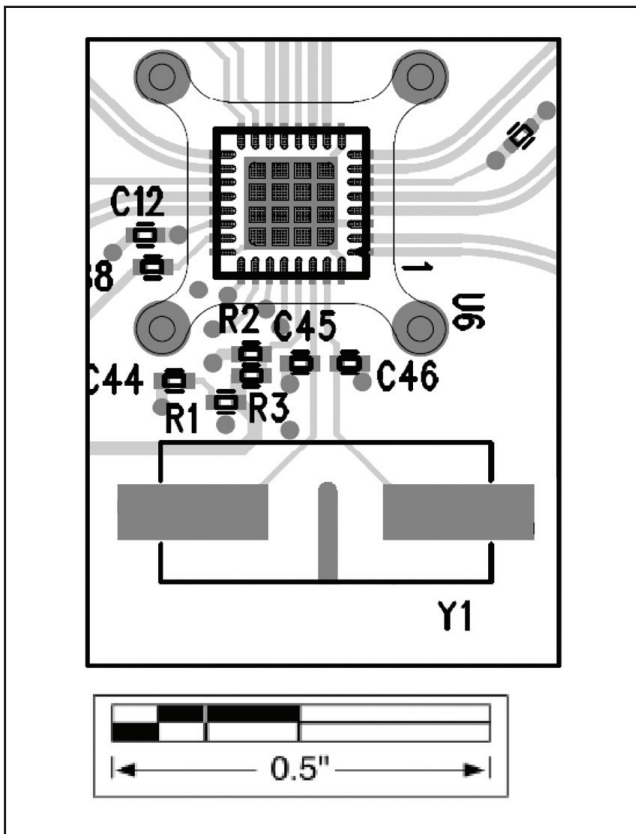


Figure 5. Crystal Layout

The layout shown in Figure 5 gives approximately 2pF of trace plus footprint capacitance per side of the crystal (Y1). The dielectric material is FR4, and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C45 = 27pF and C46 = 33pF, the measured output frequency accuracy is -1ppm at +25°C ambient temperature.

### Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 1 for recommended crystal specifications. See Figure 6 for external capacitance connection.

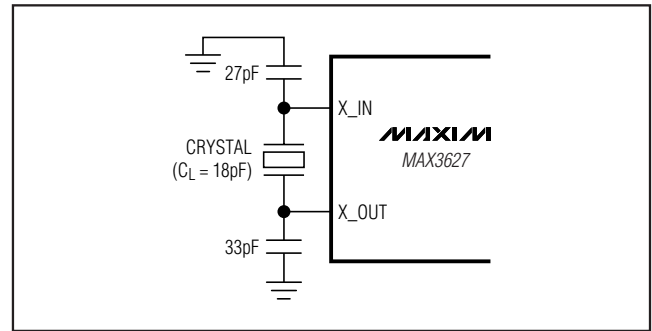


Figure 6. Crystal, Capacitors Connection

# +3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

## Interface Models

Figures 7, 8, and 9 show examples of interface models.

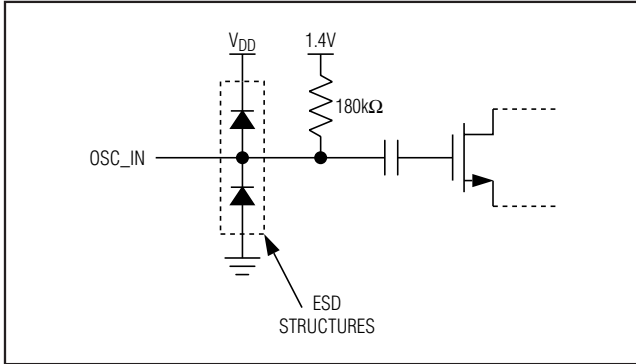


Figure 7. Simplified OSC\_IN Pin Circuit Schematic

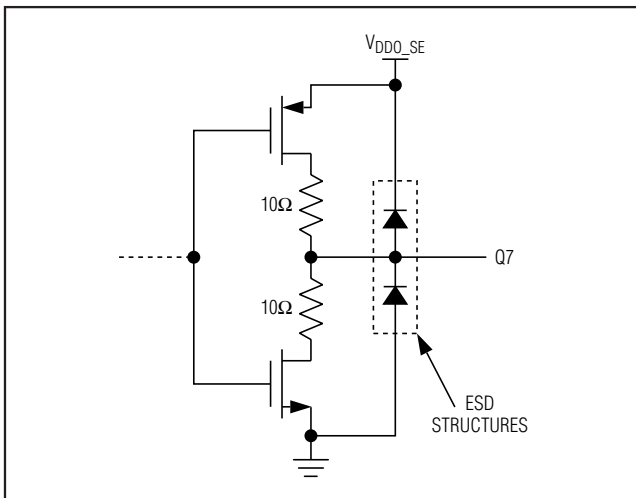


Figure 8. Simplified LVCMOS Output Circuit Schematic

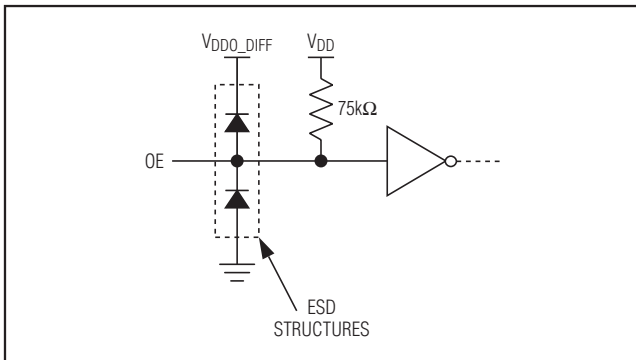


Figure 9. Simplified OE Pin Circuit Schematic

## Layout Considerations

The inputs and outputs are the most critical paths for the MAX3627 and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3627:

- An uninterrupted ground plane should be positioned beneath the clock outputs. The ground plane under the crystal should be removed to minimize capacitance.
- Ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3627 and the receive devices.
- Supply decoupling capacitors should be placed close to the supply pins, preferably on the same layer as the MAX3627.
- Take care to isolate crystal input traces from the MAX3627 outputs.
- The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X\_IN and X\_OUT pins.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance into and out of the part.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3627 evaluation kit for more information.

## Exposed-Pad Package

The exposed pad on the 32-pin TQFN package provides a very low inductance path for return current traveling to the PCB ground plane. The pad is thermal and electrical ground on the MAX3627 and must be soldered to the circuit board ground for proper electrical performance.

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255+5	<a href="#">21-0140</a>

# **+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs**

## **Revision History**

<b>REVISION NUMBER</b>	<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
0	4/09	Initial release.	—
1	12/09	Corrected errors in Figure 3.	8

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