

NB3N508S

3.3V, 216 MHz PureEdge VCXO Clock Generator with M-LVDS Output

Description

The NB3N508S is a high precision, low phase noise Voltage Controlled Crystal Oscillator (VCXO) and phase lock loop (PLL) that generates 216 MHz M-LVDS output from a 27 MHz crystal. The ± 100 ppm output pullable range is obtained using the V_{IN} pin of the VCXO with usable range from 0 V to 3.3 V. The VCXO input pin V_{IN} is a high-impedance input that can be driven directly from a pulse width modulated RC integrator circuit.

The NB3N508S is designed primarily for data and clock recovery applications within end products such as ADSL modems, set-top box receivers, and telecom systems. This device is housed in 5.0 mm x 4.4 mm narrow body TSSOP-16 pin package.

Features

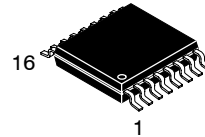
- PureEdge Clock Family Provides Accuracy and Precision
- Performs Precision Clock Multiplication from 27 MHz Crystal
- Uses 27 MHz Fundamental Mode Crystal
- External Loop Filter is Not Required
- 216 MHz M-LVDS Output
- VCXO with Pull Range ± 100 ppm
- 0 V to 3.3 V VCXO Tuning Voltage Range Capabilities
- Phase Noise:

| Offset | Noise Power |
|---------|-------------|
| 100 Hz | -80 dBc |
| 1 kHz | -88 dBc |
| 10 kHz | -105 dBc |
| 100 kHz | -106 dBc |
| 1 MHz | -120 dBc |
| 10 MHz | -145 dBc |
- Operating Range 3.3 V $\pm 5\%$
- These are Pb-Free Devices*



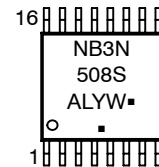
ON Semiconductor®

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TSSOP-16
DT SUFFIX
CASE 948F

MARKING DIAGRAM



- A = Assembly Location
 - L = Wafer Lot
 - Y = Year
 - W = Work Week
 - = Pb-Free Package
- (Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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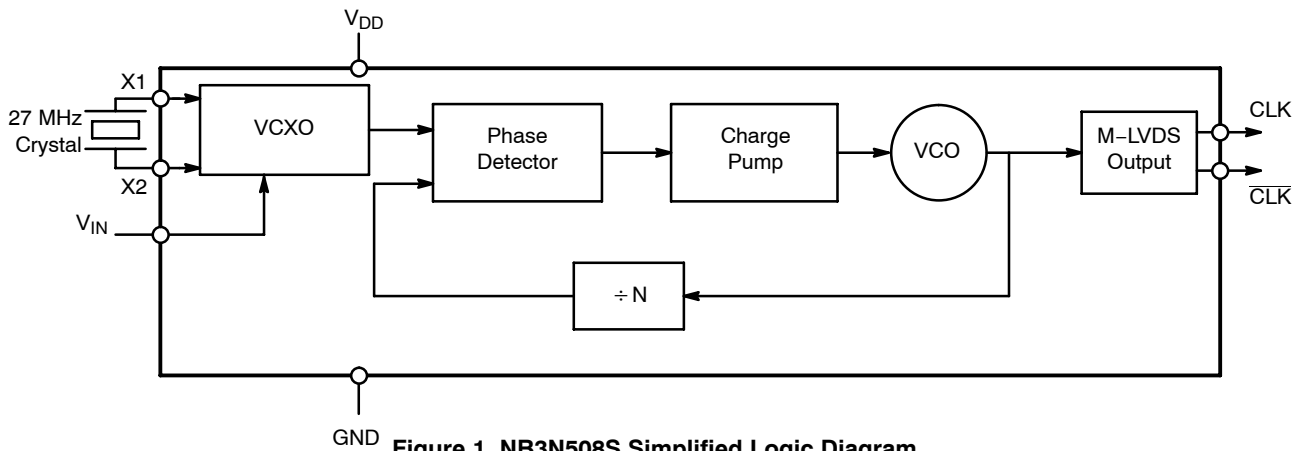


Figure 1. NB3N508S Simplified Logic Diagram

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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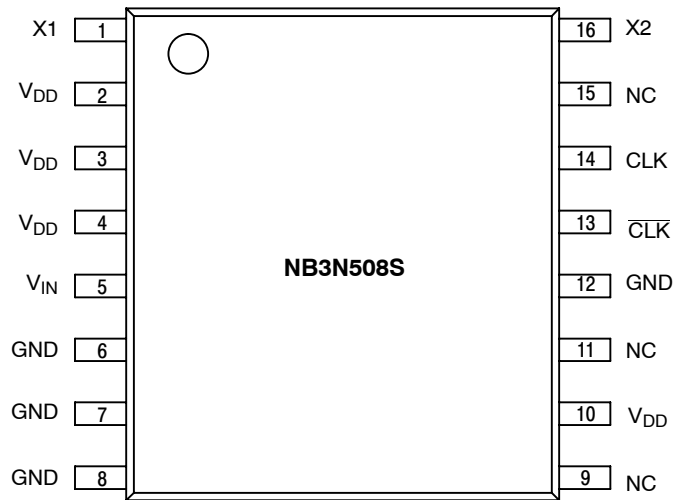


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-------------|-----------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | X1 | Crystal Input | Crystal input(IN). Connect to a 27 MHz crystal. |
| 2, 3, 4, 10 | V _{DD} | Power Supply | Positive power supply voltage. |
| 5 | V _{IN} | Input | Analog voltage input pin that controls output oscillation frequencies. V _{IN} pin range is from 0 V to 3.3 V. V _{IN} voltage should not exceed V _{DD} . |
| 6, 7, 8, 12 | GND | Power Supply | Ground 0 V. These pins provide GND return path for the devices. |
| 9, 11, 15 | NC | - | No Connect. |
| 13 | CLK | M-LVDS Output | Inverted clock output. Typically loaded with 50 Ω receiver termination resistor across diff. pair. |
| 14 | CLK | M-LVDS Output | Noninverted clock output. Typically loaded with 50 Ω receiver termination resistor across diff. pair. |
| 16 | X2 | Crystal Input | Crystal input(OUT). Connect to a 27 MHz crystal. |

Recommended Crystal Parameters

| | |
|--------------------------------------|---------|
| Crystal Fundamental AT-Cut Frequency | 27 MHz |
| Load Capacitance | 14 pF |
| Shunt Capacitance, C0 | 7 pF |
| Max Equivalent Series Resistance | 35 Ω |
| Max Initial Accuracy at 25°C | ±20 ppm |
| Temperature Stability | ±30 ppm |
| Aging | ±20 ppm |
| C0/C1 Ration | 250 Max |

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Table 2. ATTRIBUTES

| Characteristics | Value |
|---------------------------------------------------------------------------|----------------------|
| ESD Protection Human Body Model Machine Model | > 4 kV > 400 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) TSSOP-16 | Level 3 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 6000 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|------------------------------------------|---------------------|----------------------------------------|-----------------|--------------|
| V _{DD} | Positive Power Supply | GND = 0 V | | 4.6 | V |
| V _I | Input Voltage (V _{IN}) | GND = 0 V | GND ≤ V _I ≤ V _{DD} | V _{DD} | V |
| I _{OUT} | M-LVDS Output Current | Continuous Surge | | 25 50 | mA mA |
| T _A | Operating Temperature Range | | | 0 to +70 | °C |
| T _{STG} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-16 TSSOP-16 | 138 108 | °C/W °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Case) | (Note 2) | TSSOP-16 | 33 to 36 | °C/W |
| T _{SOL} | Wave Solder Pb-Free | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board - 2S2P (2 Signal, 2 Power).

Table 4. DC CHARACTERISTICS (V_{DD} = 3.135 V to 3.465 V, GND = 0 V, T_A = 0°C to +70°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|------------------|-------------------------------------------------------------------------------------|-----|------|------|------|
| I _{DD} | Power Supply Current (outputs loaded with R _L = 50 Ω) | 42 | 52 | 62 | mA |
| V _{IA} | VCXO Control Voltage, V _{IN} | 0 | | 3.3 | V |
| V _{OD} | Differential Output Voltage (Note 3) | 480 | 565 | 650 | mV |
| ΔV _{OD} | Change in Magnitude of V _{OD} for Complementary Output States (Notes 3, 6) | -50 | | 50 | mV |
| V _{OS} | Offset Voltage (See Figure 4) | 300 | | 2100 | mV |
| ΔV _{OS} | Change in Magnitude of V _{OS} for Complementary Output States (Note 6) | -50 | | 50 | mV |
| V _{OH} | Output HIGH Voltage (Note 4) | | 1300 | 2425 | mV |
| V _{OL} | Output LOW Voltage (Note 5) | -25 | 700 | | mV |
| I _{SC} | Output Short Circuit Current CLK or CLK to GND | | | 43 | mA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. M-LVDS outputs require 50 Ω receiver termination resistor between differential pair. See Figure 3

4. V_{OHmax} = V_{OSmax} + ½ V_{ODmax}.

5. V_{OLmax} = V_{OSmin} - ½ V_{ODmax}.

6. Parameters guaranteed by design but not tested in production.

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Table 5. AC CHARACTERISTICS ($V_{DD} = 3.135\text{ V}$ to 3.465 V , $GND = 0\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Note 7)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------------------------------|-----|--------|
| f_{CLKIN} | Crystal Input Frequency | | 27 | | MHz |
| f_{CLKOUT} | Output Clock Frequency | | 216 | | MHz |
| Φ_{NOISE} | Phase-Noise Performance $f_{CLKOUT} = 216\text{ MHz}$ @ 100 Hz Offset from Carrier @ 1 kHz Offset from Carrier @ 10 kHz Offset from Carrier @ 100 kHz Offset from Carrier @ 1 MHz Offset from Carrier @ 10 MHz Offset from Carrier | | -80 -88 -105 -106 -120 -145 | | dBc/Hz |
| | Spurious Noise Components | | -60 | | dBc/Hz |
| F_P | Crystal Pullability $0\text{ V} \leq V_{IN} \leq 3.3\text{ V}$ | ± 100 | | | ppm |
| t_{DUTY_CYCLE} | Output Clock Duty Cycle (Measured at Crosspoint) | 45 | 50 | 55 | % |
| t_R | Output Rise Time (CLK/CLK) (Note 8) | | 380 | 500 | ps |
| t_F | Output Fall Time (CLK/CLK) (Note 8) | | 380 | 500 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. CLK/CLK loaded with $50\ \Omega$ receiver termination resistor between diff. pair.
8. Measured differentially (CLK - CLK) at 10% to 90%; $R_L = 50\ \Omega$.

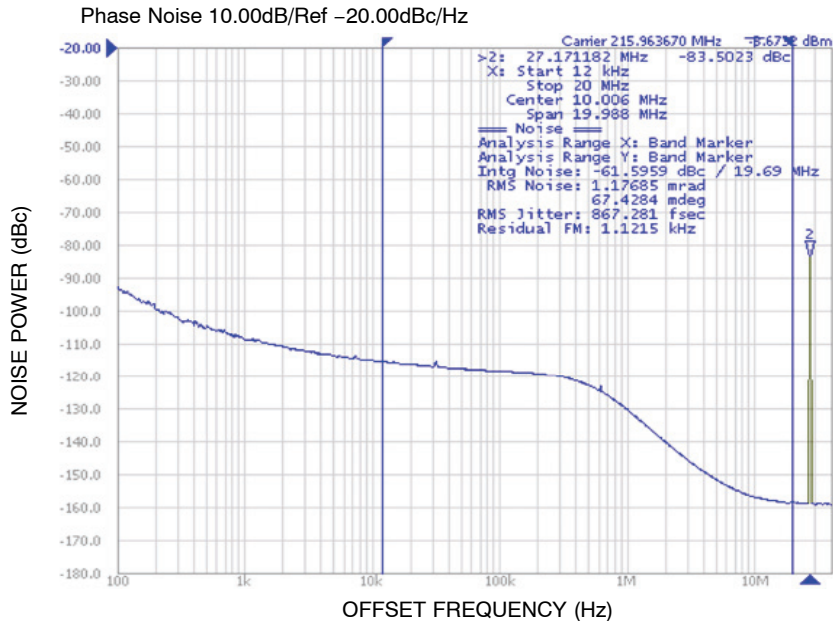


Figure 3. Typical Phase Noise Plot ($V_{DD} = 3.3\text{ V}$, $V_{IN} = 0\text{ V}$; Room Temperature)

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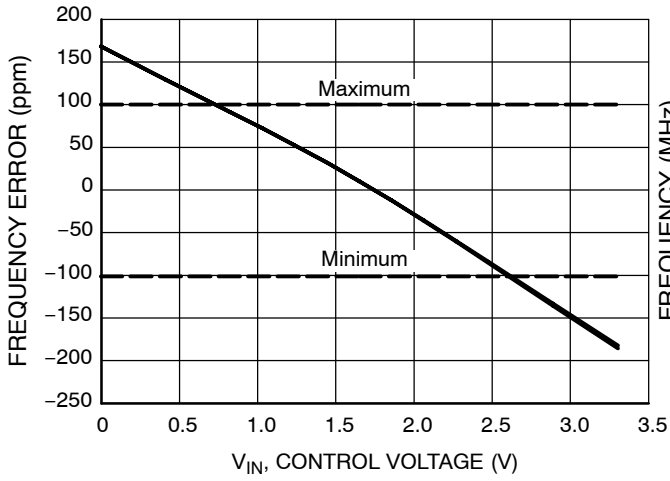


Figure 4. VCXO Pulling Range

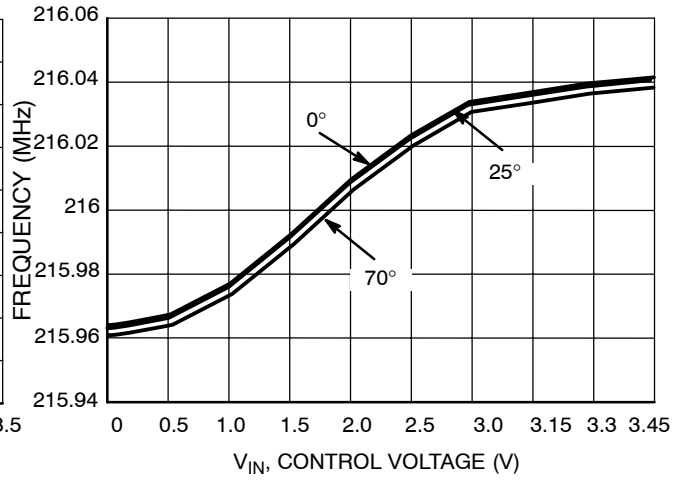


Figure 5. Output Clock Frequency vs. V_{IN} and Temperature

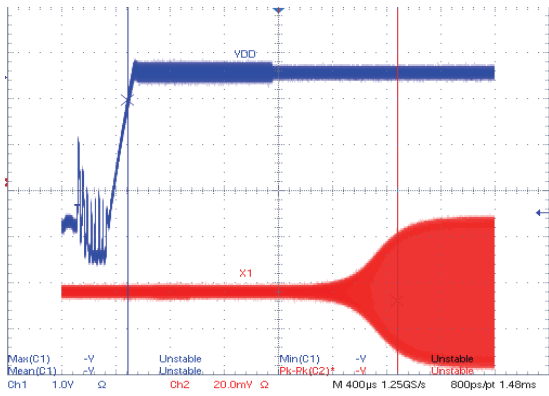


Figure 6. Typical Crystal Startup Time with $V_{IN} = 0$ V at Ambient Temperature (1.99 ms)

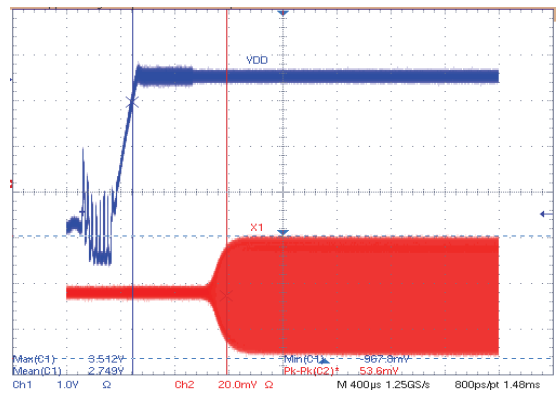


Figure 7. Typical Crystal Startup Time with $V_{IN} = 3.3$ V at Ambient Temperature (694 μ s)

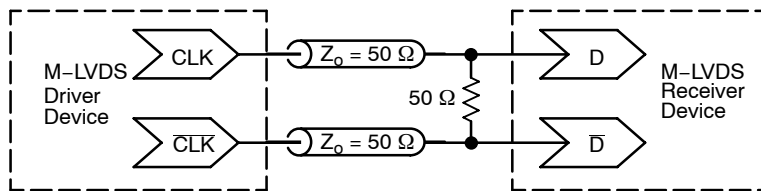


Figure 8. Typical Termination for Output Driver and Device Evaluation

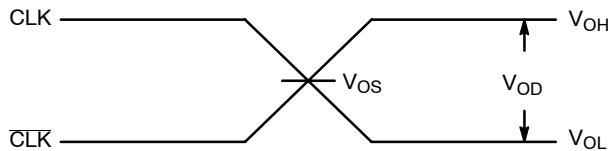


Figure 9. H-LVDS Output

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ORDERING INFORMATION

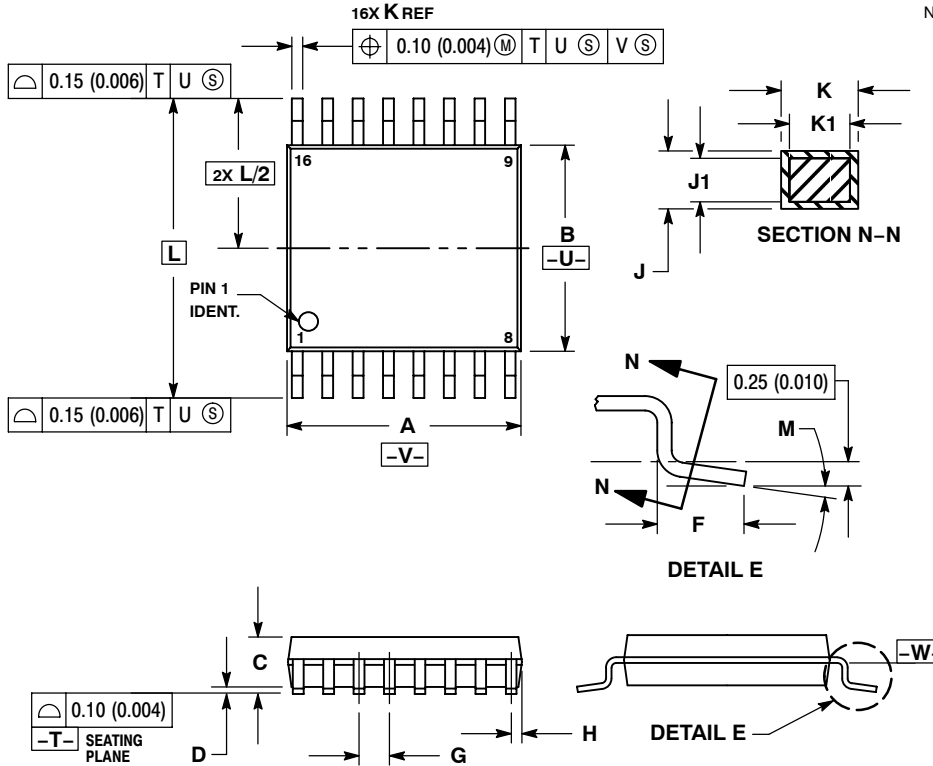
| Device | Package | Shipping† |
|---------------|-----------------------|--------------------|
| NB3N508SDTG | TSSOP-16 (Pb-Free) | 96 Units / Rail |
| NB3N508SDTR2G | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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