12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors

Data Sheet **AD7293**

FEATURES

- 4 closed-loop power amplifier (PA) drain current controllers
- Built-in PA protection, sequencing, and alert features
- Compatible with both depletion mode and enhancement mode power amplifiers
- Highly integrated
  - 4 uncommitted 12-bit analog-to-digital converter (ADC) inputs
    - ±0.5 LSB typical integral nonlinearity (INL)
  - Eight 12-bit voltage digital-to-analog converters (DACs)
    - 1.3 µs maximum settling
  - 4 high-side current sense amplifiers, ±0.1% gain error
  - 2 external temperature sensor inputs, ±1.1°C accuracy
  - Internal temperature sensor, ±1.25°C accuracy
  - 2.5 V on-chip reference
- Flexible monitoring and control ranges
  - ADC input ranges: 0 V to 1.25 V, 0 V to 2.5 V, and 0 V to 5 V
  - Bipolar DAC ranges: 0 V to +5 V, −4 V to +1 V, and −5 V to 0 V
  - Bipolar DAC reset and clamping relative to V_{CLAMPx} voltage
  - Unipolar DAC ranges: 0 V to 5 V, 2.5 V to 7.5 V, and 5 V to 10 V
  - Current sense gain: 6.25, 12.5, 25, 50, 100, and more
  - Adjustable closed-loop setpoint ramp time
- High-side voltage current sensing
  - 4 current sense inputs
    - 4 V to AV_{SS} + 60 V, ±200 mV input range
- Small package and flexible interface
  - Serial port interface (SPI) with V_{DRIVE} supporting 1.8 V, 3 V, and 5 V interfaces
  - 56-lead LFCSP
- Temperature range: −40°C to +125°C

APPLICATIONS

- GaN and GaAs power amplifier monitoring and controls
- Base station power amplifiers
- General-purpose system monitoring and controls

GENERAL DESCRIPTION

The AD7293 is a PA drain current controller containing functionality for general-purpose monitoring and control of current, voltage, and temperature, integrated into a single chip solution with an SPI-compatible interface.

The device features a 4-channel, 12-bit successive approximation register (SAR) ADC, eight 12-bit DACs (four bipolar and four unipolar with output ranges that can be configured to shut down under external pin control), a ±1.25°C accurate internal temperature sensor, and eight general-purpose input/output (GPIO) pins.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

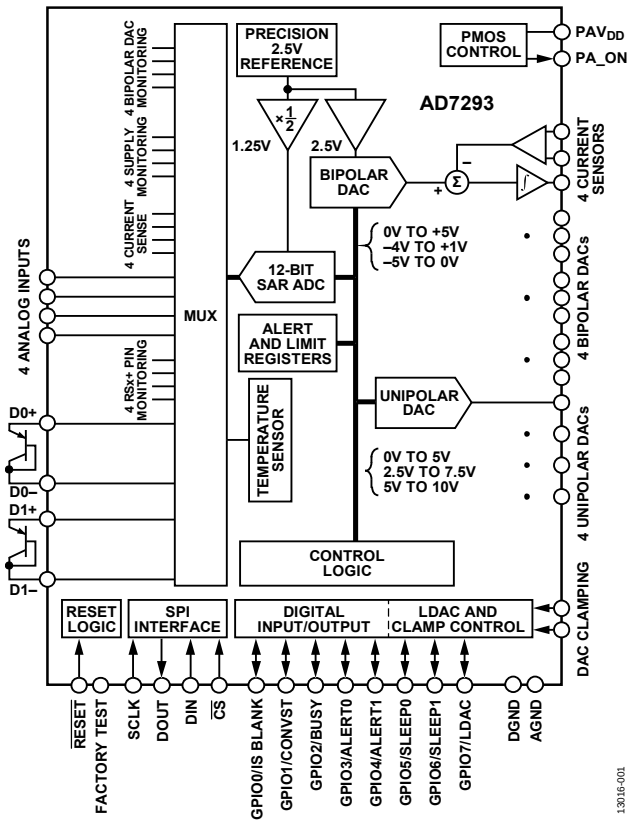

Figure 1.

The device also includes limit registers for alert functions and four high-side current sense amplifiers to measure current across external shunt resistors. These amplifiers can be optionally set to operate as part of four independent closed-loop drain current controllers.

A high accuracy 2.5 V internal reference is provided to drive the DACs and the ADC. The 12-bit ADC monitors and digitizes the internal temperature sensor, and two inputs are included for the external diode temperature sensors.

Note that throughout this data sheet, multifunction pins, such as GPIO4/ALERT1, are referred to either by the entire pin name or by a single function of the pin, for example, ALERT1, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Four independent closed-loop drain current controllers.
2. Built-in monitoring, sequencing, and alert features.
3. Compatible with both depletion mode and enhancement mode power amplifiers.

Rev. A Document Feedback

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AD7293* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7293 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1361: AD7293 Closed-Loop for Power Amplifier Drain Current Control

Data Sheet

- AD7293: 12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors Data Sheet

User Guides

- UG-817: Evaluating the AD7293 12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors

DESIGN RESOURCES

- AD7293 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7293 EngineerZone Discussions.

SAMPLE AND BUY

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REVISION HISTORY

6/2016—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

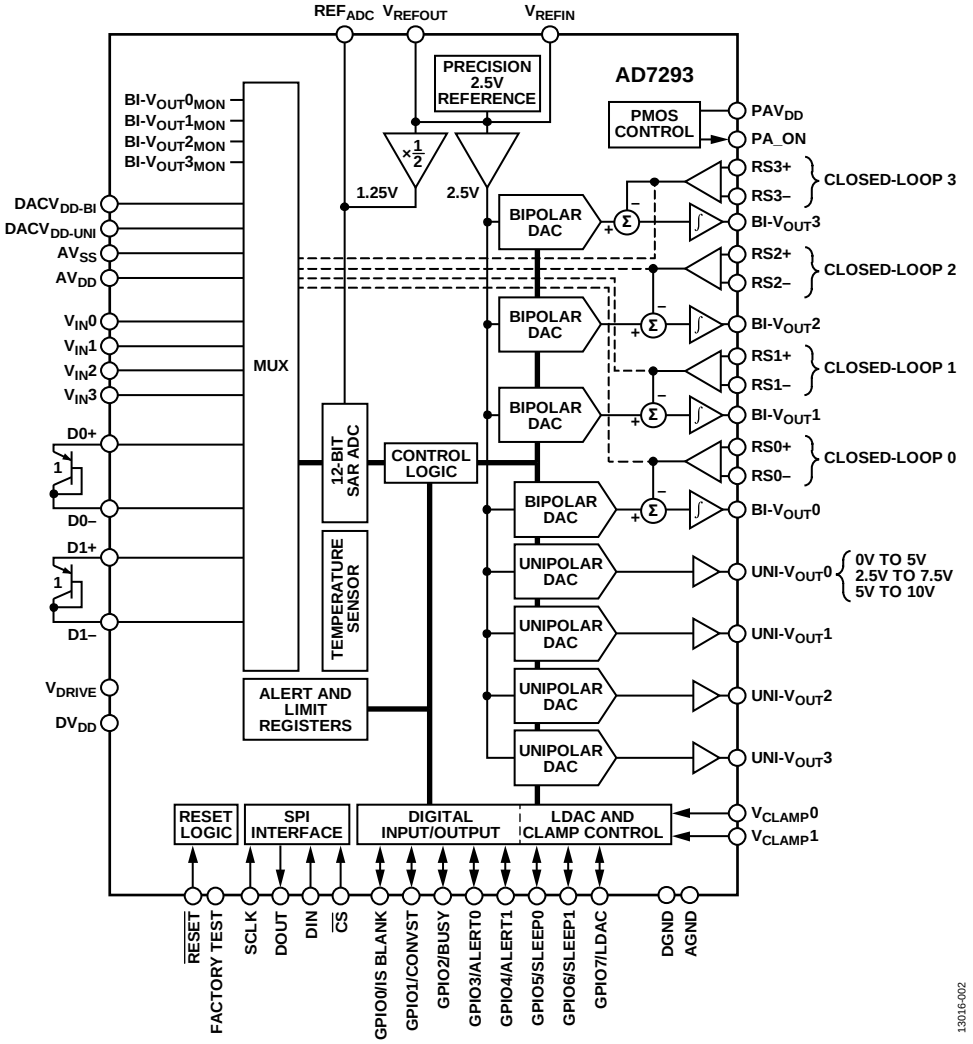


Figure 2. Closed-Loop Functional Block Diagram

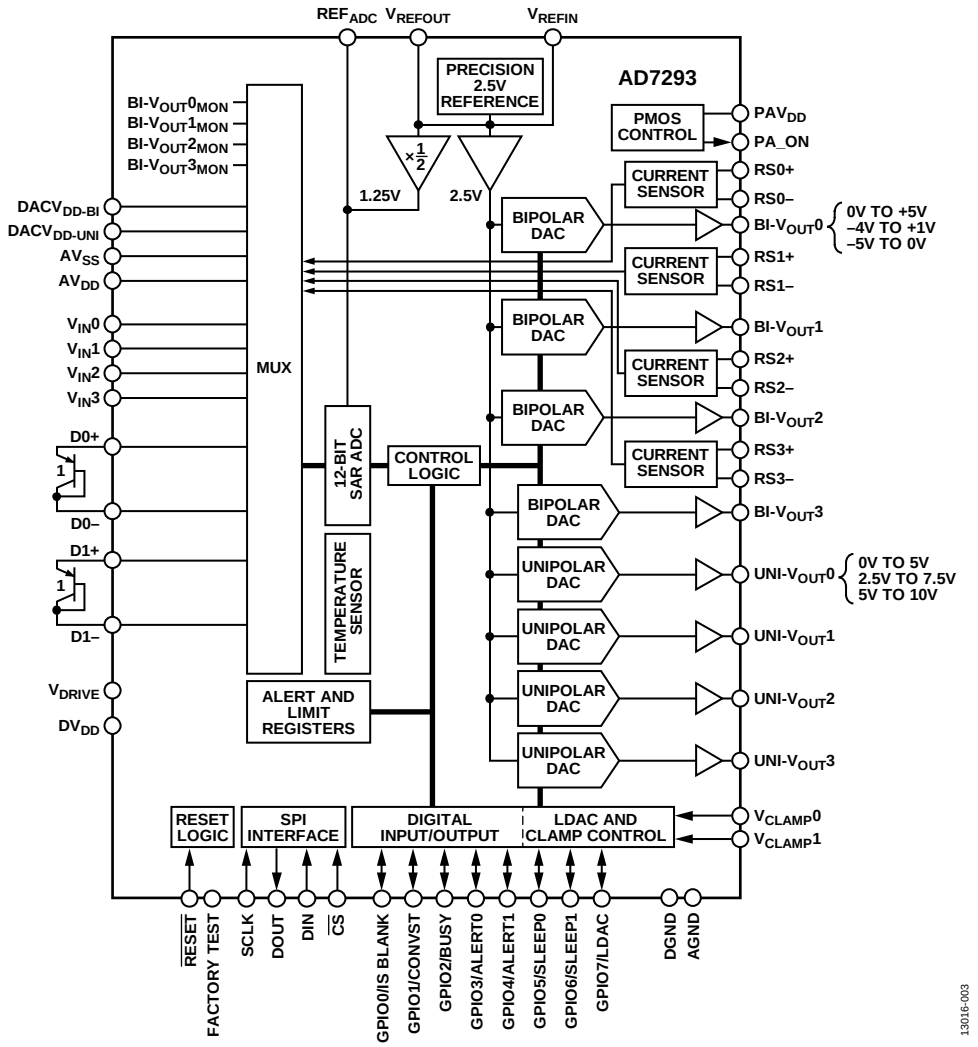


Figure 3. Open-Loop Functional Block Diagram

SPECIFICATIONS

ADC

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution		12		Bits	
Integral Nonlinearity (INL)		±0.5	±1	LSB	
Differential Nonlinearity (DNL)		±0.5	±0.99	LSB	No missing codes
Single-Ended Mode					
Zero Code Error		±0.4	±2.5	LSB	
Zero Code Error Mismatch		±0.6		LSB	
Full-Scale Error			±6.5	LSB	
Full-Scale Error Mismatch		±1.5		LSB	
Differential Mode					
Gain Error		±3	±6.5	LSB	
Gain Error Mismatch		±1.5		LSB	
Zero Code Error		±0.5	±2	LSB	
Zero Code Error Mismatch		±0.6		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 1 kHz sine wave; single-ended mode; 0 V to 4 × REF_{ADC}
Signal-to-Noise Ratio (SNR)[1, 2]		72		dB	
Signal-to-Noise + Distortion (SINAD) Ratio[1, 2]		72		dB	
Total Harmonic Distortion (THD)[1, 2]		−90.5		dB	
Channel to Channel Isolation[2]		95		dB	f_{IN} = 100 Hz to 80 kHz
Full Power Bandwidth[2]		7		MHz	At 0.1 dB; single-ended mode; 0 V to 4 × REF_{ADC}
CONVERSION RATE					
Conversion Time[2]		500		ns	
Track-and-Hold Acquisition Time[2]		100		ns	Voltage inputs in command mode
ANALOG INPUT[1]					REF_{ADC} = 1.25 V
Single-Ended Input Range	0		1.25	V	0 V to REF_{ADC} mode
	0		2.5	V	0 V to 2 × REF_{ADC} mode
	0		5	V	0 V to 4 × REF_{ADC} mode
Pseudo Differential Range ($V_{IN+} - V_{IN-}$[3])	0		1.25	V	0 V to REF_{ADC} mode
	0		2.5	V	0 V to 2 × REF_{ADC} mode
	0		5	V	0 V to 4 × REF_{ADC} mode
Differential Range ($V_{IN+} - V_{IN-}$)[4]	−1.25		+1.25	V	0 V to REF_{ADC} mode
	−2.5		+2.5	V	0 V to 2 × REF_{ADC} mode
	−5		+5	V	0 V to 4 × REF_{ADC} mode
Input Capacitance[2]		30		pF	
DC Input Leakage Current			±1	μA	
INTERNAL BI-V_{OUT}x MONITORING INPUTS					
Full-Scale Input Range	−5		+5	V	
Resolution		12		Bits	LSB step size ≈ 2.5 mV
Gain Error		±0.53		%	
Offset Error		±14		mV	
INTERNAL RSx+ MONITORING INPUTS					
Full-Scale Input Range	0		62.5	V	
Resolution		12		Bits	LSB step size ≈ 15.2 mV
Gain Error		0.06		%	
Offset Error		±11		mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL SUPPLY MONITORING INPUTS					.
AV_{DD}					
Gain Error		±0.33		%	
Offset Error		±52		mV	
AV_{SS}					
Gain Error		±0.53		%	
Offset Error		±14		mV	
$DACV_{DD-UNI}$					
Gain Error		±0.16		%	
Offset Error		±12		mV	
$DACV_{DD-BI}$					
Gain Error		±0.33		%	
Offset Error		±52		mV	
INTERNAL REFERENCE[2]					
Reference Output Voltage	2.495	2.5	2.505	V	At T_A = 25°C only
Reference Temperature Coefficient		±10	±30	ppm/°C	
EXTERNAL REFERENCE					
Reference Input Voltage Range	2.48	2.5	2.52	V	
DC Input Leakage Current			±2	µA	

[1] See the Analog-to-Digital Converter (ADC) Overview section for more details.
[2] Guaranteed by design and characterization; not production tested.
[3] V_{IN-} = 0 V for specified performance.
[4] V_{IN+} and V_{IN-} must remain within GND and AV_{DD}.

DAC

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1]					
Resolution	12			Bits	
Integral Nonlinearity (INL)		±1	±1.7	LSB	Bipolar
			±3		Unipolar
		±1		LSB	Load current ±10 mA within 300 mV of supply
Differential Nonlinearity (DNL)	−0.99	±0.3	+1	LSB	Guaranteed monotonic
Full-Scale (FS) Error		±2.5		mV	All 1s loaded to DAC register, no load applied
		±0.65		% of FS	10 mA load applied
Offset Error		±10		mV	Unipolar, 2.5 V to 7.5 V range, 5 V to 10 V range
			±10	mV	Unipolar, 0 V to 5 V range
		±2.5	±12	mV	Bipolar
Offset Error Temperature Coefficient		±8		µV/°C	Measured in the linear region, T_A = 25°C
Gain Error			±0.15	% FSR	Bipolar
			±0.4	% FSR	Unipolar
Gain Error Temperature Coefficient		±3		ppm/°C	
DAC OUTPUT CHARACTERISTICS					
Bipolar Open-Loop DAC Range	0		5	V	BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3
	−4		+1	V	
	−5		0	V	
Unipolar DAC Range	0		5	V	UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3
	2.5		7.5	V	
	5		10	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Unipolar DAC Short-Circuit Current		40		mA	Shorted to AGND or $DACV_{DD-UNI}$
Bipolar DAC Short-Circuit Current		42		mA	Shorted to AV_{SS} or $DACV_{DD-BI}$
Load Current[2]	−10		+10	mA	Source and/or sink within 300 mV of supply
Capacitive Load Stability		10		nF	$R_L = \infty$
DC Output Impedance		1		Ω	Midscale
AC CHARACTERISTICS					
Output Voltage Settling Time[2]		1.2	1.3	µs	¼ to ¾ change within ±1 LSB, measured from the last SCLK rising edge, C_L = 200 pF
Slew Rate[2]		7.5		V/µs	
Digital Feedthrough[2]		0.1		nV-sec	
DAC to DAC Crosstalk[2, 3]		0.2		nV-sec	
Output Noise Spectral Density[2, 3]		55		nV/√Hz	f_{IN} = 10 kHz, bipolar
		110		nV/√Hz	f_{IN} = 10 kHz, unipolar
Output Noise[2, 3]		102		µV p-p	Bipolar
		135		µV p-p	Unipolar
CLAMP INPUTS					Controlled by SLEEP0 and SLEEP1 digital pins
Clamp Output Voltage[2]		−3 × $V_{CLAMP}0$, $V_{CLAMP}1$		V	BI-$V_{OUT}x = -3 \times V_{CLAMP}0, V_{CLAMP}1$
Gain Error		0.2		%	Within 200 mV of AV_{SS}
Input Referred Offset Error		5		mV	
$V_{CLAMP}0$ and $V_{CLAMP}1$ Input Current		±1		µA	
Clamp Voltage Range	AV_{SS}		0	V	
Output Current[2]	−10		+10	mA	Source and/or sink within 300 mV of supply
Clamp to Open-Loop Settling Time[2]			5	µs	$R_L = \infty$, C_L = 200 pF, output voltage within 10%, 5 V transition

[1] Specification tested with output unloaded. Linearity calculated using best fit line method and based on a reduced code range equivalent to 100 mV within either side of supply or ground ± 82 codes.
[2] Guaranteed by design and characterization; not production tested.
[3] All unipolar DACs must be enabled with an output code set to a minimum code of 41 LSBs.

TEMPERATURE SENSOR

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL TEMPERATURE SENSOR[1]					
Operating Range[2]	−40		+125	°C	See Figure 30 for −55°C to +125°C operation
Accuracy		±1.25	±3	°C	Internal temperature sensor, T_A = −40°C to +125°C
		±1.25		°C	T_A = 25°C
Resolution		0.125		°C	
EXTERNAL TEMPERATURE SENSOR[1]					External transistor = 2N3906; no capacitor between Dx−/Dx+ pins, and no series resistor between transistor and Dx−/Dx+ pins
Operating Range	−55		+150	°C	Limited by external transistor
Accuracy		±1.1	±3	°C	T_A = −40°C to +105°C
Resolution		0.125		°C	LSB size

[1] Guaranteed by design and characterization; not production tested.
[2] Guaranteed functional to −55°C by design but accuracy is not guaranteed.

CURRENT SENSOR

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, gain = 6.25, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT SENSE					RSx+ = AV_{DD} to AV_{SS} + 60 V
Common-Mode Input Voltage Range	4		60	V	AV_{SS} = 0 V
	4		55	V	AV_{SS} = −5 V
Differential Input Voltage Range	−200		+200	mV	Gain = 6.25, for gain settings, see Table 44
Gain Error		±0.1	±0.7	%	
Gain Error Temperature Coefficient		−16		ppm/°C	
Offset Error (Referred to Input, RTI)			±200	µV	
Offset Error Drift		1		µV/°C	
DC Common-Mode Rejection	100	140		dB	
RSx+[1] Pin Input Current		105		µA	
RSx−[1] Pin Input Current		10		nA	
Differential Input Resistance[2]		700		kΩ	

[1] Where x is 0, 1, 2, or 3.
[2] Guaranteed by design and characterization; not production tested.

CLOSED-LOOP SPECIFICATIONS

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 5 V, AV_{SS} = −5 V, PAV_{DD} = 5 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external; V_{DRIVE} = 1.7 V to 5.5 V; T_A = −40°C to +125°C, unless otherwise noted. Power amplifier transconductance = 1 S to 5 S, and external gate filter time constant (τ_G) = 5 µs to 50 µs.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NORMAL OPERATION[1, 2]					
Setpoint Resolution		12		Bits	Equivalent to 200 mV/4096 = 49 µV at the current sense input
Sense Resistor Voltage Range	0		200	mV	
Setpoint Gain Error		±0.5		%	
Setpoint Offset Error (RTI)		±100		µV	Referred to current sense input; see Figure 31
Integrator Time Constant[3]		840		µs	Programmable; see Table 50
Closed-Loop Update Rate[3]		59.6		kHz	
Capacitive Load Stability		1		µF	5 Ω series resistance
Closed-Loop to Clamp Settling Time		1		µs	Within ±10%
Bipolar Closed-Loop Output Range	AV_{SS}		AV_{DD}	V	See the Bipolar DAC (BI-VOUTx) Offset Registers (Register 0x34 to Register 0x37) section
Integrator Programmable Voltage Limit Resolution		2.5		mV	See the Closed-Loop Integrator Programmable Voltage Limit section
START SEQUENCING PA_ON CONTROL[2]					
PA_ON Pin Output Voltage	AGND		PAV_{DD}	V	
PA_ON Off State Enable			500	µs	Measured from AV_{SS} failure event, C_L = 1 nF
			500	µs	Measured from SLEEP0 or SLEEP1 pin, 0 to 1 transition, C_L = 1 nF
PA_ON On State Enable			500	µs	Measured from SLEEP1 to SLEEP0 transition, C_L = 1 nF
PA_ON Short-Circuit Current		±10		mA	
PA_ON Resistance		250		Ω	
AV_{DD}/AV_{SS} ALARM					
AV_{DD} Alarm Threshold	3.2	3.6	3.9	V	
AV_{SS} Alarm Threshold	−3.8	−4.1	−4.4	V	

[1] Power amplifier characteristic dependent.
[2] Guaranteed by design and characterization; not production tested.
[3] Expressed as a function of the internal oscillator frequency.

GENERAL

DV_{DD}, AV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-BI}$ = 5 V, AV_{SS} = −5 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input Voltage						
High	V_{IH}	$0.8 \times V_{DRIVE}$			V	
Low	V_{IL}			$0.2 \times V_{DRIVE}$	V	
Input Leakage Current	I_{IN}		±1		µA	
Input Capacitance	C_{IN}		3		pF	
LOGIC OUTPUTS[1]						GPIO0/IS BLANK, GPIO1/CONVST, GPIO2/BUSY, GPIO3/ALERT0, and GPIO4/ALERT1 are open-drain outputs
Output Voltage						
High	V_{OH}			0.4	V	I_{SINK} = 3 mA
Low	V_{OL}			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current				±1	µA	
Floating-State Output Capacitance			8		pF	
GENERAL-PURPOSE OUPUTS						
Output Voltage						
High	V_{OH}			V_{DRIVE} − 0.2	V	I_{SINK}/I_{SOURCE} = 1 mA
Low	V_{OL}			0.4	V	I_{SINK}/I_{SOURCE} = 1 mA
POWER REQUIREMENTS						
Supply Voltages						
Positive Analog	AV_{DD}	4.5		5.5	V	
Negative Analog	AV_{SS}	−5.5		−4.5 or 0	V	
Logic Power	V_{DRIVE}	1.7		5.5	V	Supports 1.8 V, 3 V, and 5 V interfaces
Unipolar DAC	$DACV_{DD-UNI}$	4.5		12.5	V	
Bipolar DAC	$DACV_{DD-BI}$	4.5		5.5	V	
PA_ON Power	PAV_{DD}	4.5		AV_{SS} + 60	V	
RSx+ Voltage	V_{RSx+}	4		AV_{SS} + 60	V	
Supply Currents						All power supplies set to maximum voltage; ADC on and converting; DACs enabled with no load applied
AV_{DD}	AI_{DD}		9	12.5	mA	
AV_{SS}	AI_{SS}		−4.4	−5.4	mA	
V_{DRIVE}	I_{DRIVE}		1	2.1	mA	
$DACV_{DD-UNI}$	$DACI_{DD-UNI}$		2.1	3	mA	
$DACV_{DD-BI}$	$DACI_{DD-BI}$		5	8.2	mA	
PAV_{DD}	PAI_{DD}		81	100	µA	
Power Dissipation			110		mW	

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

SPI Serial Interface

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 2.7 V to 16 V, AV_{SS} = 0 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 7.

Parameter	Description	Limit at T_{MIN}/T_{MAX}		Unit
		V_{DRIVE} = 1.7 V to 2.7 V	V_{DRIVE} = 2.7 V to 5.5 V	
f_{SCLK}	Frequency of serial read clock[1]	8	15	MHz max
t_1	SCLK period	150	66.67	ns min
t_2	SCLK low	40	26	ns min
t_3	SCLK high	40	26	ns min
t_4	$\overline{CS}$ falling edge to SCLK rising edge	5	5	ns min
t_5	DIN setup time to SCLK rising edge	10	10	ns min
t_6[2]	DIN hold time after SCLK rising edge	10	10	ns max
t_7	Last SCLK rising edge to $\overline{CS}$ rising edge	5	5	ns min
t_8	$\overline{CS}$ high	12	10	ns min
t_9[3]	$\overline{CS}$ rising edge to next SCLK rising edge	1	1	ns min
t_{10}	SCLK falling edge to $\overline{CS}$ falling edge	1	1	ns min
t_{11}	SCLK falling edge to output data valid delay time from high impedance[4]	60	30	ns max
t_{12}	SCLK falling edge to output data valid delay time[4]	60	30	ns max
t_{13}	Last SCLK falling edge to DOUT high impedance[4]	20	20	ns typ
t_{14}	$\overline{CS}$ rising edge to DOUT high impedance[4]	25	15	ns max

[1] DOUT loaded with 10 pF for DOUT timing specifications.
[2] Time required for the output to cross 0.2 × V_{DRIVE} and 0.8 × V_{DRIVE} when V_{DRIVE} < 2.7 V; time required for the output to cross 0.3 × V_{DRIVE} and 0.7 × V_{DRIVE} when 2.7 ≤ V_{DRIVE} ≤5.5 V.
[3] Guaranteed by design and characterization; not production tested.
[4] MISO speed set to maximum in the general register.

Asynchronous Inputs

AV_{DD}, DV_{DD}, $DACV_{DD-BI}$ = 4.5 V to 5.5 V (connect AV_{DD} and $DACV_{DD-BI}$ to the same potential), $DACV_{DD-UNI}$ = 2.7 V to 16 V, AV_{SS} = 0 V, RSx+ = AV_{DD} to 55 V, AGND = DGND = 0 V, V_{REFIN} = 2.5 V internal or external, V_{DRIVE} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 8.

Parameter	Description	Limit at T_{MIN}/T_{MAX}		Unit
		V_{DRIVE} = 1.7 V to 2.7 V	V_{DRIVE} = 2.7 V to 5.5 V	
t_{15}[1]	Minimum LDAC pulse width	90	90	ns min
t_{16}	Minimum CONVST pulse width	90	90	ns min
t_{17}	Minimum IS BLANK pulse width	90	90	ns min
t_{18}	Minimum $\overline{RESET}$ pulse width	90	90	ns min

[1] Guaranteed by design and characterization; not production tested.

Timing Diagrams

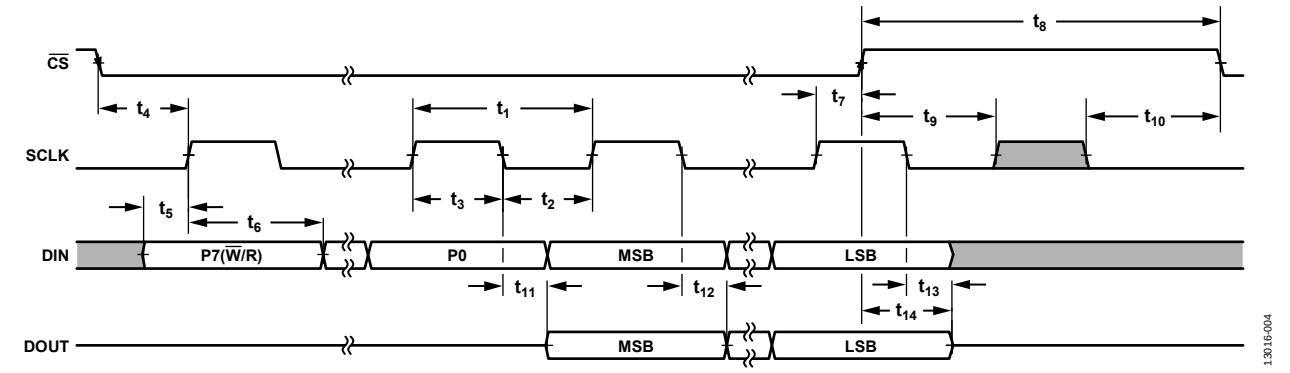


Figure 4. Serial Interface Timing Diagram

Figure 5. Asynchronous Inputs

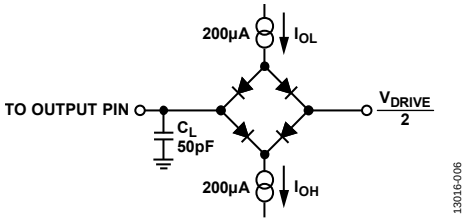


Figure 6. Load Circuit for Digital Output (DOUT) Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
±5 V Analog Output Pins (BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, BI-V_{OUT}3) to AV_{SS}	AV_{SS} − 0.3 V to $DACV_{DD-BI}$ + 0.3 V
12.5 V Analog Output Pins (UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, UNI-V_{OUT}3) to AGND	−0.3 V to $DACV_{DD-UNI}$ + 0.3 V
12.5 V Supply ($DACV_{DD-UNI}$) to AGND	−0.3 V to +15 V
2 V Analog Pins (REF_{ADC}, D1−, D1+, D0−, D0+) to AGND	−0.3 V to +2 V
5 V Analog Pins (FACTORY TEST, V_{REFIN}, V_{REFOUT}, V_{CLAMP}0, V_{CLAMP}1, V_{IN}x[1]) to AGND	−0.3 V to AV_{DD} + 0.3 V
5 V Digital Pins (GPIO5/SLEEP0, GPIO6/SLEEP1, $\overline{RESET}$, GPIO7/LDAC, $\overline{CS}$, DOUT) to DGND	−0.3 V to V_{DRIVE} + 0.3 V
5 V Open-Drain Pins (GPIO4/ALERT1, SCLK, DIN, DV_{DD}, GPIO3/ALERT0, GPIO2/BUSY, GPIO1/CONVST, GPIO0/IS BLANK) to DGND	−0.3 V to +7 V
5 V Supply Pins[2] (V_{DRIVE}, $DACV_{DD-BI}$, AV_{DD}) to AGND	−0.3 V to +7 V
−5 V Supply Pin (AV_{SS}) to AGND	−7 V to +0.3 V
60 V Analog Pins (RSx−) to RSx+	(RSx+) − 0.3 V to (RSx+) + 0.3 V
60 V Digital Pin (PA_ON) to AGND	−0.3 V to PAV_{DD} + 0.3 V
60 V Supply Pins (RSx+, PAV_{DD}) to AGND	−0.3 V to AV_{SS} + 65 V
Ground Pins (DGND, AGND) to AGND	−0.3 V to +0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Reflow Profile	J-STD 20 (JEDEC)
Maximum Junction Temperature	150°C
ESD Rating, All Pins	
Human Body Model (HBM)	2 kV
Field-Induced Charged Device Model (FICDM)	1 kV

[1] x = 0, 1, 2, or 3.
[2] Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a 4-layer JEDEC 2S2P type printed circuit board (PCB) with a thermal via, that is, a device soldered in a circuit board for surface-mount packages, per JESD51-7.

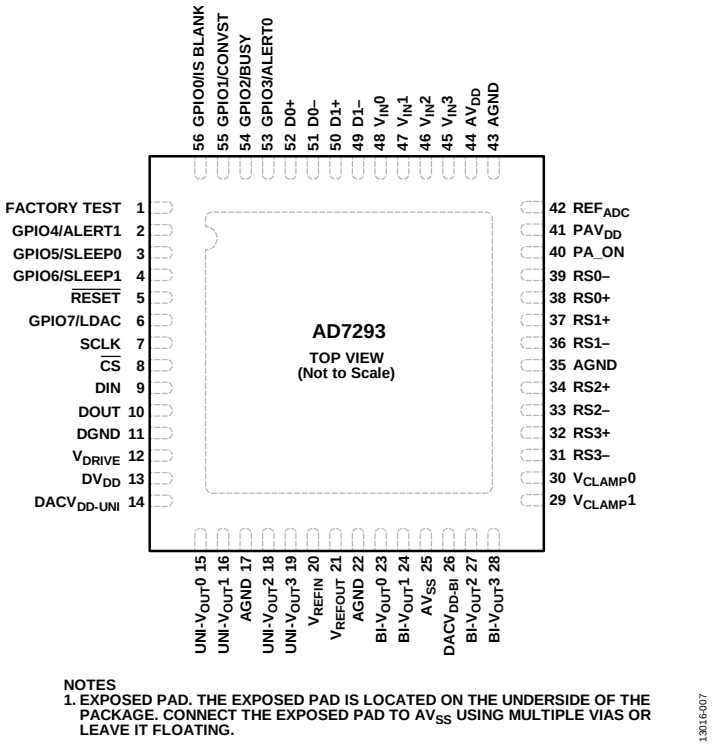
Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP	27	0.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE PACKAGE. CONNECT THE EXPOSED PAD TO AV_{SS} USING MULTIPLE VIAS OR LEAVE IT FLOATING.

Figure 7. Pin Configuration

Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	FACTORY TEST	Factory Test Pin. Leave this pin unconnected, or connect it to DGND.
2	GPIO4/ALERT1	General-Purpose Input/Output 4 Pin (GPIO4, Default as Input).
		Alert 1 Pin (ALERT1, Default). When configured as an alert, this pin acts as an out of range indicator. The polarity of the pin is register selectable. This pin is an open-drain output, and requires a pull-up resistor connected to V_{DRIVE}.
3	GPIO5/SLEEP0	General-Purpose Input/Output 5 Pin (GPIO5, Default as Input).
		Sleep 0 Pin (SLEEP0). DAC power-down digital input pin (polarity is register selectable). This pin can be configured to trigger DAC clamping on any combination of DAC channels.
4	GPIO6/SLEEP1	General-Purpose Input/Output 6 Pin (GPIO6).
		Sleep 1 Pin (SLEEP1, Default). DAC power-down digital input pin (polarity is register selectable). This pin can be configured to trigger DAC clamping on any combination of DAC channels.
5	$\overline{\text{RESET}}$	Reset Input. Taking this pin low performs a hardware reset.
6	GPIO7/LDAC	General-Purpose Input/Output 7 Pin (GPIO7).
		DAC Load Pin (LDAC, Default). When this input is active, the DAC registers are updated. The polarity of this pin is register selectable. See the Load DAC (LDAC Pin) section for more information.
7	SCLK	SPI Serial Clock Input.
8	$\overline{\text{CS}}$	Chip Select Signal. This active low, logic input signal frames the serial data input.
9	DIN	SPI Serial Data Input. The serial data loaded into the registers is provided on this pin. Data is clocked into the device on the rising edge of SCLK.
10	DOUT	SPI Serial Data Output. The serial data read from the registers is provided on this pin. Data is clocked out on the falling edge of SCLK. DOUT is high impedance when it is not outputting data.
11	DGND	Digital Ground. DGND is the ground reference point for all digital circuitry. Refer all digital signals to DGND. Connect both the DGND and AGND pins to the ground plane of the system.
12	V_{DRIVE}	Drive Voltage Reference Level of the SPI Bus from 1.7 V to 5.5 V.
13	DV_{DD}	Digital Supply Voltage from 4.5 V to 5.5 V.

Pin Number	Mnemonic	Description
14	$DACV_{DD-UNI}$	DAC Positive Supply Pin for the Unipolar DAC Output Amplifiers on UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3.
15, 16, 18, 19	UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, UNI-V_{OUT}3,	Unipolar DAC Outputs. The clamp and power-on reset voltage for these DACs is 0 V.
17, 22, 35, 43	AGND	Analog Ground. Connect both the AGND and DGND pins to the ground plane of the system.
20	V_{REFIN}	Reference Input to the Device. Connect this pin to an external reference voltage, or tie this pin to V_{REFOUT}.
21	V_{REFOUT}	2.5 V Reference Output. Connect to V_{REFIN} to operate in internal reference mode. An optional 10 nF capacitor is recommended between the reference output and AGND for noise filtering.
23, 24, 27, 28	BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, BI-V_{OUT}3	Bipolar DAC Outputs in Open-Loop Mode and Integrator Outputs in Closed-Loop Mode. The clamp and power-on reset voltage for these DACs is dictated by the V_{CLAMP}x pins.
25	AV_{SS}	DAC Negative Supply Pin for the BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3 DAC Output Amplifiers.
26	$DACV_{DD-BI}$	Analog Supply Pin for BI-V_{OUT}0, BI-V_{OUT}1, BI-V_{OUT}2, and BI-V_{OUT}3. Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.
29	V_{CLAMP}1	Power-On Reset and Clamp Voltage for BI-V_{OUT}2 and BI-V_{OUT}3.
30	V_{CLAMP}0	Power-On Reset and Clamp Voltage for BI-V_{OUT}0 and BI-V_{OUT}1.
31, 33, 36, 39	RS3−, RS2−, RS1−, RS0−	Negative Connection for External Shunt Resistors.
32, 34, 37, 38	RS3+, RS2+, RS1+, RS0+	Positive Connection for External Shunt Resistors.
40	PA_ON	Power Amplifier On. This pin drives an external, positive channel metal oxide semiconductor (PMOS) switch capable of turning on/off the drain current to a PA transistor. The maximum voltage is set by PAV_{DD} and limited to AV_{SS} + 60 V. The power amplifier is turned on when the output is low. The AV_{SS} and AV_{DD} supply alarms can be configured to automatically trigger PA_ON. An alert condition can be configured to trigger PA_ON. Additionally, PA_ON can be turned on/off by issuing a register write.
41	PAV_{DD}	Power Supply for the PA_ON Control Signal. This pin is limited to 4 V to AV_{SS} + 60 V.
42	REF_{ADC}	Internal ADC Reference Voltage. The output at this pin is half the reference value (V_{REFIN}), 1.25 V. Connect decoupling capacitors to this pin to decouple the reference buffer. For best performance, connect a 4.7 µF compensation capacitor between REF_{ADC} and AGND. For stability, the amplifier requires a minimum capacitance of 220 nF (X7R/C0G ceramic) connected between REF_{ADC} and AGND, located as close to the AD7293 as possible (no more than 1 Ω of interconnect resistance).
44	AV_{DD}	Supply Voltage for All of the Analog Circuitry on the AD7293. The operating range is 4.5 V to 5.5 V. Connect AV_{DD} and $DACV_{DD-BI}$ to the same potential.
45 to 48	V_{IN}3, V_{IN}2, V_{IN}1, V_{IN}0	ADC Analog Inputs. Unused inputs must not be left floating. The input range of these pins is register selectable: 0 V to 1.25 V, 0 V to 2.5 V, or 0 V to 5 V.
49, 50, 51, 52	D1−, D1+, D0−, D0+	Temperature Sensor Analog Inputs. Connect these pins to the external temperature sensing transistor. Tie these pins to AGND if unused.
53	GPIO3/ALERT0	General-Purpose Input/Output 3 Pin (GPIO3, Default as Input). Alert 0 Pin (ALERT0). When ALERT0 is configured as an alert, this pin acts as an out of range indicator. Open-drain output whether in GPIO mode or alert mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required.
54	GPIO2/BUSY	General-Purpose Input/Output 2 Pin (GPIO2, Default as Input). Busy Pin (BUSY). When BUSY is configured as a busy output, this pin becomes active when a conversion is in progress. Open-drain output whether in GPIO mode or busy mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required.
55	GPIO1/CONVST	General-Purpose Input/Output 1 Pin (GPIO1, Default as Input). This pin is an open-drain output in GPIO mode. The polarity of this pin is register selectable. ADC External Convert Start Input Pin (CONVST). CONVST triggers conversions via this pin. The CONVST pin is useful for synchronizing the ADC sampling instant with an external source. A pull-up resistor connected to V_{DRIVE} is required in GPIO mode or if unused.
56	GPIO0/IS BLANK	General-Purpose Input/Output 0 Pin (GPIO0, Default as Input). This pin is an open-drain output in GPIO mode. The polarity of this pin is register selectable. A pull-up resistor connected to V_{DRIVE} is required in GPIO mode or if unused. Current Sensor Conversion Blank Pin (IS BLANK). This pin can blank current sensor conversions and the polarity of this pin is register selectable.
	EPAD	Exposed Pad. The exposed pad is located on the underside of the package. Connect the exposed pad to AV_{SS} using multiple vias or leave it floating.

TYPICAL PERFORMANCE CHARACTERISTICS

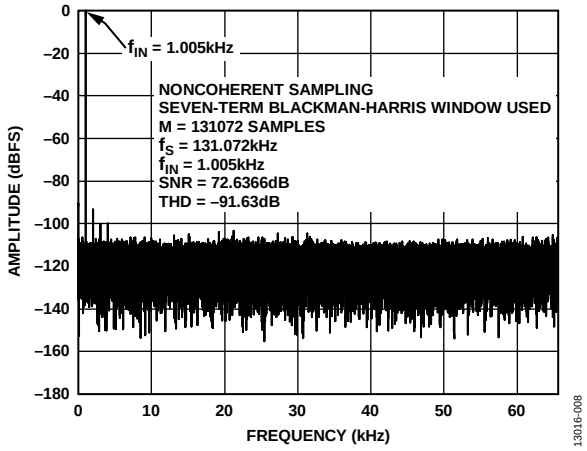


Figure 8. Signal-to-Noise Ratio, Single-Ended Input, 2 × REF_{ADC} Range

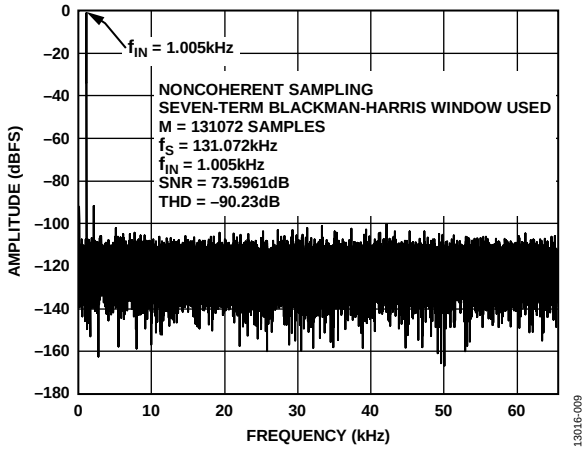


Figure 9. Signal-to-Noise Ratio, Differential Input, REF_{ADC} Range

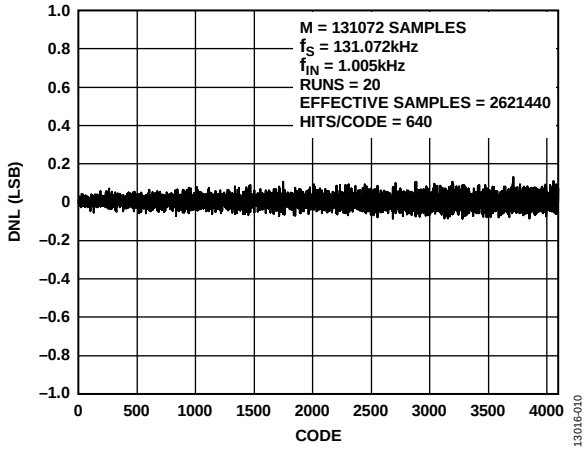


Figure 10. ADC DNL Single-Ended, REF_{ADC} Range

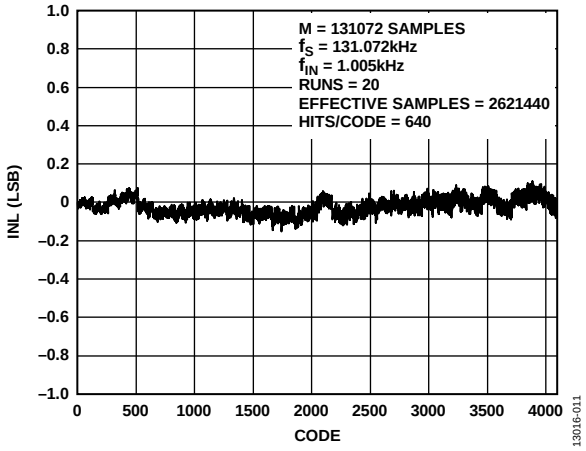


Figure 11. ADC INL Single-Ended, REF_{ADC} Range

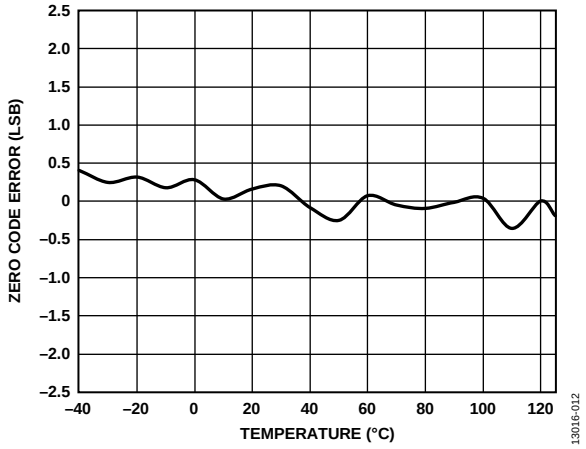


Figure 12. ADC Zero Code Error vs. Temperature

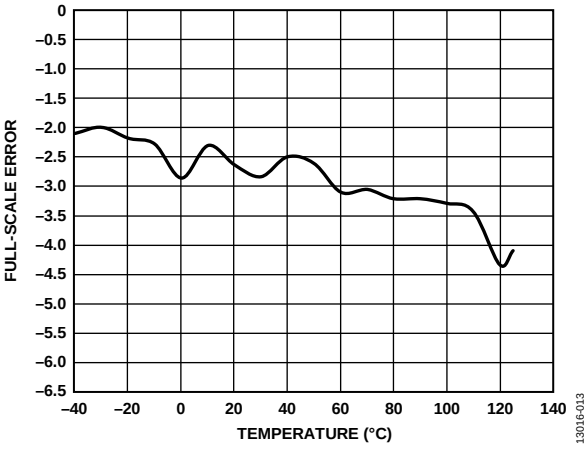


Figure 13. ADC Full-Scale Error vs. Temperature

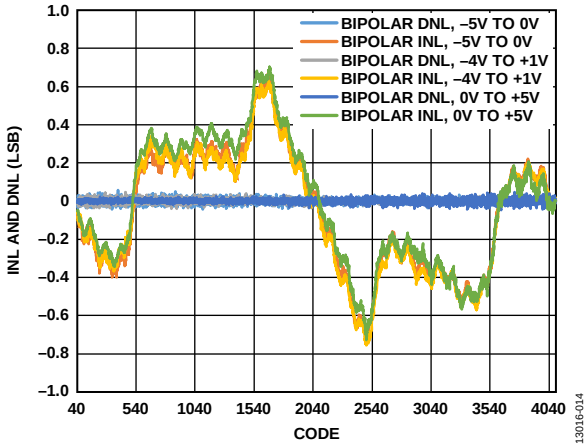


Figure 14. Bipolar DAC INL and DNL

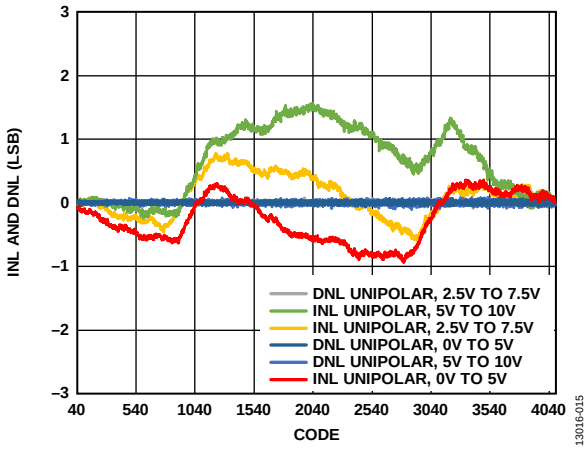


Figure 15. Unipolar DAC INL and DNL

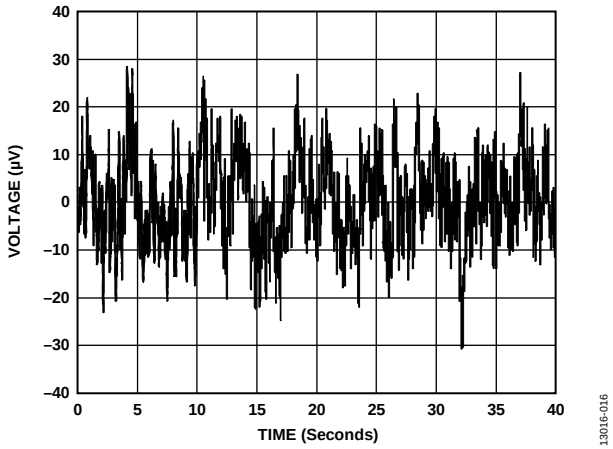


Figure 16. 0.1 Hz to 10 Hz DAC Output Noise, Input Code 0x000

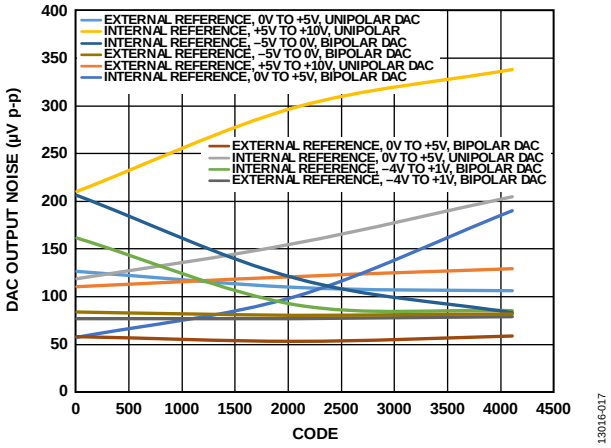


Figure 17. 0.1 Hz to 10 Hz DAC Output Noise vs. Code

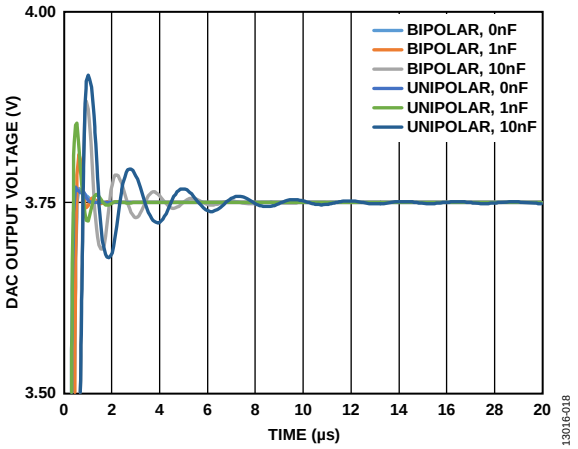


Figure 18. Zoomed In Settling Time for a ¼ to ¾ Output Voltage Step

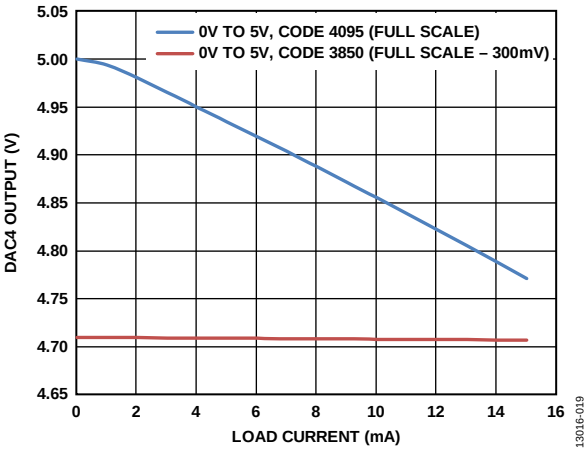


Figure 19. DAC4 Output (Full Scale) vs. Load Current

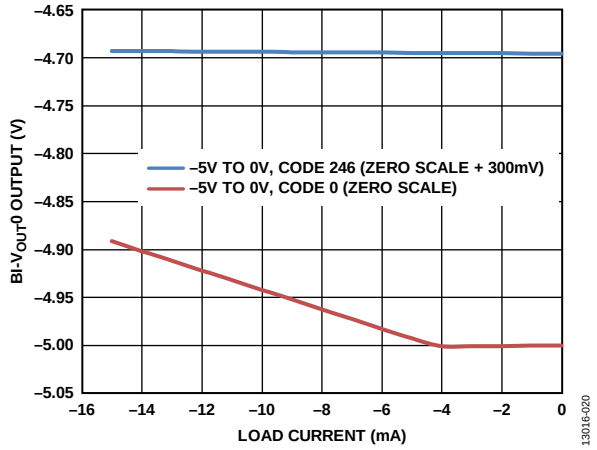


Figure 20. BI-V_{OUT}0 Output Voltage (Zero Scale) vs. Load Current

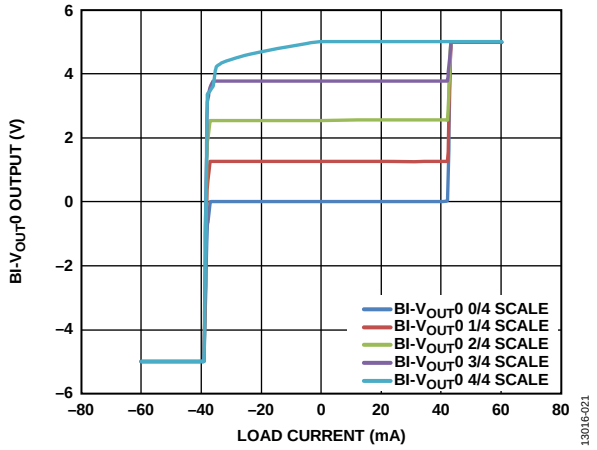


Figure 21. BI-V_{OUT}0 Output Voltage vs. Load Current

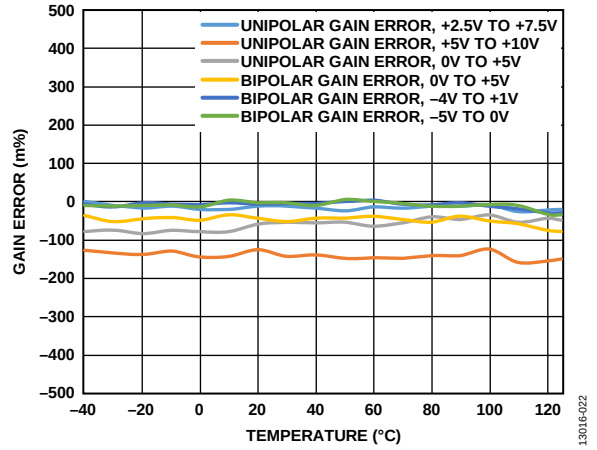


Figure 22. DAC Gain Error vs. Temperature

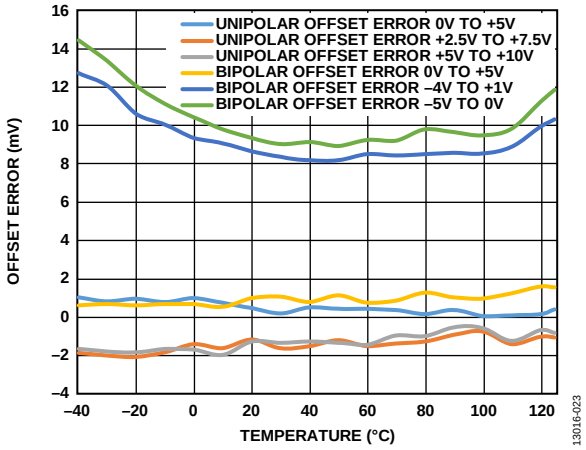


Figure 23. DAC Offset Error vs. Temperature

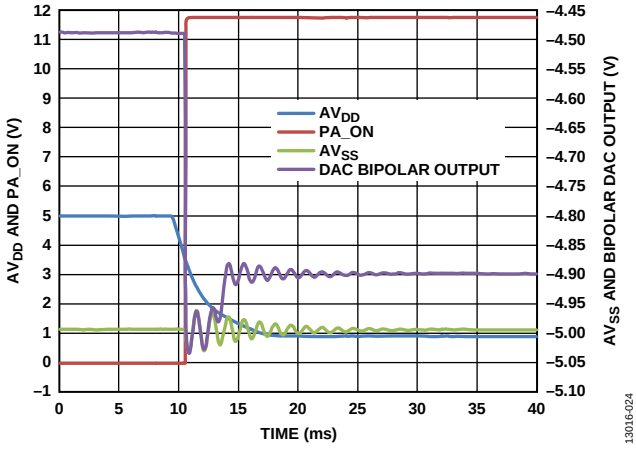


Figure 24. Bipolar DAC Response to AV_{DD} Failure

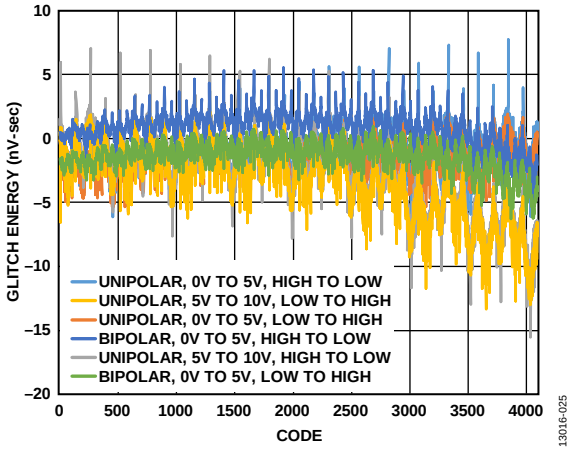


Figure 25. DAC Glitch Energy vs. Code

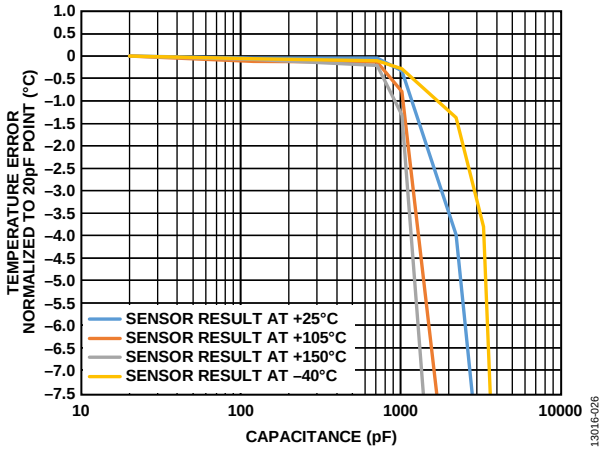


Figure 26. Temperature Error vs. Capacitance from Dx+ to Dx–

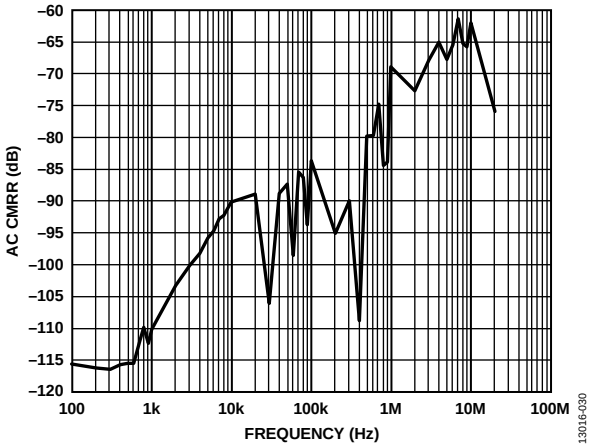


Figure 29. High-Side Current Sensor at Common-Mode Rejection Ratio (CMRR)

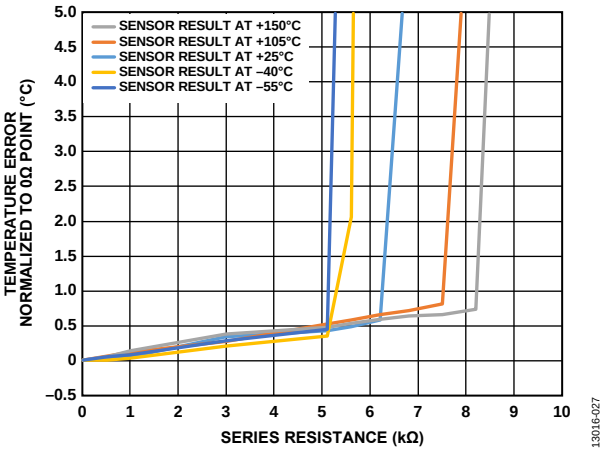


Figure 27. Temperature Error vs. Series Resistance for Typical Devices

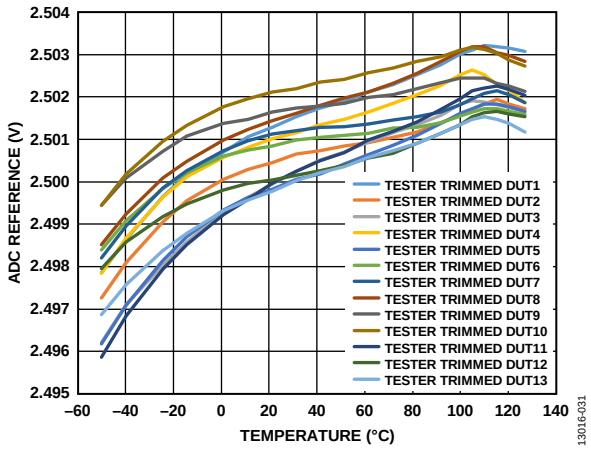


Figure 30. ADC Reference vs. Temperature

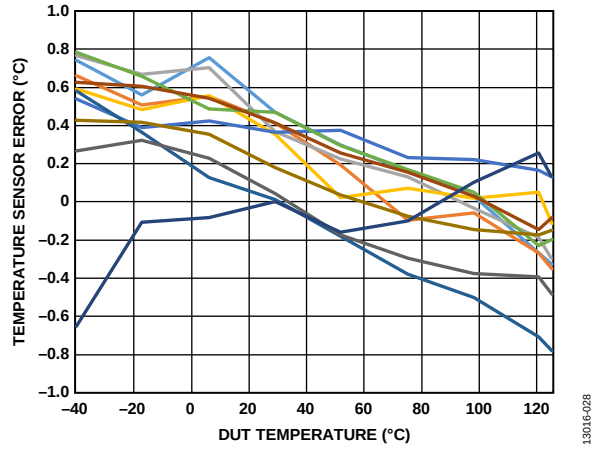


Figure 28. Temperature Sensor Error vs. Device Under Test (DUT) Temperature

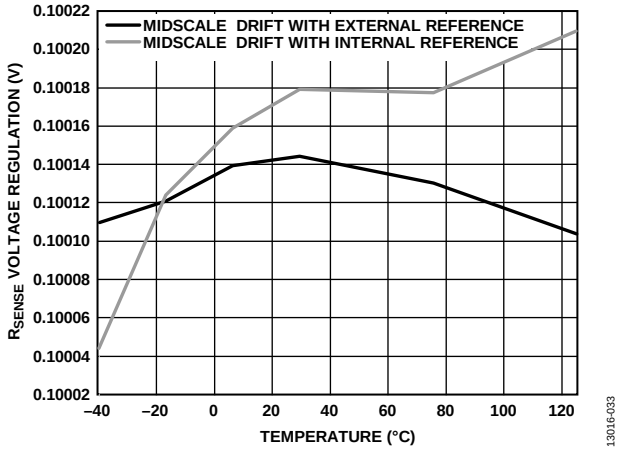


Figure 31. Closed-Loop R_{SENSE} Voltage Regulation vs. Temperature

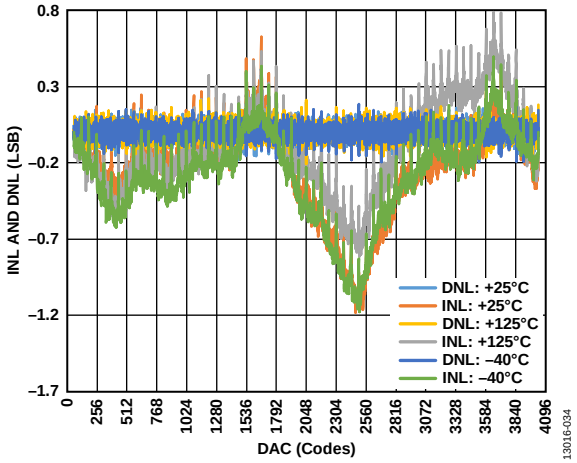


Figure 32. Closed-Loop INL and DNL

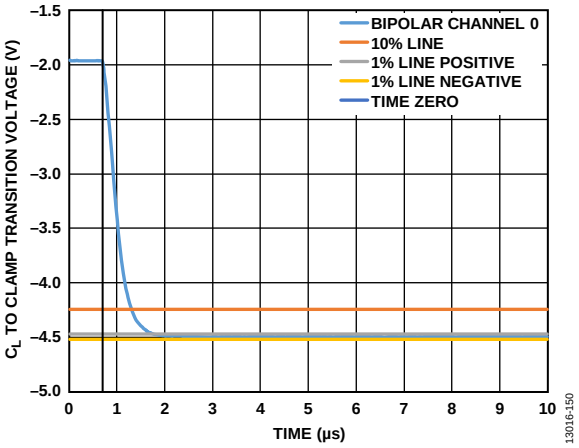


Figure 34. Closed Loop to Clamp Settling Time

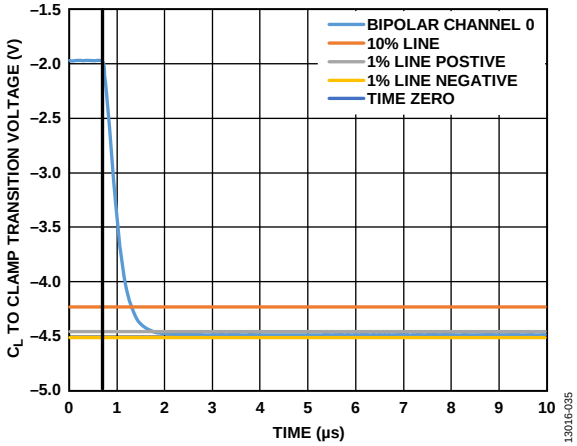


Figure 33. Open Loop to Clamp Settling Time

THEORY OF OPERATION

ANALOG-TO-DIGITAL CONVERTER (ADC) OVERVIEW

The AD7293 provides the user with a multichannel multiplexer, an on-chip track-and-hold, and a successive approximation ADC based around a capacitive DAC. The analog input range for the ADC is selectable as a 0 V to REF_{ADC}, 0 V to 2 × REF_{ADC}, or 0 V to 4 × REF_{ADC} input single-ended input, where REF_{ADC} = 1.25 V.

The various monitored and uncommitted input signals are multiplexed into the ADC. The AD7293 has four uncommitted analog input channels, $V_{IN}0$ to $V_{IN}3$.

ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer least significant bit (LSB) values (1 LSB, 2 × LSB, and so on). The reference voltage for the ADC is referred from the main 2.5 V reference through an amplifier that attenuates the voltage by one half. REF_{ADC} = 1.25 V.

In single-ended mode, the LSB size is $REF_{ADC}/4096$ when the 0 V to REF_{ADC} range is selected, 2 × $REF_{ADC}/4096$ when the 0 V to 2 × REF_{ADC} range is selected, and 4 × $REF_{ADC}/4096$ when the 0 V to 4 × REF_{ADC} range is selected (which is the default value). Figure 35 shows the ideal transfer characteristic for the ADC when outputting straight binary coding.

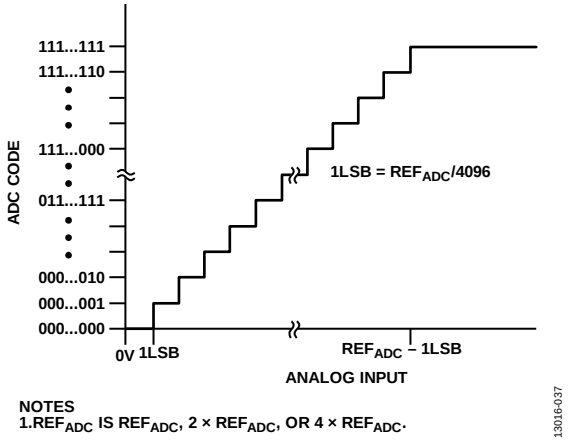


Figure 35. Single-Ended Transfer Characteristics

In differential mode, the LSB size is 2 × $REF_{ADC}/4096$ when the 0 V to REF_{ADC} range is selected, 4 × $REF_{ADC}/4096$ when the 0 V to 2 × REF_{ADC} range is selected, and 8 × $REF_{ADC}/4096$ when the 0 V to 4 × REF_{ADC} range is selected. Figure 36 shows the ideal transfer characteristic for the ADC when outputting differential coding (with the 2 × REF_{ADC} range).

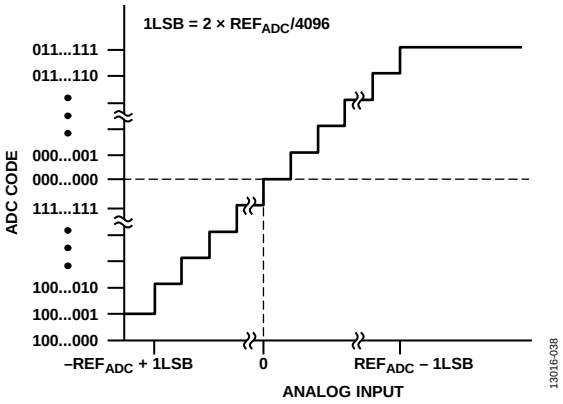


Figure 36. Differential Transfer Characteristics

Table 12. Code Transition and Voltage

Code Transition	Single-Ended Voltage (V_{IN})	Differential Voltage ($V_{IN}+ - V_{IN}-$)
0x000 to 0x001	REF_{ADC} × Range/4096	$-REF_{ADC}$ × Range × 2047/2048
0x7FF to 0x800	REF_{ADC} × Range/2	0 V
0xFFE to 0xFFF	REF_{ADC} × Range × 4095/4096	$+REF_{ADC}$ × Range × 2047/2048

For $V_{IN}0$ to $V_{IN}3$ in single-ended mode, the output code is straight binary, and the ideal input voltage is given by

$$V_{IN} = ((Code + 0.5)/ 4096) \times REF_{ADC} \times Range$$

The differential code is shown in Table 12, and the associated voltage is calculated by

$$V_{IN+} - V_{IN-} = ((Code - 2047.5)/2048) \times REF_{ADC} \times Range$$

where:

Code is the decimal equivalent of the binary code read from the ADC register.

REF_{ADC} = 1.25 V.

Range = 1 when in the 0 V to REF_{ADC} range.

Range = 2 when in the 0 V to 2 × REF_{ADC} range.

Range = 4 when in the 0 V to 4 × REF_{ADC} range.

Table 13. ADC Range Selected vs. LSB Size

Range	Value	Single-Ended ADC LSB	Differential ADC LSB
00	4 × REF_{ADC}[1]	4 × $REF_{ADC}/4096$	8 × $REF_{ADC}/4096$
01	2 × REF_{ADC}[1]	2 × $REF_{ADC}/4096$	4 × $REF_{ADC}/4096$
10	2 × REF_{ADC}[1]	2 × $REF_{ADC}/4096$	4 × $REF_{ADC}/4096$
11	REF_{ADC}[1]	$REF_{ADC}/4096$	2 × $REF_{ADC}/4096$

[1] REF_{ADC} = 1.25 V.

ANALOG INPUTS

The AD7293 has four analog inputs, $V_{IN}3$ to $V_{IN}0$. Depending on the configuration register setup, they can be configured as four single-ended inputs or two fully differential channels.

Single-Ended Mode

The AD7293 can have four single-ended analog input channels. In applications where the signal source is high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range is programmed to the following modes: 0 V to REF_{ADC}, 0 V to 2 × REF_{ADC}, or 4 × REF_{ADC} mode. The voltage, with respect to AGND on the ADC analog input pins, cannot exceed AV_{DD}.

Differential Mode

The AD7293 can have two differential input pairs ($V_{IN}3$ and $V_{IN}2$, $V_{IN}1$ and $V_{IN}0$). The amplitude of the differential signal is the difference between the signals at V_{IN+} and V_{IN-} ($V_{IN}0$ and $V_{IN}1$, or $V_{IN}3$ and $V_{IN}2$). Simultaneously drive V_{IN+} and V_{IN-} by two signals, each of amplitude REF_{ADC}, 2 × REF_{ADC}, or 4 × REF_{ADC}, depending on the range chosen, which are 180° out of phase.

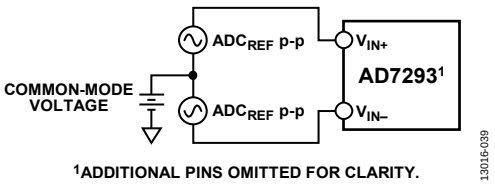


Figure 37. Differential Input (V_{IN+}/V_{IN-} Refer to $V_{IN}0$ to $V_{IN}3$)

Assuming that the 0 V to REF_{ADC} range is selected, the amplitude of the differential signal is, therefore, −REF_{ADC} to +REF_{ADC} peak to peak, regardless of the common-mode voltage (V_{CM}).

The common-mode voltage is the average of the two signals.

$$(V_{IN+} + V_{IN-})/2$$

The common-mode voltage is the voltage on which the two inputs are centered. The result is that the span of each input is $V_{CM} \pm REF_{ADC}/2$. This common-mode voltage must be set up externally.

When a conversion takes place, the common-mode voltage is rejected, resulting in a virtually noise free signal of amplitude −REF_{ADC} to +REF_{ADC}, corresponding to the digital output codes of −2048 to +2047 in twos complement format.

When using the 2 × REF_{ADC} range, the input signal amplitude extends from −2 × REF_{ADC} (V_{IN+} = 0 V and V_{IN-} = REF_{ADC}) to +2 × REF_{ADC} (V_{IN-} = 0 V and V_{IN+} = REF_{ADC}).

Similarly, when using the 4 × REF_{ADC} range, the input signal amplitude extends from −4 × REF_{ADC} (V_{IN+} = 0 V and V_{IN-} = REF_{ADC}) to +4 × REF_{ADC} (V_{IN-} = 0 V and V_{IN+} = REF_{ADC}).

Pseudo Differential Mode

The four uncommitted analog input channels can be configured as two pseudo differential pairs. Two uncommitted inputs, $V_{IN}0$ and $V_{IN}1$, are a pseudo differential pair, as are $V_{IN}2$ and $V_{IN}3$. In this mode, V_{IN+} is connected to the signal source, which can have a maximum amplitude of REF_{ADC}, 2 × REF_{ADC}, or 4 × REF_{ADC}, depending on the range that is chosen, to make use of the full dynamic range of the device. A dc input is applied to V_{IN-}. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The ADC channel allocation determines the channel specified as V_{IN+}. The differential mode must be selected to operate in the pseudo differential mode. The resulting converted pseudo differential data is stored in twos complement format in the result register.

For $V_{IN}0$, the governing equation for the pseudo differential mode is

$$V_{OUT} = 2(V_{IN+} - V_{IN-}) - REF_{ADC}$$

where:
V_{IN+} is the single-ended signal.
V_{IN-} is a dc voltage.
REF_{ADC} = 1.25 V.

The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC ground, allowing dc common-mode voltages to be cancelled.

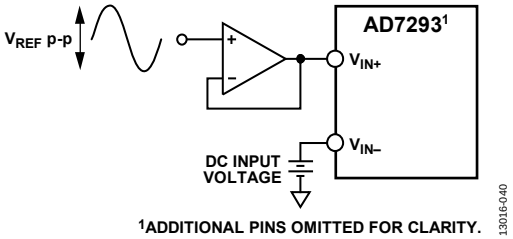


Figure 38. Pseudo Differential Input (V_{IN+}/V_{IN-} Refer to $V_{IN}0$ to $V_{IN}3$)

CURRENT SENSOR

Four bidirectional high-side current sense amplifiers are provided that can accurately amplify differential current shunt voltages in the presence of high common-mode voltages from AV_{DD} up to AV_{SS} + 60 V. The current sensors can be read directly, or optionally, they can be set to operate as part of the four independent closed-loop, drain current controllers. See the Closed-Loop section for more information.

In open-loop operation, the current sense amplifiers measure the current through a shunt resistor. Each amplifier can accept differential inputs up to ±200 mV. A selectable gain amplifies the measured voltage drop across the current sensor.

The AD7293 high-side current sense amplifier is configured as a differential integrator.

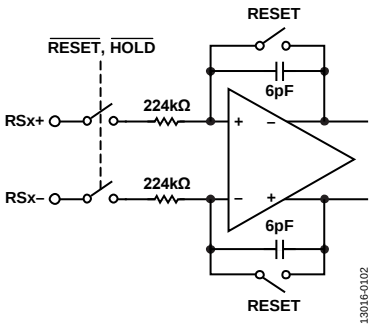


Figure 39. Current Sensor Internal Diagram

Before each measurement, the integrator is held in a reset state for 9.2 µs. The input is then connected and measured for a programmable amount of time, resulting in a gain equal to the following:

$$Gain = Integration\ Time/(224\ k\Omega \times 6\ pF)$$

Table 14. Current Sensor Gain Settings

Code	Typical Gain	Voltage Across R_{SENSE}[1] (mV)	Typical Integration Time (µs)
0000 (Default)	6.25	±200	8.4
0001	12.5	±100	16.8
0010	18.75	±66.67	25.2
0011	25	±50	33.6
0100	37.5	±33.33	50.4
0101	50	±25	67.2
0110	75	±16.67	100.8
0111	100	±12.5	134.4
1000	200	±6.25	268.8
1001	400	±3.125	537.6
1010	781.25	±1.6	1050

[1] R_{SENSE} is the external sense resistor.

When integration is complete, the input switches open, keeping the output constant until the ADC completes its conversion of the output signal. If no other ADC channels are enabled, the conversion takes an additional 4.2 µs. Otherwise, the current sense amplifier waits for its turn in the ADC conversion sequence before resetting and starting a new measurement.

Keep the external source impedance low with respect to the input resistance of the integrator to avoid creating a gain error.

Calculate the current sensor input channel LSB as follows:

$$V_{SENSE}\ LSB = (2 \times REF_{ADC})/(Gain \times 4096)$$

$$V_{RSx+} - V_{RSx-} = -REF_{ADC}/Gain, \text{ with DOUT} = 0x000$$

$$V_{RSx+} - V_{RSx-} = 0\ V, \text{ with DOUT} = 0x7FF$$

$$V_{RSx+} - V_{RSx-} = REF_{ADC}/Gain, \text{ with DOUT} = 0xFFF$$

where:
$V_{SENSE}\ LSB$ is the current sense input channel LSB size in volts.
V_{RSx+} is the voltage for the RSx+ pins.
V_{RSx-} is the voltage for the RSx− pins.
REF_{ADC} = 1.25 V.
Gain can be set between 6.25 and 781.25 as shown in Table 14.

$$I_{SENSE}\ LSB = 2 \times (REF_{ADC}/(Gain \times 4096 \times R_{SENSE}))$$

where:
$I_{SENSE}\ LSB$ is the current sense input channel LSB size in amperes.
R_{SENSE} is the external sense resistor.

Choosing the External Sense Resistor (R_{SENSE})

The resistor values used in conjunction with the current sense amplifiers on the AD7293 are determined by the specific application requirements in terms of voltage, current, and power.

Small resistors minimize power dissipation, have low inductance to prevent induced voltage spikes, and have good tolerance, which reduces current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipation and good accuracy; however, higher value resistors may be required to use the full input range of the ADC.

When the sense current is known, the voltage range of the AD7293 current sensor is divided by the maximum sense current to yield a suitable resistor value. If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, in which case, the current sensor gain can be increased to maximize the ADC input range used.

R_{SENSE} must be able to dissipate the I^2R losses. If the power dissipation rating of the resistor is exceeded, its value may drift, or the resistor may be damaged, resulting in an open circuit. If the power dissipation of the resistor is exceeded, it can result in a differential voltage across the AD7293 terminals in excess of the absolute maximum ratings.

$$R_{SENSE} \leq \frac{Current\ Sensor\ Input\ Voltage\ Range}{I_{SENSE(MAX)}}$$

where:
R_{SENSE} is the value of the current sense resistor in Ω.
Current Sensor Input Voltage Range is the current sensor amplifier input voltage range as dictated by the gain setting chosen (see Table 14).
$I_{SENSE\ (MAX)}$ is the maximum current required in A.

TEMPERATURE SENSOR

The AD7293 contains one local and two remote temperature sensors. The temperature sensors can continuously monitor the three temperature inputs, and new readings are automatically available every 5 ms.

The on-chip temperature sensor measures the device die temperature. The internal temperature sensor measures between −40°C and 125°C, where the LSB size is 0.125°C.

The AD7293 includes two remote temperate sensors. The device is factory calibrated to work with 2N3906 discrete transistors.

For RF applications, the use of high Q capacitors functioning as a filter protects the integrity of the measurement. Connect these capacitors between the base and the emitter, as close to the external device as possible. However, large capacitances affect the accuracy of the temperature measurement; therefore, the recommended maximum capacitor value is 100 pF. In most cases, a capacitor is not required; the selection of any capacitor is dependent on the noise frequency level.

The AD7293 automatically cancels out the effect of parasitic, base, and collector resistance on the temperature reading. This cancelation gives a more accurate result, without the need for any user characterization of the parasitic resistance. The AD7293 can compensate for up to 4 kΩ series resistance typically.

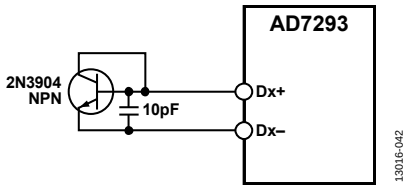


Figure 40. Measuring Temperature Using a NPN Transistor

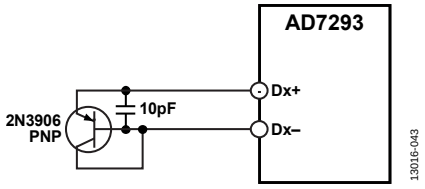


Figure 41. Measuring Temperature Using a PNP Transistor

Table 15. Temperature Sensor Data Format

Temperature (°C)	$T_{SENSE}x$ Result Registers (Page 0x00, Register 0x20 to Register 0x22), Bits[D15:D4]
−40	0110 1100 0000
−25	0111 0011 1000
−10	0111 1011 0000
−0.125	0111 1111 1111
0	1000 0000 0000
+0.125	1000 0000 0001
+10	1000 0101 0000
+25	1000 1100 1000
+50	1001 10 01 0000
+75	1010 0101 1000
+100	1011 0010 0000
+125	1011 1110 1000

INTERNAL CHANNEL MONITORING

The ADC can internally read the outputs of the four bipolar DACs, AV_{DD}, $DACV_{DD-UNI}$, $DACV_{DD-BI}$, AV_{SS}, and the voltage on the RS0+ to RS3+ pins in the background. A sequencer is available that allows multiple channels to be converted in a predetermined sequence.

The ADC is used in its single-ended mode. The LSB size varies with the different supply monitoring registers. AV_{DD} and $DACV_{DD-BI}$ are divided by 5, and $DACV_{DD-UNI}$ is divided by 20 to scale within the 0 V to REF_{ADC} range. AV_{SS} is level shifted to within a −7.5 V to +2.5 V range, where 0x0000 equates to approximately −7.5 V, and 0xFFFF equates to approximately +2.5 V. REF_{ADC} = 1.25 V.

For $RSx+_{MON}$ (internal monitoring of the voltage on the RS0+ to RS3+ pins), divide by 50 to scale them to the 0 V to REF_{ADC} range. Use the ADC in single-ended mode. The $RSx+_{MON}$ monitor result registers store the 12-bit ADC results for the current sense supply channels (see Figure 42).

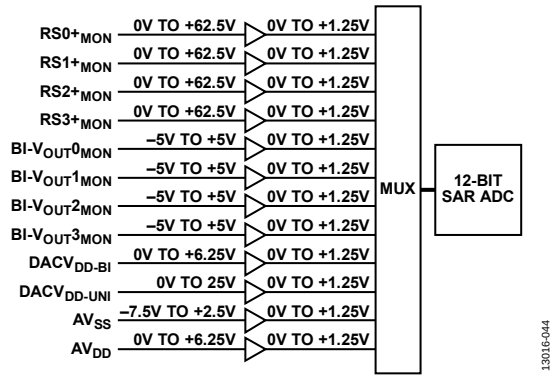


Figure 42. Internal Channel Monitoring

DAC OPERATION

The AD7293 contains eight 12-bit DACs, four bipolar DACs, and four unipolar DACs. These provide digital control with 12 bits of resolution combined with offset range select registers and a 2.5 V internal reference. The DAC core is a 12-bit string DAC. The resistor string structure consists of a string of resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. When one of the switches connecting the string to an amplifier is closed, the voltage is tapped off. This architecture is inherently monotonic and linear. The eight DACs are split into two groups based on their output range.

Bipolar DACs

The bipolar DACs ($BI\text{-}V_{OUT}0$, $BI\text{-}V_{OUT}1$, $BI\text{-}V_{OUT}2$, and $BI\text{-}V_{OUT}3$) can be configured through the offset range registers to 0 V to +5 V, −5 V to 0 V, or −4 V to +1 V (see Table 85).

Writing to these register addresses sets the 12-bit DAC output voltage. There is also a load bit and a copy bit (see Table 27).

If the load bit is set to 1, the device waits for LDAC to become active before loading the voltage codes onto the DACs rather than immediately after the write operation. If the copy bit is set to 1 when writing to a bipolar DAC register, it sets all bipolar DAC registers to the same value in open-loop mode only.

$$V_{OUT} = \left(2 \times V_{REFIN} \times \left(\frac{D}{2^n}\right)\right) + V_{OFFSET}$$

where:

V_{REFIN} = 2.5 V.

D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 4095 for the 12-bit AD7293).

n is the resolution of the DAC.

V_{OFFSET} = 0 V (0 V to +5 V range), −4 V (−4 V to +1 V range), or −5 V (−5 V to 0 V range).

Table 16. Bipolar DAC Voltage Offset Ranges

Range (V)	0x000	0xFFF	V_{OFFSET} (V)
0 to +5	0 V	2 V × V_{REFIN}	0
−4 to +1	−1.6 V × V_{REFIN}	0.4 V × V_{REFIN}	−4
−5 to 0	−2 V × V_{REFIN}	0 V	−5

The ADC can also monitor these four outputs.

The bipolar DACs in addition to the four current sensors in the PA controller can operate as four independent closed-loop drain current controllers (see the Closed-Loop Mode section).

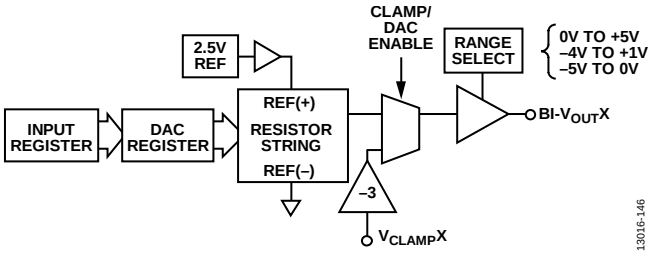


Figure 43. Bipolar DAC Architecture Block Diagram

Unipolar DACs

The unipolar DAC outputs, UNI-V_{OUT}0, UNI-V_{OUT}1, UNI-V_{OUT}2, and UNI-V_{OUT}3, can be configured through the offset range registers to 0 to 5 V, 2.5 V to 7.5 V, or 5 V to 10 V (see Table 84).

The DACs have one control register to control the interaction between two registers: input registers and output registers. The output registers contain the digital code used by the resistor strings as well as a copy and load bit. Writing to these register addresses sets the 12-bit DAC output voltage codes.

If the load bit is set to one, the device waits for LDAC to become active before loading the voltage codes onto the DACs rather than immediately after the write operation. If the copy bit is set to 1, writing to a unipolar DAC registers sets all the other unipolar DAC registers to the same value.

$$V_{OUT} = \left(2 \times V_{REFIN} \times \left(\frac{D}{2^n}\right)\right) + V_{OFFSET}$$

where:
V_{REFIN} = 2.5 V.
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 4095 for the 12-bit AD7293).
n is the resolution of the DAC.
V_{OFFSET} = 0 V (0 V to 5 V range), 2.5 V (2.5 V to 7.5 V range), or 5 V (5 V to 10 V range).

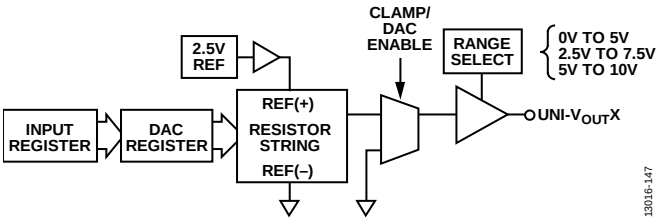


Figure 44. Unipolar DAC Architecture Block Diagram

Table 17. Unipolar DAC Voltage Offset Ranges

Range (V)	0x000	0xFFF	V_{OFFSET} (V)
0 to 5	0 V	2 V × V_{REFIN}	0
2.5 to 7.5	V_{REFIN}	3 V × V_{REFIN}	2.5
5 to 10	2 V × V_{REFIN}	4 V × V_{REFIN}	5

DAC Enabling and Clamping

On power-up, the DAC outputs default to their clamp values (see Table 18). All DACs can be enabled and disabled/clamped via the DAC enable register (common to all pages).

Table 18. Clamp Values

DAC Output	Clamp Value
UNI-V_{OUT}0	0 V
UNI-V_{OUT}1	0 V
UNI-V_{OUT}2	0 V
UNI-V_{OUT}3	0 V
BI-V_{OUT}0	−3 × V_{CLAMP}0
BI-V_{OUT}1	−3 × V_{CLAMP}0
BI-V_{OUT}2	−3 × V_{CLAMP}1
BI-V_{OUT}3	−3 × V_{CLAMP}1

All DACs (bipolar DACs only on power-up) can be set to clamp using the digital SLEEP0 and SLEEP1 pins. The DAC outputs controlled by the digital SLEEP0 and SLEEP1 pins are selectable by writing to the corresponding sleep bit in the DAC snooze/SLEEPx pin register (see Table 45) in the configuration page. When the SLEEPx pin is pulled active, the corresponding unipolar and bipolar DACs associated with the pin are forced into clamp. Clamping does not clear the DAC output register value, making it possible to return to the same voltage as before the clamp event. While in clamp mode, the DAC registers can be updated. When a SLEEPx pin is used, a snooze function is available that clears the DAC registers and requires an additional write to the DAC enable register to wake up the DAC after clearing the clamp condition.

The bipolar DACs power-on reset and clamp value is dependent on the V_{CLAMP}0 and V_{CLAMP}1 voltage level. After a power-on reset or when the digital SLEEP0 or SLEEP1 pin is configured to trigger a clamp, the bipolar DAC outputs reset to the clamp value (see Table 18).

After a power-on reset or when the digital SLEEP0 or SLEEP1 pin is configured to trigger clamping, the unipolar DAC outputs default to 0 V.

Software Clamping: Internal ALERT0 Routing

There is an option to allow the ALERT0 alert to trigger the clamp function. The DACs power back up when the alert is cleared without an additional write to the DAC enable registers. Bit D1 of the general register in the configuration page allows ALERT0 control over the clamping function of the four bipolar DACs.

PMOS Drain Switch Control

The AD7293 PA_ON output pin is capable of driving an external PMOS switch. This external PMOS turns on or off the drain current to a PA field effect transistor (FET). The PA_ON output pin controls the device during power-up and power-down. This feature can also be used as a protection feature when an alert condition is detected because ALERT0 alerts or an AV_{SS} or AV_{DD} supply failure can be used to trigger the PA_ON pin. PAV_{DD} determines the maximum voltage at the output of the PA_ON pin. The off state is equal to PAV_{DD} while the on state is equal to AGND. The default state of the PA_ON signal is off.

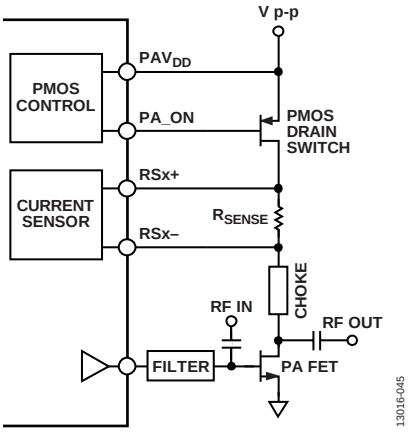


Figure 45. PMOS Drain Switch Control

REFERENCE

The AD7293 has one high performance, 2.5 V on-chip reference accessed via the V_{REFOUT} pin. Noise performance can be improved by the addition of a 10 nF capacitor between the V_{REFOUT} pin and the AGND pin. Connect V_{REFOUT} to the V_{REFIN} pin to use the on-chip reference of the AD7293. An internal amplifier attenuates to the ADC core, making the voltage at the ADC, REF_{ADC} = 1.25 V, half of V_{REFIN} = 2.5 V. Use the REF_{ADC} pin for measurement purposes only.

A 220 nF capacitor is required on the REF_{ADC} pin and must be placed as close to the AD7293 as possible with no vias. The internal reference typically requires 20 ms to power up and settle when using a 220 nF decoupling capacitor on the REF_{ADC} pin.

Buffer the internal reference before it is used by external circuitry.

The AD7293 can also operate with an external reference of 2.5 V connected to the V_{REFIN} pin.

If using an external reference, select a low temperature coefficient specification, such as the ADR4525, to reduce the temperature dependence of the system output voltage on ambient conditions.

V_{DRIVE} FEATURE

The AD7293 also has a V_{DRIVE} feature that controls the voltage at which the SPI operates. Connect the V_{DRIVE} pin to the supply to which the SPI bus is pulled. The V_{DRIVE} pin sets the input and output threshold levels for the digital logic pins. The V_{DRIVE} feature allows the AD7293 to interface with 1.8 V, 3.3 V, and 5 V processors.

OPEN-LOOP MODE

In open-loop mode, the default mode of operation, the current sense amplifiers and bipolar DACs operate independently.

CLOSED-LOOP MODE

Alternatively, the AD7293 current sensors and bipolar DACs can operate as four independent closed-loop drain current controllers (closed-loop mode).

In closed-loop operation, the drain current through the PA FET is set and automatically maintained by the PA controller through a regulation circuit that includes the DAC and current sense monitor. The control loop sets the PA bias current and continuously maintains a constant voltage across the sense resistor (V_{SENSE} = $I_{SENSE} \times R_{SENSE}$). When the DAC current updates, the closed-loop adjusts the gate voltage of the PA until the drain current matches the corresponding DAC code. The continuous regulation of the loop compensates for variations of the PA threshold or voltage drop on the LPF due to the PA gate current. The integrator leads to a smooth transition on the output of the pin.

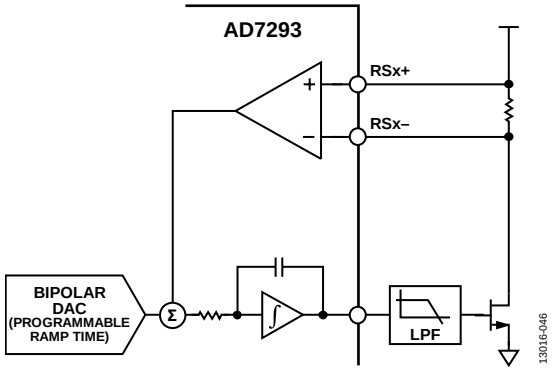


Figure 46. Closed-Loop Control

Each of the four current closed loops consists of a DAC, an error amplifier, and an integrator in the forward path to drive the gate of the PA FET. A high-side current sense amplifier in the feedback path senses that PA drain bias current and closes the loop.

An external gate filter can be introduced between the gate of the power amplifier and the integrator output pins when operating in closed-loop mode to limit the noise bandwidth and to ensure PA stability. The gate filter time constant (τ_G) must be between 5 µs and 50 µs.

Adjustable Closed-Loop Setpoint Ramp Time

The transition between two successive setpoints of the DAC are interpolated in a linear manner with the aid of a ramp generator. When moving to a new closed-loop setpoint, limiting the rate of change of the drain current is often required. To facilitate this, the AD7293 can automatically generate a linear ramp between the old and new DAC settings, over a programmable duration. Write to the ramp time register to enable this feature, which allows ramp times of between 4 ms and 31.75 ms to generate, programmable in 250 µs steps. If a value of less than 4 ms is written to the register, the ramp generator disables, and the new

target DAC code is set immediately. Depending on the overall loop time constant, an additional settling time can be required after the end of the ramp for the drain current to reach the prescribed set point.

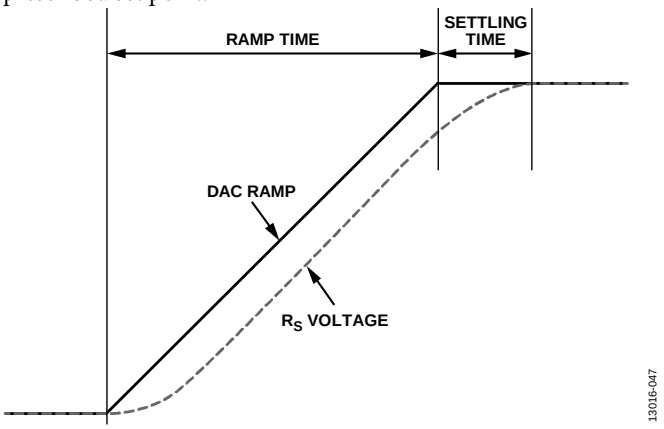


Figure 47. Programmable Ramp Time Representation

Fast Ramp Feature

To accelerate the initial settling of the closed loop, the fast ramp feature can be enabled. When the ramp time register is programmed to 0x0000, the ramp generator disables. In this mode, when the current sense reading is less than 0x00F, the integrator time constant is reduced to 408 µs, allowing the gate control voltage to reach the PA threshold voltage as quickly as possible. When above this current, the time constant automatically returns to its programmed value. When a different switching threshold is desired, use the current sense offset register to allow Code 0x00F to represent a higher or lower current. This features may be useful to prevent unwanted overshoot (lower threshold) or to speed up settling (higher threshold).

Closed-Loop Sequencing

On power-up or following a reset, the system is configured as follows:

- The four bipolar outputs (BI-V_{OUT}0 to BI-V_{OUT}3) are set to their clamp value, regardless of the levels of the SLEEP0 or the SLEEP1 pin.
- All of the DAC data registers are set to 0x0000, and the bipolar DACs operate in open loop.
- The PA_ON signal is set to the off state.

To enter closed-loop operation, it is important to follow these steps:

1. Configure the AD7293 for closed-loop operating mode by writing to the integrator limit and closed-loop control register (Register 0x28) from the configuration page. Additionally, if PMOS drain switch control is used, set the PA_ON signal to the on state by writing to the PA_ON control register (Register 0x29) from the same page.
2. The DACs must be programmed at this point. Choose the target drain current such that the PA is within its operating region. The I_{SENSE} gain setting must be left at the default value of 6.25 in closed-loop mode. At this point, setting the corresponding ramp time to 0 may be required so that the ramp generator disables, and the DAC jumps to the target value quickly.
3. Release the DACs out of clamp by writing to the DAC enable register (Register 0x04) and wait 5 ms for the PAs to settle to the initial drain current. At this point, ensure that the programmed ramp time is 0, such that the ramp generator is disabled, and the DAC resolves to the target value.
4. Program the desired ramp times for each channel by writing to the corresponding ramp time registers (Register 0x2A to Register 0x2D) from the configuration page.
5. Program the target drain current by writing to the DAC registers. In addition to the ramp time, allow a delay of 1 ms before checking whether the PA drain current corresponds to the intended target current. During the active ramp period, if the DAC input register (Page 0x00, Register 0x30 to Register 0x37) is read back, it is seen as ramping up or ramping down to the target code.

If the user writes a new target drain current while the ramp is active, the device restarts the internal timer and aims to reach the new drain current within the programmed ramp time.

If the device is configured in closed-loop mode, the ADC runs conversions on the corresponding current sensor channel in the background. In addition to the current sensor conversions, additional channels can be configured to run background conversions (via the corresponding background enable registers). The user can read back the conversion results via the channel specific result registers in Page 0x00 and Page 0x01.

Closed-Loop Integrator Programmable Voltage Limit

The AD7293 ADC can monitor the voltage at the output of the integrator by writing to a register (Register 0x23) from the configuration page (see Table 46).

The integrator voltage limit feature allows the user to set upper and lower limits on the integrator output voltage in closed-loop mode of operation. When the integrator limit is active, the integrator pauses and the output voltage holds constant. The polarity of the error amplifier (comparison between measured current and target current) determines when it is safe to deactivate the soft limit. For example, a lower target current is programmed, which makes the integrator output decrease, making it safe to deactivate the integrator limit.

It is recommended to use the hysteresis registers (see Table 66 and Table 69) to avoid the device switching in and out of the alert condition close to the limits. Additionally, the integrator limit feature can be made a function of the upper/lower limits only by ignoring the polarity of the error amplifier (via D2 of the general register (Register 0x14) from the configuration page). The integrator limit feature does not enable by default and can be enabled by writing to the integrator limit and closed-loop control register (Register 0x28).

Closed-Loop Range Upper Voltage Limit

An analog circuit within the output integrator creates a hardware range upper limit on the output voltage of either 0 V or 1 V, as shown in Table 19. If the hardware limiting circuitry is active, an alert appears on the INT_{LIMITx} and AV_{SS}/AV_{DD} alert register (Register 0x1A). See the $INT_{LIMIT}x$ and AV_{SS}/AV_{DD} Alert Register (Register 0x1A) section.

Table 19. Closed-Loop Range Upper Voltage Limit

Operation	Bipolar DAC Range (V)	Range Limit
Open Loop	X = don't care	Off
Closed Loop	0 to +5	Off
Closed Loop	−4 to +1	On (1 V)
Closed Loop	−5 to 0	On (0 V)

DIGITAL INPUT/OUTPUT REGISTERS

Eight pins can be set as GPIOs or can perform various digital functions. Three registers located on the configuration page set up the functionality of the GPIO interface. GPIO0 to GPIO3 default to the GPIOs on power-up. ALERT1, SLEEP0, SLEEP1, and LDAC default to digital functions on power-up.

The GPIO register (Register 0x5) configures the GPIOs in the device. In GPIO mode, and with the output drivers enabled, the GPIO outputs reflect the value written to this register. In functional mode, any write to this register has no effect on the GPIO outputs. See the GPIO Register (Register 0x05) section.

The digital output enable register (Register 0x11) enables the output drivers of the GPIO pins; therefore, when using one of the pins as an output in GPIO mode or functional mode (for alerts and busy), the corresponding bit must be set. See the Digital Output Enable Register (Register 0x11) section.

The digital input/output function register (Register 0x12) allows the user to put the relevant pin into GPIO mode or functional mode. See the Digital Input/Output Function Register (Register 0x12) section.

The digital functional polarity register (Register 0x13) sets the polarity of the digital input/output pins in functional mode only. The associated input/output signal can be made active low or active high. See the Digital Functional Polarity Register (Register 0x13) section.

LOAD DAC (LDAC PIN)

The AD7293 DACs have doubled buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. If the load bit is held high when writing to a DAC, updates to the DAC register are controlled by the LDAC pin.

Instantaneous DAC Updating (Asynchronous)

In this operation mode, the SPI data is clocked into the DAC input register on the rising edge of the SCLK. The output register is updated, and the output begins to change. Instantaneous DAC updating is only applicable when the load bit is not set when writing to the DAC register. Hold the LDAC pin in its false state.

Deferred DAC Updating (Synchronous)

In this mode, the SPI data is clocked into the DAC input registers on the rising edge of the SCLK. However, the update of the output registers can be blocked during the SPI write by setting the load bit. The output registers can be synchronously updated (data is transferred from the DAC input register to the DAC output register) by taking the LDAC pin to its true state.

ALERTS AND LIMITS

The high and low limit pages comprise registers that set the high and low alerts for the analog input channels, the current sensors, the internal supply monitoring channels, the internal bipolar DAC monitoring channels, and the RSx+ monitoring channels. Each register is 16 bits in length; values are 12-bit, left justified (padded with 0s as the four LSBs). On power-up, the low limit registers contain all zeros, whereas the high limit registers contain 0xFFF0.

The alert high limit registers on Page 0x04 (High Limit 0) and Page 0x05 (High Limit 1) store the upper limit that activates an alert (see the High Limit 0 (Page 0x04) section and the High Limit 1 (Page 0x05) section). If the conversion result is greater than the value in the alert high limit register, an alert triggers. The alert low registers on Page 0x06 (Low Limit 0) and Page 0x07 (Low Limit 1) store the low limit that activates an alert (see the Low Limit 0 (Page 0X06) section and the Low Limit 1 (Page 0X07) section). If the conversion result is less than the value in the alert low limit register, an alert triggers.

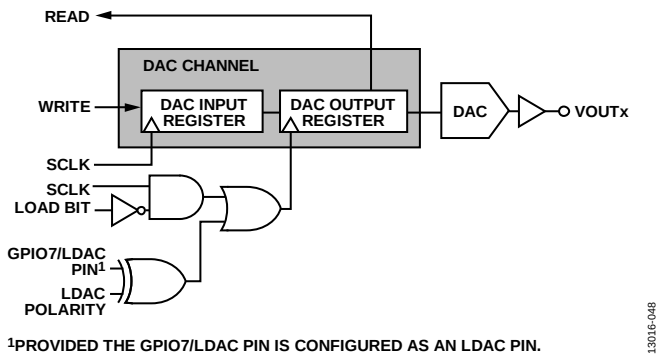


Figure 48. Simplified Diagram of Input Loading Circuitry for a Single DAC

If a conversion result exceeds the high or low limit set in the alert limits register, the AD7293 signals an alert in one or more of the following ways:

- Via hardware using the GPIO3/ALERT0 and GPIO4/ALERT1 pins
- Via software using the alert bits or registers on the alert page (Page 0x10).

ALERTx Pins

Two pins can be configured as ALERTx pins. On power-up, Pin 2 (GPIO4/ALERT1) is configured as an alert whereas Pin 53 is configured as a GPIO (GPIO3/ALERT0). When these pins are configured as ALERTx pins, any combination of high and low alerts on any of the ADC channels can route to these pins. The polarity of the alert output pins can be set to active high or active low via the digital function polarity register on the configuration page.

If an alert pin signals an alert event and the contents of the alert flags registers are not read before the next conversion is completed, the contents of the register may change if the out of range signal returns to the specified range. In this case, the ALERT0 or ALERT1 pin no longer signals the occurrence of an alert event.

Software Alerts Page

The alert summary register (Register 0x10) contains a summary of alerts for the voltage, temperature sensor, current sensor, and other monitoring inputs that have violated limits. See the Alert Summary (ALERTSUM) Register (Register 0x10) section.

To gather more detailed information, the remaining registers contain two individual status bits per channel: one corresponding to the high limit and the other corresponding to the low limit. A bit with a status of one shows the channel on which the violation occurred and whether the violation occurred on the high or low limit.

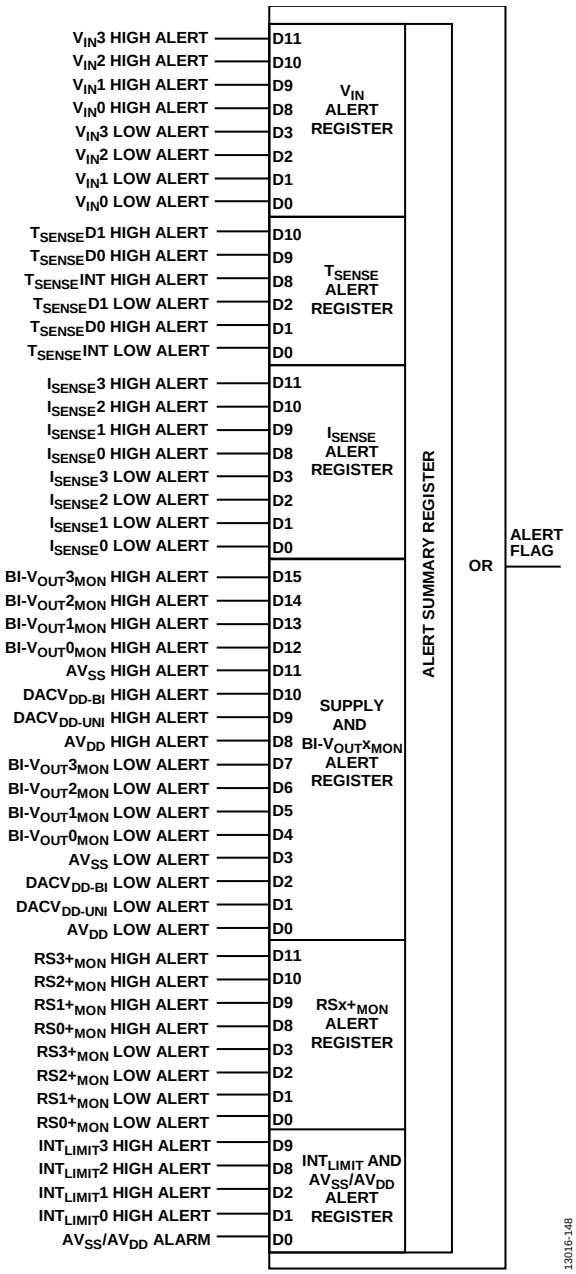


Figure 49. Software Alerts Page

GPIO0 to GPIO3 Routing to ALERT1

A bit in the general register allows the GPIO0 to GPIO3 status to route to the ALERT1 pin. Set GPIO0 to GPIO3 up as inputs (bit set to 0 in the digital output enable register). If the GPIO is read as 1, this read appears on ALERT1, and the GPIO register can be read for the status of the pin to detect which pin has caused ALERT1 to become active.

AV_{DD} AND AV_{SS} ALARM

There are comparators on AV_{DD} (+3.6 V typical) and AV_{SS} (−4.1 V typical) that can be routed to the ALERTx pins or can be used to control the PA_ON state and to put the bipolar DACs/integrator outputs in the clamp state. By default, these alarms are enabled.

When AV_{SS} is greater than −4.1 V, there is a mask register available whereby an alert of AV_{SS} or AV_{DD} is not creating an alert on the ALERTx pin.

MAXIMUM AND MINIMUM PAGES

The maximum and minimum pages contain storage registers for the maximum and minimum conversion results. This function is useful when monitoring the minimum and maximum conversion values over time is required.

HYSTERESIS

The hysteresis value determines the reset point for the ALERTx pin and/or software alert bit if a violation of the limits occurs. The hysteresis register stores the hysteresis value when using the limit registers. Each pair of limit registers has a dedicated hysteresis register (see Figure 50). If software is periodically polling the device to detect an alert, the hysteresis can be useful to ensure that no out of limit condition is missed.

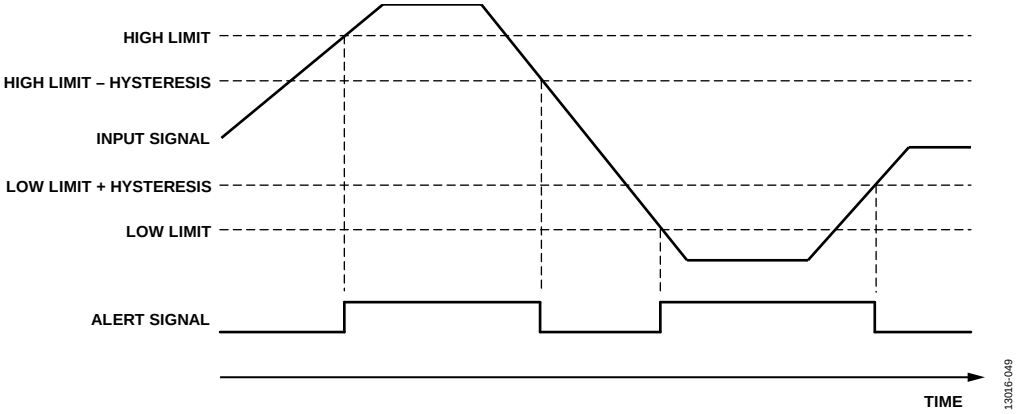
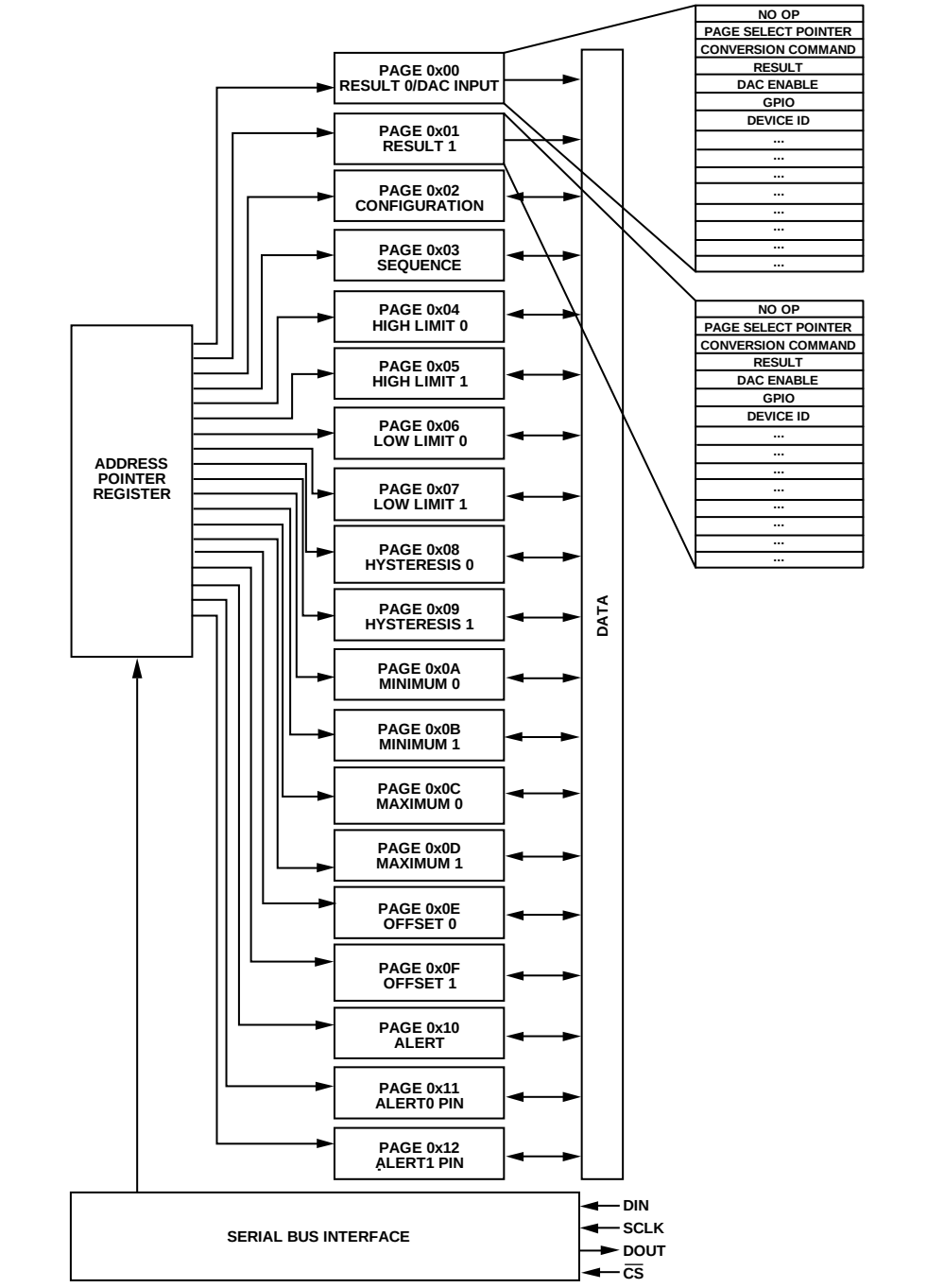


Figure 50. Hysteresis

REGISTER SETTINGS

The register structure for the AD7293 is partitioned using pages. There are 19 pages in total. Each contains a different number of registers that are used to store and access information to configure and control the device. Each page and subregister have an address that an 8-bit address pointer register points to when communicating with it. The address pointer register is an 8-bit register. The six LSBs (D5 to D0) are the pointer address bits that point to one of the AD7293 data registers, and the MSB (D7) is the read (high)/write (low) bit. There are read only and read/write registers.



NOTES
1. EACH PAGE CONTAINS 7 COMMMON REGISTERS IN ADDITION TO PAGE SPECIFIC REGISTERS.
2. THE CONFIGURATION PAGE CONTAINS THE REGISTERS THAT SELECT THE BACKGROUND MODE CYCLE OF CHANNELS TO BE CONVERTED BY THE ADC. THE SEQUENCE PAGE APPLIES TO COMMAND MODE ONLY.

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Figure 51. Register Structure

REGISTERS COMMON TO ALL PAGES

A number of registers is common to all pages. The register function is the same for all pages.

No Op Register (Register 0x00)

The no op register does not physically exist and this address space is reserved to prevent any writes to the device when the input data line is held low.

Page Select Pointer Register (Register 0x01)

This 8-bit pointer register selects the page that the user is trying to access. A read of this register indicates the page the user is currently pointing to. The two MSBs are reserved and the six LSBs can be written to select any of the pages.

Conversion Command (Register 0x02)

The conversion command register is a special 8-bit register used to initiate a conversion. To command a conversion, write the command register address to the device with the MSB read bit set. When the device address pointer register receives a special conversion command, the previous contents of the address pointer are retained and used to determine which channel to convert. If pointing to the sequence register, the next channel in the sequence converts.

Result Register (Register 0x03)

The 16-bit, read only ADC data register provides read access to the most recent ADC conversion result in command mode. Otherwise, it is necessary for the application software to keep track of what channel was converted.

DAC Enable Register (Register 0x04)

This 8-bit register enables the DACs. See Table 20.

GPIO Register (Register 0x05)

This 8-bit register configures the GPIOs in the device. In GPIO mode, and with the output drivers enabled, the GPIO outputs reflect the value written to this register. In functional mode, any write to this register has no effect on the GPIO outputs. The status (high/low) of the GPIO pins can be read back by reading this register (both in functional and GPIO modes). See Table 21.

Device ID Register (Register 0x0C)

This 16-bit read-only register stores the Device ID assigned to Analog Devices, Inc. See Table 22 for more information.

Software Reset Register (Register 0x0F)

To issue a software reset write a specific value, 0x7293, to this 16-bit register and pull $\overline{CS}$ high. The user must write 0x0000 to this register to clear it following the software reset. See Table 23.

Table 20. DAC Enable Register

Bit Number(s)	Bit Name	Description
D7	BI-V_{OUT}3	0: disable. 1: enable.
D6	BI-V_{OUT}2	0: disable. 1: enable.
D5	BI-V_{OUT}1	0: disable. 1: enable.
D4	BI-V_{OUT}0	0: disable. 1: enable.
D3	UNI-V_{OUT}3	0: disable. 1: enable.
D2	UNI-V_{OUT}2	0: disable. 1: enable.
D1	UNI-V_{OUT}1	0: disable. 1: enable.
D0	UNI-V_{OUT}0	0: disable. 1: enable.

Table 21. GPIO Register

Bit Number(s)	Bit Name	Description
D7	GPIO7	0: disable. 1: enable.
D6	GPIO6	0: disable. 1: enable.
D5	GPIO5	0: disable. 1: enable.
D4	GPIO4	0: disable. 1: enable.
D3	GPIO3	0: disable. 1: enable.
D2	GPIO2	0: disable. 1: enable.
D1	GPIO1	0: disable. 1: enable.
D0	GPIO0	0: disable. 1: enable.

Table 22. Device ID Register

Bit Number(s)	Bit Name	Description
[15:0]	ID register	Analog Devices, Device ID = 0x0018

Table 23. Software Reset Register

Bit Number(s)	Bit Name	Description
[15:0]	Reset register	Software reset = 0x7293

RESULT 0/DAC INPUT (PAGE 0x00)

Result 0/DAC input is located at Page 0x00. It contains result registers for the ADC, the temperature sensor, and the current sensor channel. The page also contains DAC input registers to set the output voltage.

Table 24. Result 0/DAC Input (Page 0x0)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	$V_{IN}0$	2	R	0x0000
0x11	$V_{IN}1$	2	R	0x0000
0x12	$V_{IN}2$	2	R	0x0000
0x13	$V_{IN}3$	2	R	0x0000
0x20	T_{SENSE}INT	2	R	0x0000
0x21	T_{SENSE}D0	2	R	0x0000
0x22	T_{SENSE}D1	2	R	0x0000
0x28	$I_{SENSE}0$	2	R	0x0000
0x29	$I_{SENSE}1$	2	R	0x0000
0x2A	$I_{SENSE}2$	2	R	0x0000
0x2B	$I_{SENSE}3$	2	R	0x0000
0x30	UNI-$V_{OUT}0$	2	R/W	0x0000
0x31	UNI-$V_{OUT}1$	2	R/W	0x0000
0x32	UNI-$V_{OUT}2$	2	R/W	0x0000
0x33	UNI-$V_{OUT}3$	2	R/W	0x0000
0x34	BI-$V_{OUT}0$	2	R/W	0x0000
0x35	BI-$V_{OUT}1$	2	R/W	0x0000
0x36	BI-$V_{OUT}2$	2	R/W	0x0000
0x37	BI-$V_{OUT}3$	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

Voltage Input ($V_{IN}x$) Result Registers (Register 0x10 to Register 0x13)

These registers store the 12-bit ADC results from the four input channels.

In single-ended mode, the LSB size is $REF_{ADC}/4096$ when the 0 V to REF_{ADC} range is selected, $2 \times REF_{ADC}/4096$ when the 0 V to $2 \times REF_{ADC}$ range is selected, and $4 \times REF_{ADC}/4096$ when the 0 V to $4 \times REF_{ADC}$ range is selected (which is the default value). REF_{ADC} = 1.25 V. See the ADC Transfer Functions section for more information. See Table 25 for more information.

Temperature Sensor (T_{SENSE}INT and T_{SENSE}Dx) Result Registers (Register 0x20 to Register 0x22)

These registers store the 12-bit ADC results from the three temperature sensor channels. 1 LSB = 0.125°C. See Table 26 for more information.

Current Sensor ($I_{SENSE}x$) Result Registers (Register 0x28 to Register 0x2B)

These registers store the 12-bit ADC results from the four current sensor channels. See Table 25 for more information.

DAC Input (UNI-$V_{OUT}x$ and BI-$V_{OUT}x$) Registers (Register 0x30 to Register 0x37)

Writing to these register addresses sets the 12-bit DAC output voltage codes, as shown in Table 27.

If the load bit is set to 1, the device waits for the DAC load pin (GPIO7/LDAC) before loading the voltage codes onto the DACs rather than immediately after the write operation. If the copy bit is set to 1, writing to any of the four DAC registers (unipolar and bipolar are grouped separately) sets all the other DAC registers to the same value.

While reading back the DAC result registers, only the 12-bit internal DAC output register value is visible to the user. Bits[D3:D0] read 0 irrespective of the status of the copy and load bits.

Table 25. Voltage Input (Register 0x10 to Register 0x13) and Current Sensor (Register 0x28 to Register 0x2B) Result Registers

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

Table 26. Temperature Sensor Result Register

Bit Number(s)	Bit Name	Description
D15	B11	0: −256°C 1: 0°C
D14	B10	0: 0°C 1: 128°C
D13	B9	0: 0°C 1: 64°C
D12	B8	0: 0°C 1: 32°C
D11	B7	0: 0°C 1: 16°C
D10	B6	0: 0°C 1: 8°C
D9	B5	0: 0°C 1: 4°C
D8	B4	0: 0°C 1: 2°C
D7	B3	0: 0°C 1: 1°C
D6	B2	0: 0°C 1: 0.5°C
D5	B1	0: 0°C 1: 0.25°C
D4	B0	0: 0°C 1: 0.125°C
[D3:D0]	Reserved	Reserved

Table 27. DAC Input Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D2]	D1	D0
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved	Copy	Load

Table 28. Copy and Load Bit Descriptions

Bit Number(s)	Bit Name	Description
[D15:D4]	B11 to B0	Data bits
D1	Copy	0: no action 1: copies data to all DAC registers
D0	Load	0: all channels updated with latest results 1: input register loaded but output voltage dependent on LDAC

RESULT 1 (PAGE 0x01)

Table 29. Result 1 (Page 0x01)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD}	2	R	0x0000
0x11	$DACV_{DD-UNI}$	2	R	0x0000
0x12	$DACV_{DD-BI}$	2	R	0x0000
0x13	AV_{SS}	2	R	0x0000
0x14	$BI\text{-}V_{OUT}0_{MON}$	2	R	0x0000
0x15	$BI\text{-}V_{OUT}1_{MON}$	2	R	0x0000
0x16	$BI\text{-}V_{OUT}2_{MON}$	2	R	0x0000
0x17	$BI\text{-}V_{OUT}3_{MON}$	2	R	0x0000
0x28	$RS0+_{MON}$	2	R	0x0000
0x29	$RS1+_{MON}$	2	R	0x0000
0x2A	$RS2+_{MON}$	2	R	0x0000
0x2B	$RS3+_{MON}$	2	R	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

Voltage Supply Monitor Result Registers (Register 0x10 to Register 0x13)

The ADC is used in its single-ended mode. The LSB size varies with the different supply monitoring registers. AV_{DD} and $DACV_{DD-BI}$ are divided by 5, and $DACV_{DD-UNI}$ is divided by 20 to scale within the 0 V to REF_{ADC} range. AV_{SS} is level shifted to within a −7.5 V to +2.5 V range, where 0x0000 equates to approximately −7.5 V and 0xFFFF equates to approximately +2.5 V. REF_{ADC} = 1.25 V.

Bipolar DAC Internal Monitor Result ($BI\text{-}V_{OUT}0_{MON}$ to $BI\text{-}V_{OUT}3_{MON}$) Registers (Register 0x14 to Register 0x17)

These registers store the 12-bit ADC results from the four internal inputs for monitoring the bipolar DAC outputs in open-loop mode or the integrator outputs in closed-loop mode. The DAC monitoring channel voltages between −5 V and +5 V are level shifted to the 0 V to REF_{ADC} range before conversions.

$RSx+_{MON}$ Result Registers (Register 0x28 to Register 0x2B)

The voltages on the RSx+ pins ($RSx+_{MON}$) are divided by 50 to scale them to the 0 V to REF_{ADC} range. Use the ADC in single-ended mode. The $RSx+_{MON}$ monitor result registers store the 12-bit ADC results for the current sense supply channels.

Table 30. Monitor Register Configuration

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

CONFIGURATION (PAGE 0x02)

This page contains the registers that configure the device operation.

Table 31. Configuration (Page 0x2)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x11	Digital output enable	2	R/W	0x0010
0x12	Digital input/output function	2	R/W	0x000F
0x13	Digital functional polarity	2	R/W	0x0090
0x14	General	2	R/W	0x0000
0x15	V_{IN}x Range 0	2	R/W	0x0000
0x16	V_{IN}x Range 1	2	R/W	0x0000
0x17	V_{IN}x differential/ single-ended enable	2	R/W	0x0000
0x18	V_{IN}x filter	2	R/W	0x0000
0x19	V_{IN}x background enable	2	R/W	0x0000
0x1A	Conversion delay	2	R/W	0x0000
0x1B	T_{SENSE}x background enable	2	R/W	0x0000
0x1C	I_{SENSE}x background enable	2	R/W	0x0000
0x1D	I_{SENSE}x gain	2	R/W	0x0000
0x1F	DAC snooze/SLEEP0 pin	2	R/W	0xFF00
0x20	DAC snooze/SLEEP1 pin	2	R/W	0xFF00
0x23	RSx+$_{MON}$, supply monitor, BI-V_{OUT}x background enable	2	R/W	0x0000
0x28	Integrator limit and closed-loop control	2	R/W	0x0000
0x29	PA_ON control	2	R/W	0x0130
0x2A	Ramp Time 0	2	R/W	0x0000
0x2B	Ramp Time 1	2	R/W	0x0000
0x2C	Ramp Time 2	2	R/W	0x0000
0x2D	Ramp Time 3	2	R/W	0x0000
0x2E	Closed-loop fast ramp and integrator time constant	2	R/W	0xBBBB
0x2F	INT_{LIMITx} and AV_{SS}/ AV_{DD} alarm mask	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

Digital Output Enable Register (Register 0x11)

This 16-bit register enables the output drivers of the GPIO pins by setting the corresponding bit to one. When using one of the pins as an output in GPIO mode or functional mode (for alerts or busy), the corresponding bit must be set.

Digital Input/Output Function Register (Register 0x12)

All GPIOs are in either functional mode (power-up) or GPIO mode. The relevant GPIO pin is in GPIO mode when the corresponding bit in this register is set to 1. The relevant GPIO pin is in functional mode when the corresponding bit in this register is cleared to 0. Four pins are in functional mode and four pins are in GPIO mode after a power-on reset.

Digital Functional Polarity Register (Register 0x13)

This register sets the polarity of the digital input/output pins in functional mode only. The associated input/output signal can be made active low by setting the corresponding bit in this register to 1. Functional mode is set up in the digital input/output function register (Register 0x12).

General Register (Register 0x14)

This 16-bit register selects the internal ADC reference or an external reference and other general functions. The status on GPIO0 to GPIO3 can be routed to ALERT1. Error amplifier control over the integrator limit feature is also configurable in this register. ALERT0 can be routed internally to clamp the bipolar DACs.

V_{IN}x Range x Registers (Register 0x15 and Register 0x16)

These two 16-bit registers combine together to specify the input range of the V_{IN}x channels. The default range is $4 \times REF_{ADC}$. If either of the corresponding range bits from the two range registers is set to one, the analog input voltage range is set to $2 \times REF_{ADC}$. If both the bits are set to one, the analog input voltage range is REF_{ADC}. See Table 36 and Table 37 for range selection. REF_{ADC} = 1.25 V.

V_{IN}x Differential/Single-Ended Enable Register (Register 0x17)

This register runs the ADC conversions for the voltage input channels in differential and pseudo differential mode. The corresponding differential pairs for the channels are as follows: $V_{IN}0$ to $V_{IN}1$ for Channel 0, $V_{IN}1$ to $V_{IN}0$ for Channel 1, $V_{IN}2$ to $V_{IN}3$ for Channel 2, and $V_{IN}3$ to $V_{IN}2$ for Channel 3. The differential mode bits are ignored when the device is in pseudo differential mode.

V_{IN}x Filter Register (Register 0x18)

A digital filter can be applied to the conversion result of all four V_{IN}x channels. Set the corresponding filter bit to 1 to apply the digital filter.

V_{IN}x Background Enable Register (Register 0x19)

Set the corresponding enable bit to 1 to convert the V_{IN}x channels in the background.

Conversion Delay Register (Register 0x1A)

This register can add a conversion delay (during the acquisition phase) to the $V_{IN}x$ channels in command mode conversions. The resolution of this register is 320 ns. That is, each bit adds 320 ns to the conversion delay.

Temperature Sensor ($T_{SENSE}x$) Background Enable Register (Register 0x1B)

To enable the temperature sensor conversions, write to the corresponding bit from this register. To enable digital filtering, also write to the corresponding bit.

Current Sensor ($I_{SENSE}x$) Background Enable Register (Register 0x1C)

To enable the $I_{SENSE}x$ conversions, write to the corresponding bit from this register. To enable digital filtering, also write to the corresponding bit.

Current Sensor ($I_{SENSE}x$) Gain Register (Register 0x1D)

The $I_{SENSE}x$ gain register is a 16-bit register that controls the gain settings for the four current sense channels.

DAC Snooze/SLEEP0 Pin Register (Register 0x1F)

To clamp the relevant DAC output via the GPIO5/SLEEP0 pin set the corresponding bit in this register to 1. The snooze bits determine the power-up/power-down condition of the DACs after removing the clamp signal. If any of the snooze bits are set to 1, an additional write to the DAC enable register is required to wake up the corresponding DAC. If the snooze bits are not set, directly use the SLEEP0 pin to wake up the DAC.

DAC Snooze/SLEEP1 Pin Register (Register 0x20)

To clamp the relevant DAC output via the GPIO6/SLEEP1 pin, set the corresponding bit in this register to 1.

RSx+$_{MON}$, Supply Monitor, BI-$V_{OUT}x$ Background Enable Register (Register 0x23)

The $RSx+_{MON}$ and voltage supply channels can convert in the background by setting the corresponding enable bit to 1.

Integrator Limit and Closed-Loop Control Register (Register 0x28)

This register configures the device in closed-loop mode and controls the integrator limit function as described in the Closed-Loop Integrator Programmable Voltage Limit section.

PA_ON Control Register (Register 0x29)

This register controls the PA_ON pin and allows AVss/AV_{DD} alarm control over the PA_ON pin. Note that the AV_{SS}/AV_{DD} alarm must be cleared before the PA_ON pin can switch back to the on state.

This register also allows clamp pin control over the PA_ON pin. Setting the clamp bit to 1 allows control of the PA_ON pin via the SLEEP0 and SLEEP1 pins, where, if the pin goes high, the PA_ON pin goes to the off state. If the snooze bit is set to 1, an additional write to this register is required to set the PA_ON pin to the on state after clearing the corresponding SLEEP0 and SLEEP1 pins.

Ramp Time 0 to Ramp Time 3 Registers (Register 0x2A to Register 0x2D)

These 16-bit registers (Ramp Time 0 to Ramp Time 3) configure the ramp time for the closed-loop channels. The resolution of each bit is 250 µs and the maximum programmable ramp time is 31.75 ms.

The minimum programmable ramp time for each channel is 4 ms. Enter 0x0000 to disable the ramp circuitry and to have the DAC resolve the target value immediately.

Closed-Loop Fast Ramp and Integrator Time Constant Register (Register 0x2E)

Use this register to disable or to enable the fast ramp scheme for the closed-loop channels when they release from clamp. The integrator time constant can trim to the values shown in Table 50.

Integrator Limit Active Status ($INT_{LIMIT}x$) and AV_{SS}/AV_{DD} Alarm Mask Register (Register 0x2F)

Use this 16-bit register to mask any of the closed-loop integrator limit active status values or the AVss/AV_{DD} alarm. When masked, the status values are not visible when reading back the corresponding alert registers, or if the status values are routed to any of the ALERTx pins.

Table 32. Digital Output Enable Register (Register 0x11)

Bit Number(s)	Bit Name	Description
[D15:D8]	Reserved	Reserved
D7	GPIO7/LDAC (Pin 6)	1: enable output drivers. 0: disable output drivers.
D6	GPIO6/SLEEP1 (Pin 4)	1: enable output drivers. 0: disable output drivers.
D5	GPIO5/SLEEP0 (Pin 3)	1: enable output drivers. 0: disable output drivers.
D4	GPIO4/ALERT1 (Pin 2)	1: enable output drivers (default). 0: disable output drivers.
D3	GPIO3/ALERT0 (Pin 53)	1: enable output drivers. 0: disable output drivers.
D2	GPIO2/BUSY (Pin 54)	1: enable output drivers. 0: disable output drivers.
D1	GPIO1/CONVST (Pin 55)	1: enable output drivers. 0: disable output drivers.
D0	GPIO0/IS BLANK (Pin 56)	1: enable output drivers. 0: disable output drivers.

Table 33. Digital Input/Output Function Register (Register 0x12)

Bit Number(s)	Bit Name	Description
[D15:D8]	Reserved	Reserved
D7	Pin 6	0: LDAC (default) 1: GPIO7
D6	Pin 4	0: SLEEP1 (default) 1: GPIO6
D5	Pin 3	0: SLEEP0 (default) 1: GPIO5
D4	Pin 2	0: ALERT1 (default) 1: GPIO4
D3	Pin 53	0: ALERT0 1: GPIO3 (default)
D2	Pin 54	0: BUSY 1: GPIO2 (default)
D1	Pin 55	0: CONVST 1: GPIO1 (default)
D0	Pin 56	0: IS BLANK 1: GPIO0 (default)

Table 34. Digital Functional Polarity Register (Register 0x13)

Bit Number(s)	Bit Name	Description
[D15:D8]	Reserved	Reserved
D7	LDAC	0: LDAC is active high 1: LDAC is active low (default)
D6	SLEEP1	0: SLEEP1 is active high (default) 1: SLEEP1 is active low
D5	SLEEP0	0: SLEEP0 is active high (default) 1: SLEEP0 is active low
D4	ALERT1	0: ALERT1 is active high 1: ALERT1 is active low (default)
D3	ALERT0	0: ALERT0 is active high (default) 1: ALERT0 is active low
D2	BUSY	0: BUSY is active high (default) 1: BUSY is active low
D1	CONVST	0: CONVST is active high (default) 1: CONVST is active low
D0	IS BLANK	0: IS BLANK is active high (default) 1: IS BLANK is active low

Table 35. General Register (Register 0x14)

Bit Number(s)	Bit Name	Description
[D15:D8]	Reserved	Reserved
D7	ADC_REF	0: external reference (default) 1: internal reference
D6	GPIO ALERT1 routing	0: feature disabled (default) 1: GPIO0 to GPIO3 status routed to ALERT1 if configured as general-purpose input
[D5:D4]	MISO speed	00: maximum (default) 01: fast 10: slow 11: minimum

Bit Number(s)	Bit Name	Description
D3	T_{SENSE} diode check	0: external check on (default) 1: external check off
D2	Limit control	0: alert control over software limit feature (default) 1: alert and error amplifier control over software limit feature
D1	ALERT0 clamp	0: no control (default) 1: ALERT0 routed internally to clamp bipolar DACs
D0	Reserved	Reserved

Table 36. Voltage Input (V_{IN}x) Range 0 Voltage Input Range Register (Register 0x15)

Bit Number(s)	Bit Name	Description[1, 2]
[D15:D4]	Reserved	Reserved
D3	$V_{IN}3$ Range 0	Used in conjunction with $V_{IN}3$ Range 1 bit (see Table 37) to specify the input range of $V_{IN}3$
D2	$V_{IN}2$ Range 0	Used in conjunction with $V_{IN}2$ Range 1 bit (see Table 37) to specify the input range of $V_{IN}2$
D1	$V_{IN}1$ Range 0	Used in conjunction with $V_{IN}1$ Range 1 bit (see Table 37) to specify the input range of $V_{IN}1$
D0	$V_{IN}0$ Range 0	Used in conjunction with $V_{IN}0$ Range 1 bit (see Table 37) to specify the input range of $V_{IN}0$

[1] REF_{ADC} = 1.25 V.
[2] See Table 38 for bit descriptions.

Table 37. V_{IN}x Range 1 Voltage Input Range Register (Register 0x16)

Bit Number(s)	Bit Name	Description[1, 2]
[D15:D4]	Reserved	Reserved
D3	$V_{IN}3$ Range 1	Used in conjunction with $V_{IN}3$ Range 0 bit (see Table 36) to specify the input range of $V_{IN}3$
D2	$V_{IN}2$ Range 1	Used in conjunction with $V_{IN}2$ Range 0 bit (see Table 36) to specify the input range of $V_{IN}2$
D1	$V_{IN}1$ Range 1	Used in conjunction with $V_{IN}1$ Range 0 bit (see Table 36) to specify the input range of $V_{IN}1$
D0	$V_{IN}0$ Range 1	Used in conjunction with $V_{IN}0$ Range 0 bit (see Table 36) to specify the input range of $V_{IN}0$

[1] REF_{ADC} = 1.25 V.
[2] See Table 38 for bit descriptions.

Table 38. V_{IN}x Range 1 and V_{IN} Range 0 Bit Descriptions

V_{IN} Range 0, V_{IN}x[1] Range Bit	V_{IN} Range 1, V_{IN}x[1] Range Bit	V_{IN}x[1] Input Range Bit
0	0	$4 \times REF_{ADC}$ (default)
0	1	$2 \times REF_{ADC}$
1	0	$2 \times REF_{ADC}$
1	1	REF_{ADC}

[1] x = 3, 2, 1, or 0.

Table 39. V_{IN}x Differential/Single-Ended Enable Register (Register 0x17)

Bit Number(s)	Bit Name	Description
[D15:D10]	Reserved	Reserved
D9	$V_{IN}2\_V_{IN}3\_PDIFF$	$V_{IN}2$ and $V_{IN}3$ pseudo differential mode 0: disable (default) 1: enable
D8	$V_{IN}0\_V_{IN}1\_PDIFF$	$V_{IN}0$ and $V_{IN}1$ pseudo differential mode 0: disable (default) 1: enable
[D7:D2]	Reserved	Reserved
D1	$V_{IN}2\_V_{IN}3\_DIFF$	$V_{IN}2$ and $V_{IN}3$ differential mode 0: disable (default) 1: enable
D0	$V_{IN}0\_V_{IN}1\_DIFF$	$V_{IN}0$ and $V_{IN}1$ differential mode 0: disable (default) 1: enable

Table 40. V_{IN}x Filter Register (Register 0x18)

Bit Number(s)	Bit Name	Description
[D15:D4]	Reserved	Reserved
D3	V_{IN}3 filter	0: disable (default) 1: enable
D2	V_{IN}2 filter	0: disable (default) 1: enable
D1	V_{IN}1 filter	0: disable (default) 1: enable
D0	V_{IN}0 filter	0: disable (default) 1: enable

Table 41. V_{IN}x Background Enable Register (Register 0x19)

Bit Number(s)	Bit Name	Description
[D15:D4]	Reserved	Reserved
D3	V_{IN}3_BG_EN	0: disable background conversions (default) 1: enable background conversions
D2	V_{IN}2_BG_EN	0: disable background conversions (default) 1: enable background conversions
D1	V_{IN}1_BG_EN	0: disable background conversions (default) 1: enable background conversions
D0	V_{IN}0_BG_EN	0: disable background conversions (default) 1: enable background conversions

Table 42. Temperature Sensor (T_{SENSE}x) Background Enable Register (Register 0x1B)

Bit Number(s)	Bit Name	Description
[D15:D11]	Reserved	Reserved
D10	T_{SENSE}D1 filter	0: disable digital filtering (default) 1: enable digital filtering
D9	T_{SENSE}D0 filter	0: disable digital filtering (default) 1: enable digital filtering
D8	T_{SENSE}INT filter	0: disable digital filtering (default) 1: enable digital filtering
[D7:D3]	Reserved	Reserved
D2	T_{SENSE}D1_EN	0: disable background conversions (default) 1: enable background conversions
D1	T_{SENSE}D0_EN	0: disable background conversions (default) 1: enable background conversions
D0	T_{SENSE}INT_EN	0: disable background conversions (default) 1: enable background conversions

Table 43. Current Sensor (I_{SENSE}x) Background Enable Register (Register 0x1C)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	I_{SENSE}3 filter	0: disable digital filtering (default) 1: enable digital filtering
D10	I_{SENSE}2 filter	0: disable digital filtering (default) 1: enable digital filtering
D9	I_{SENSE}1 filter	0: disable digital filtering (default) 1: enable digital filtering
D8	I_{SENSE}0 filter	0: disable digital filtering (default) 1: enable digital filtering

Bit Number(s)	Bit Name	Description
[D7:D4]	Reserved	Reserved
D3	$I_{SENSE}3$_EN	0: disable background conversions (default) 1: enable background conversions
D2	$I_{SENSE}2$_EN	0: disable background conversions (default) 1: enable background conversions
D1	$I_{SENSE}1$_EN	0: disable background conversions (default) 1: enable background conversions
D0	$I_{SENSE}0$_EN	0: disable background conversions (default) 1: enable background conversions

Table 44. I_{SENSE}x Gain Register (Register 0x1D)

Bit Number(s)	Bit Name	Description		
[D15:D12], [D11:D8], [D7:D4], [D3:D0]	$I_{SENSE}3$ gain, $I_{SENSE}2$ gain, $I_{SENSE}1$ gain, $I_{SENSE}0$ gain	These bits control the gain settings for the four current sense channels.		
		Code	**Gain Value**	**Voltage Across R_{SENSE} (mV)**
		0000 (default)	6.25	±200
		0001	12.5	±100
		0010	18.75	±66.67
		0011	25	±50
		0100	37.5	±33.33
		0101	50	±25
		0110	75	±16.67
		0111	100	±12.5
		1000	200	±6.25
		1001	400	±3.125
		1010	781.25	±1.6
		Others	6.25	±200

Table 45. DAC Snooze/SLEEP0 Pin Register (Register 0x1F) and DAC Snooze/SLEEP1 Pin Register (Register 0x20)

Bit Number(s)	Bit Name	Description
D15	BI-$V_{OUT}3$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D14	BI-$V_{OUT}2$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D13	BI-$V_{OUT}1$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D12	BI-$V_{OUT}0$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D11	UNI-$V_{OUT}3$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by SLEEP1 pin (Register 0x20) (default)
D10	UNI-$V_{OUT}2$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D9	UNI-$V_{OUT}1$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D8	UNI-$V_{OUT}0$ snooze	0: no control 1: snooze enabled when clamped by the SLEEP0 pin (Register 0x1F) or by the SLEEP1 pin (Register 0x20) (default)
D7	BI-$V_{OUT}3$ sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D6	BI-$V_{OUT}2$ sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D5	BI-$V_{OUT}1$ sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)

Bit Number(s)	Bit Name	Description
D4	BI-V_{OUT}0 sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D3	UNI-V_{OUT}3 sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D2	UNI-V_{OUT}2 sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D1	UNI-V_{OUT}1 sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)
D0	UNI-V_{OUT}0 sleep	0: no control (default) 1: can be clamped by the SLEEP0 pin (Register 0x1F) or clamped by the SLEEP1 pin (Register 0x20)

Table 46. RSx+$_{MON}$, Supply Monitor, BI-V_{OUT}x Background Enable Register (Register 0x23)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	RS3+$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D10	RS2+$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D9	RS1+$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D8	RS0+$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D7	BI-V_{OUT}3$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D6	BI-V_{OUT}2$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D5	BI-V_{OUT}1$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D4	BI-V_{OUT}0$_{MON}$	0: disable background conversions (default) 1: enable background conversions
D3	AV_{SS}	0: disable background conversions (default) 1: enable background conversions
D2	$DACV_{DD-BI}$	0: disable background conversions (default) 1: enable background conversions
D1	$DACV_{DD-UNI}$	0: disable background conversions (default) 1: enable background conversions
D0	AV_{DD}	0: disable background conversions (default) 1: enable background conversions

Table 47. Integrator Limit and Closed-Loop (CL) Control Register (Register 0x28)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	INT_CL_LIMIT_CH3	0: no control (default) 1: the soft closed-loop limit for the channel is enabled
D10	INT_CL_LIMIT_CH2	0: no control (default) 1: the soft closed-loop limit for the channel is enabled
D9	INT_CL_LIMIT_CH1	0: no control (default) 1: the soft closed-loop limit for the channel is enabled
D8	INT_CL_LIMIT_CH0	0: no control (default) 1: the soft closed-loop limit for the channel is enabled
[D7:D4]	Reserved	Reserved

Bit Number(s)	Bit Name	Description
D3	Closed-Loop 3	0: closed loop is disabled (default) 1: closed loop is enabled
D2	Closed-Loop 2	0: closed loop is disabled (default) 1: closed loop is enabled
D1	Closed-Loop 1	0: closed loop is disabled (default) 1: closed loop is enabled
D0	Closed-Loop 0	0: closed loop is disabled (default) 1: closed loop is enabled

Table 48. PA_ON Control Register (Register 0x29)

Bit Number(s)	Bit Name	Description
[D15:D10]	Reserved	Reserved
D9	PA_ON enable	0: PA_ON signal is in the off state (default) 1: PA_ON signal is in the on state
D8	PA_ON trigger	0: no control 1: AV_{SS}/AV_{DD} alarm or ALERT0 triggers PA_ON (default)
[D7:D6]	Reserved	Reserved
D5	SLEEP1 snooze	0: no control 1: PA_ON snooze after SLEEP1 enable (default)
D4	SLEEP0 snooze	0: no control 1: PA_ON snooze after SLEEP0 enable (default)
[D3:D2]	Reserved	Reserved
D1	PA_ON SLEEP1	0: no control (default) 1: PA_ON controlled by the SLEEP1 pin
D0	PA_ON SLEEP0	0: no control (default) 1: PA_ON controlled by the SLEEP0 pin

Table 49. Ramp Time 0 to Ramp Time 3 Registers (Register 0x2A to Register 0x2D)

Bit Number(s)	Bit Name	Description
[D15:D7]	Reserved	Reserved
[D6:D0]	B6 to B0	Ramp time bits configure the ramp time for the DACs in closed-loop mode 0000000 = no ramp function (default) 0000001 to 0010000 = 4 ms 0010001 = 4.25 ms … 1111110 = 31.5 ms 1111111 = 31.75 ms

Table 50. Closed-Loop Fast Ramp and Integrator Time Constant Register (Register 0x2E)

Bit Number(s)	Bit Name	Description
D15	CL3_FR	0: Closed-Loop 3 fast ramp disable 1: Closed-Loop 3 fast ramp enable (default)
[D14:D12]	CL3_CAP_TRIM[2:0]	000: not applicable 001: 2.352 ms 010: 1.218 ms 011: 840 µs (default) 100: 650 µs 101: 538 µs 110: 462 µs 111: 408 µs

Bit Number(s)	Bit Name	Description
D11	CL2_FR	0: Closed-Loop 2 fast ramp disable 1: Closed-Loop 2 fast ramp enable (default)
[D10:D8]	CL2_CAP_TRIM[2:0]	000: not applicable 001: 2.352 ms 010: 1.218 ms 011: 840 µs (default) 100: 650 µs 101: 538 µs 110: 462 µs 111: 408 µs
D7	CL1_FR	0: Closed-Loop 1 fast ramp disable 1: Closed-Loop 1 fast ramp enable (default)
[D6:D4]	CL1_CAP_TRIM[2:0]	000: not applicable 001: 2.352 ms 010: 1.218 ms 011: 840 µs (default) 100: 650 µs 101: 538 µs 110: 462 µs 111: 408 µs
D3	CL0_FR	0: Closed-Loop 0 fast ramp disable 1: Closed-Loop 0 fast ramp enable (default)
[D2:D0]	CL0_CAP_TRIM[2:0]	000: not applicable 001: 2.352 ms 010: 1.218 ms 011: 840 µs (default) 100: 650 µs 101: 538 µs 110: 462 µs 111: 408 µs

Table 51. Integrator Limit Active Status ($INT_{LIMIT}x$) and AV_{SS}/AV_{DD} Alarm Mask Register (Register 0x2F)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	$INT_{LIMIT}3$	0: no masking (default) 1: masks alerts such that they are not visible when reading back the corresponding alert registers and/or if routed to ALERTx pins
D10	$INT_{LIMIT}2$	0: no masking (default) 1: masks alerts such that they are not visible when reading back the corresponding alert registers and/or if routed to ALERTx pins
D9	$INT_{LIMIT}1$	0: no masking (default) 1: masks alerts such that they are not visible when reading back the corresponding alert registers and/or if routed to ALERTx pins
D8	$INT_{LIMIT}0$	0: no masking (default) 1: masks alerts such that they are not visible when reading back the corresponding alert registers and/or if routed to ALERTx pins
[D7:D1]	Reserved	Reserved
D0	AV_{SS}/AV_{DD} alarm	0: no masking (default) 1: masks alert

SEQUENCE (PAGE 0x03)

The sequence page contains registers that allow the user to sequence and read back the conversions results from selected channels in command mode.

Table 52. Sequence (Page 0x03)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}x sequence	2	R/W	0x0000
0x11	I_{SENSE}x and T_{SENSE}x sequence	2	R/W	0x0000
0x12	RSx+$_{MON}$, supply monitor, and BI-V_{OUT}x monitor sequence	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

Voltage Input (V_{IN}x) Sequence Register (Register 0x10)

This 16-bit register allows the user to sequence the ADC conversions for the four input channels in command mode.

Current Sensor (I_{SENSE}x) and Temperature Sensor (T_{SENSE}x) Sequence Register (Register 0x11)

This 16-bit register allows the user to sequence the results read back for the four current sense and three temperature sensor channels. The range for the current sense and temperature sense channels is fixed at 0 V to REF_{ADC} (1.25 V). However, the corresponding bit from the enable registers on the configuration page must be set to run a conversion for a temperature sensor or current sensor channel in command mode.

RSx+$_{MON}$, Supply Monitor, and BI-V_{OUT}x Monitor Sequence Register (Register 0x12)

This 16-bit register allows the user to sequence and read back the ADC conversion results for the four RSx+ pins, four voltage supplies, and the four DAC monitor channels in command mode.

Table 53. V_{IN}x Sequence Register (Register 0x10)

Bit Number(s)	Bit Name	Description
[D15:D4]	Reserved	Reserved
D3	V_{IN}3	1: command mode sequencing enabled 0: command mode sequencing disabled (default)
D2	V_{IN}2	1: command mode sequencing enabled 0: command mode sequencing disabled (default)
D1	V_{IN}1	1: command mode sequencing enabled 0: command mode sequencing disabled (default)
D0	V_{IN}0	1: command mode sequencing enabled 0: command mode sequencing disabled (default)

Table 54. I_{SENSE}x and T_{SENSE}x Sequence Register (Register 0x11)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	I_{SENSE}3	0: no control (default) 1: command mode sequencing enabled
D10	I_{SENSE}2	0: no control (default) 1: command mode sequencing enabled
D9	I_{SENSE}1	0: no control (default) 1: command mode sequencing enabled
D8	I_{SENSE}0	0: no control (default) 1: command mode sequencing enabled
[D7:D3]	Reserved	Reserved
D2	T_{SENSE}D1	0: no control (default) 1: command mode sequencing enabled
D1	T_{SENSE}D0	0: no control (default) 1: command mode sequencing enabled
D0	T_{SENSE}INT	0: no control (default) 1: command mode sequencing enabled

Table 55. RSx+$_{MON}$, Supply Monitor, and BI-V$_{OUT}$x Monitor Sequence Register (Register 0x12)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	RS3+$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D10	RS2+$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D9	RS1+$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D8	RS0+$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D7	BI-V$_{OUT}$3$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D6	BI-V$_{OUT}$2$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D5	BI-V$_{OUT}$1$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D4	BI-V$_{OUT}$0$_{MON}$	0: no control (default) 1: command mode sequencing enabled
D3	AV$_{SS}$	0: no control (default) 1: command mode sequencing enabled
D2	DACV$_{DD-BI}$	0: no control (default) 1: command mode sequencing enabled
D1	DACV$_{DD-UNI}$	0: no control (default) 1: command mode sequencing enabled
D0	AV$_{DD}$	0: no control (default) 1: command mode sequencing enabled

HIGH LIMIT 0 (PAGE 0x04)

Table 56. High Limit 0 (Page 0x04)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 high limit	2	R/W	0xFFF0
0x11	V_{IN}1 high limit	2	R/W	0xFFF0
0x12	V_{IN}2 high limit	2	R/W	0xFFF0
0x13	V_{IN}3 high limit	2	R/W	0xFFF0
0x20	T_{SENSE}INT high limit	2	R/W	0xFFF0
0x21	T_{SENSE}D0 high limit	2	R/W	0xFFF0
0x22	T_{SENSE}D1 high limit	2	R/W	0xFFF0
0x28	I_{SENSE}0 high limit	2	R/W	0xFFF0
0x29	I_{SENSE}1 high limit	2	R/W	0xFFF0
0x2A	I_{SENSE}2 high limit	2	R/W	0xFFF0
0x2B	I_{SENSE}3 high limit	2	R/W	0xFFF0

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x High Limit Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the high limits for the four input channels. The default value of these registers is 0xFFF0.

Temperature Sensor (T_{SENSE}x) High Limit Registers (Register 0x20 to Register 0x22)

These read/write 16-bit registers set the high limits for the three temperature sensor channels. The default value of these registers is 0xFFF0.

Table 57. Temperature Sensor High Limit Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D15	B11	0: −256°C 1: 0°C (default)
D14	B10	0: 0°C 1: 128°C (default)
D13	B9	0: 0°C 1: 64°C (default)
D12	B8	0: 0°C 1: 32°C (default)
D11	B7	0: 0°C 1: 16°C (default)
D10	B6	0: 0°C 1: 8°C (default)
D9	B5	0: 0°C 1: 4°C (default)
D8	B4	0: 0°C 1: 2°C (default)
D7	B3	0: 0°C 1: 1°C (default)
D6	B2	0: 0°C 1: 0.5°C (default)
D5	B1	0: 0°C 1: 0.25°C (default)
D4	B0	0: 0°C 1: 0.125°C (default)
[D3:D0]	Reserved	Reserved

Current Sensor (I_{SENSE}x) High Limit Registers (Register 0x28 to Register 0x2B)

These read/write 16-bit registers set the high limits for the four current sensor channels. The default value of these registers is 0xFFF0.

Table 58. V_{IN}x (Register 0x10 to Register 0x13) and I_{SENSE}x High Limit Registers (Register 0x28 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

HIGH LIMIT 1 (PAGE 0x05)

Table 59. High Limit 1 (Page 0x05)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} high limit	2	R/W	0xFFF0
0x11	$DACV_{DD-UNI}$ high limit	2	R/W	0xFFF0
0x12	$DACV_{DD-BI}$ high limit	2	R/W	0xFFF0
0x13	AV_{SS} high limit	2	R/W	0xFFF0
0x14	$BI\text{-}V_{OUT}0_{MON}$ high limit	2	R/W	0xFFF0
0x15	$BI\text{-}V_{OUT}1_{MON}$ high limit	2	R/W	0xFFF0
0x16	$BI\text{-}V_{OUT}2_{MON}$ high limit	2	R/W	0xFFF0
0x17	$BI\text{-}V_{OUT}3_{MON}$ high limit	2	R/W	0xFFF0
0x28	$RS0+_{MON}$ high limit	2	R/W	0xFFF0
0x29	$RS1+_{MON}$ high limit	2	R/W	0xFFF0
0x2A	$RS2+_{MON}$	2	R/W	0xFFF0
0x2B	$RS3+_{MON}$	2	R/W	0xFFF0

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$) and AV_{SS} High Limit Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the high limits for the four voltage supply conversions. The default value of these registers is 0xFFF0.

$BI\text{-}V_{OUT}0_{MON}$ to $BI\text{-}V_{OUT}3_{MON}$ High Limit Registers (Register 0x14 to Register 0x17)

These registers store the high limits for the four internal inputs for monitoring the bipolar DAC outputs in open-loop mode or the integrator outputs in closed-loop mode.

$RSx+_{MON}$ High Limit Registers (Register 0x28 to Register 0x2B)

These registers store the high limits for the $RSx+_{MON}$ monitoring channels.

Table 60. AV_{DD}, DAC Supply, AV_{SS}, $BI\text{-}V_{OUT}x_{MON}$, and $RSx+_{MON}$ High Limit Registers (Register 0x10 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

LOW LIMIT 0 (PAGE 0x06)

Table 61. Low Limit 0 (Page 0x06)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 low limit	2	R/W	0x0000
0x11	V_{IN}1 low limit	2	R/W	0x0000
0x12	V_{IN}2 low limit	2	R/W	0x0000
0x13	V_{IN}3 low limit	2	R/W	0x0000
0x20	T_{SENSE}INT low limit	2	R/W	0x0000
0x21	T_{SENSE}D0 low limit	2	R/W	0x0000
0x22	T_{SENSE}D1 low limit	2	R/W	0x0000
0x28	I_{SENSE}0 low limit	2	R/W	0x0000
0x29	I_{SENSE}1 low limit	2	R/W	0x0000
0x2A	I_{SENSE}2 low limit	2	R/W	0x0000
0x2B	I_{SENSE}3 low limit	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x Low Limit Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the low limits for the four input channels.

Temperature Sensor (T_{SENSE}x) Low Limit Registers (Register 0x20 to Register 0x22)

These read/write 16-bit registers set the low limits for the three temperature sensor channels.

Table 62. Temperature Sensor Low Limit Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D15	B11	0: −256°C (default) 1: 0°C
D14	B10	0: 0°C (default) 1: 128°C
D13	B9	0: 0°C (default) 1: 64°C
D12	B8	0: 0°C (default) 1: 32°C
D11	B7	0: 0°C (default) 1: 16°C
D10	B6	0: 0°C (default) 1: 8°C
D9	B5	0: 0°C (default) 1: 4°C
D8	B4	0: 0°C (default) 1: 2°C
D7	B3	0: 0°C (default) 1: 1°C
D6	B2	0: 0°C (default) 1: 0.5°C
D5	B1	0: 0°C (default) 1: 0.25°C
D4	B0	0: 0°C (default) 1: 0.125°C
[D3:D0]	Reserved	Reserved

Current Sensor (I_{SENSE}x) Low Limit Registers (Register 0x28 to Register 0x2B)

These read/write 16-bit registers set the low limits for the four current sensor channels.

Table 63. V_{IN}x and Current Sensor Low Limit Registers (Register 0x10 to Register 0x13, and Register 0x28 to Register 0x2B)

MSB												LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**[D3:D0]**
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

LOW LIMIT 1 (PAGE 0x07)

Table 64. Low Limit 1 (Page 0x07)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} low limit	2	R/W	0x0000
0x11	$DACV_{DD-UNI}$ low limit	2	R/W	0x0000
0x12	$DACV_{DD-BI}$ low limit	2	R/W	0x0000
0x13	AV_{SS} low limit	2	R/W	0x0000
0x14	BI-$V_{OUT}0_{MON}$ low limit	2	R/W	0x0000
0x15	BI-$V_{OUT}1_{MON}$ low limit	2	R/W	0x0000
0x16	BI-$V_{OUT}2_{MON}$ low limit	2	R/W	0x0000
0x17	BI-$V_{OUT}3_{MON}$ low limit	2	R/W	0x0000
0x28	RS0+$_{MON}$ low limit	2	R/W	0x0000
0x29	RS1+$_{MON}$ low limit	2	R/W	0x0000
0x2A	RS2+$_{MON}$ low limit	2	R/W	0x0000
0x2B	RS3+$_{MON}$ low limit	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$), and AV_{SS} Low Limit Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the low limits for the four supply channels.

BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$ Low Limit Registers (Register 0x14 to Register 0x17)

These registers store the low limits from the four internal inputs for monitoring the bipolar DAC outputs, although the intention is to monitor the bipolar DAC outputs in open-loop mode or the integrator outputs in closed-loop mode.

RSx+$_{MON}$ Low Limit Registers (Register 0x28 to Register 0x2B)

These registers store the low limits for the RSx+$_{MON}$ monitoring channels.

Table 65. AV_{DD}, DAC Supply, AV_{SS}, BI-$V_{OUT}x_{MON}$, and RSx+$_{MON}$ Low Limit Registers (Register 0x10 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

HYSTERESIS 0 (PAGE 0x08)

Table 66. Hysteresis 0 (Page 0x08)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 hysteresis	2	R/W	0x0000
0x11	V_{IN}1 hysteresis	2	R/W	0x0000
0x12	V_{IN}2 hysteresis	2	R/W	0x0000
0x13	V_{IN}3 hysteresis	2	R/W	0x0000
0x20	T_{SENSE}INT hysteresis	2	R/W	0x0000
0x21	T_{SENSE}D0 hysteresis	2	R/W	0x0000
0x22	T_{SENSE}D1 hysteresis	2	R/W	0x0000
0x28	I_{SENSE}0 hysteresis	2	R/W	0x0000
0x29	I_{SENSE}1 hysteresis	2	R/W	0x0000
0x2A	I_{SENSE}2 hysteresis	2	R/W	0x0000
0x2B	I_{SENSE}3 hysteresis	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x Hysteresis Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the hysteresis values for the four input channels.

Temperature Sensor (T_{SENSE}x) Hysteresis Registers (Register 0x20 to Register 0x22)

These read/write 16-bit registers set the hysteresis values for the three temperature sensor channels. The MSB of this register must be set to 1.

Table 67. Temperature Sensor Hysteresis Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D15	Reserved	Reserved. Must be set to 1.
D14	B10	0: 0°C (default) 1: 128°C
D13	B9	0: 0°C (default) 1: 64°C
D12	B8	0: 0°C (default) 1: 32°C
D11	B7	0: 0°C (default) 1: 16°C
D10	B6	0: 0°C (default) 1: 8°C
D9	B5	0: 0°C (default) 1: 4°C
D8	B4	0: 0°C (default) 1: 2°C
D7	B3	0: 0°C (default) 1: 1°C
D6	B2	0: 0°C (default) 1: 0.5°C
D5	B1	0: 0°C (default) 1: 0.25°C
D4	B0	0: 0°C (default) 1: 0.125°C
[D3:D0]	Reserved	Reserved

Current Sensor (I_{SENSE}x) Hysteresis Registers (Register 0x28 to Register 0x2B)

These read/write 16-bit registers set the hysteresis values for the four current sensor channels.

Table 68. V_{IN}x and Current Sensor Hysteresis Registers (Register 0x10 to Register 0x13, and Register 0x28 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

HYSTERESIS 1 (PAGE 0x09)

Table 69. Hysteresis 1 (Page 0x09)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} hysteresis	2	R/W	0x0000
0x11	$DACV_{DD-UNI}$ hysteresis	2	R/W	0x0000
0x12	$DACV_{DD-BI}$ hysteresis	2	R/W	0x0000
0x13	AV_{SS} hysteresis	2	R/W	0x0000
0x14	BI-$V_{OUT}0_{MON}$ hysteresis	2	R/W	0x0000
0x15	BI-$V_{OUT}1_{MON}$ hysteresis	2	R/W	0x0000
0x16	BI-$V_{OUT}2_{MON}$ hysteresis	2	R/W	0x0000
0x17	BI-$V_{OUT}3_{MON}$ hysteresis	2	R/W	0x0000
0x28	RS0+$_{MON}$ hysteresis	2	R/W	0x0000
0x29	RS1+$_{MON}$ hysteresis	2	R/W	0x0000
0x2A	RS2+$_{MON}$ hysteresis	2	R/W	0x0000
0x2B	RS3+$_{MON}$ hysteresis	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$), and AV_{SS} Hysteresis Registers (Register 0x10 to Register 0x13)

These read/write 16-bit registers set the hysteresis values for the four supply voltage conversions.

BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$ Hysteresis Registers (Register 0x14 to Register 0x17)

These read/write 16-bit registers set the hysteresis values for the four DAC monitoring conversions.

RSx+$_{MON}$ Hysteresis Registers (Register 0x28 to Register 0x2B)

These read/write 16-bit registers set the hysteresis values for the four RSx+ conversions.

Table 70. AV_{DD}, DAC Supply, AV_{SS}, BI-$V_{OUT}x_{MON}$, and RSx+$_{MON}$ Hysteresis Registers (Register 0x10 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

MINIMUM 0 (PAGE 0x0A)

Table 71. Minimum 0 (Page 0x0A)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 minimum	2	R/W	0xFFF0
0x11	V_{IN}1 minimum	2	R/W	0xFFF0
0x12	V_{IN}2 minimum	2	R/W	0xFFF0
0x13	V_{IN}3 minimum	2	R/W	0xFFF0
0x20	T_{SENSE}INT minimum	2	R/W	0xFFF0
0x21	T_{SENSE}D0 minimum	2	R/W	0xFFF0
0x22	T_{SENSE}D1 minimum	2	R/W	0xFFF0
0x28	I_{SENSE}0 minimum	2	R/W	0xFFF0
0x29	I_{SENSE}1 minimum	2	R/W	0xFFF0
0x2A	I_{SENSE}2 minimum	2	R/W	0xFFF0
0x2B	I_{SENSE}3 minimum	2	R/W	0xFFF0

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x Minimum Registers (Register 0x10 to Register 0x13)

These 16-bit registers store the minimum ADC conversion results for the relevant input channel. The default value of these registers is 0xFFF0. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Temperature Sensor (T_{SENSE}x) Minimum Registers (Register 0x20 to Register 0x22)

These 16-bit registers store the minimum ADC conversion results for the relevant temperature sensor channel. The default value of these registers is 0xFFF0. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Table 72. Temperature Sensor Minimum Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D15	B11	0: −256°C 1: 0°C
D14	B10	0: 0°C 1: 128°C
D13	B9	0: 0°C 1: 64°C
D12	B8	0: 0°C 1: 32°C
D11	B7	0: 0°C 1: 16°C
D10	B6	0: 0°C 1: 8°C
D9	B5	0: 0°C 1: 4°C
D8	B4	0: 0°C 1: 2°C
D7	B3	0: 0°C 1: 1°C
D6	B2	0: 0°C 1: 0.5°C
D5	B1	0: 0°C 1: 0.25°C
D4	B0	0: 0°C 1: 0.125°C
[D3:D0]	Reserved	Reserved

Current Sensor (I_{SENSE}x) Minimum Registers (Register 0x28 to Register 0x2B)

These 16-bit registers store the minimum ADC conversion results for the relevant current sensor channel. The default value of these registers is 0xFFF0. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Table 73. V_{IN}x and Current Sensor Minimum Registers (Register 0x10 to Register 0x13, and Register 0x28 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

MINIMUM 1 (PAGE 0x0B)

Table 74. Minimum 1 (Page 0x0B)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} minimum	2	R/W	0xFFF0
0x11	$DACV_{DD-UNI}$ minimum	2	R/W	0xFFF0
0x12	$DACV_{DD-BI}$ minimum	2	R/W	0xFFF0
0x13	AV_{SS} minimum	2	R/W	0xFFF0
0x14	BI-$V_{OUT}0_{MON}$ minimum	2	R/W	0xFFF0
0x15	BI-$V_{OUT}1_{MON}$ minimum	2	R/W	0xFFF0
0x16	BI-$V_{OUT}2_{MON}$ minimum	2	R/W	0xFFF0
0x17	BI-$V_{OUT}3_{MON}$ minimum	2	R/W	0xFFF0
0x28	RS0+$_{MON}$ minimum	2	R/W	0xFFF0
0x29	RS1+$_{MON}$ minimum	2	R/W	0xFFF0
0x2A	RS2+$_{MON}$ minimum	2	R/W	0xFFF0
0x2B	RS3+$_{MON}$ minimum	2	R/W	0xFFF0

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$), and AV_{SS} Minimum Registers (Register 0x10 to Register 0x13)

These 16-bit registers store the minimum ADC conversion results for the relevant channels. These registers can be set back to their default value by writing to them.

BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$ Minimum Registers (Register 0x14 to Register 0x17)

These 16-bit registers store the minimum ADC conversion results for the relevant DAC monitoring channels. These registers can be set back to their default value by writing to them.

RSx+$_{MON}$ Minimum Registers (Register 0x28 to Register 0x2B)

These 16-bit registers store the minimum ADC conversion results for the relevant channels. These registers can be set back to their default value by writing to them.

Table 75. AV_{DD}, DAC Supply, AV_{SS}, BI-$V_{OUT}x_{MON}$, and RSx+$_{MON}$ Minimum Registers (Register 0x10 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

MAXIMUM 0 (PAGE 0x0C)

Table 76. Maximum 0 (Page 0x0C)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 maximum	2	R/W	0x0000
0x11	V_{IN}1 maximum	2	R/W	0x0000
0x12	V_{IN}2 maximum	2	R/W	0x0000
0x13	V_{IN}3 maximum	2	R/W	0x0000
0x20	T_{SENSE}INT maximum	2	R/W	0x0000
0x21	T_{SENSE}D0 maximum	2	R/W	0x0000
0x22	T_{SENSE}D1 maximum	2	R/W	0x0000
0x28	I_{SENSE}0 maximum	2	R/W	0x0000
0x29	I_{SENSE}1 maximum	2	R/W	0x0000
0x2A	I_{SENSE}2 maximum	2	R/W	0x0000
0x2B	I_{SENSE}3 maximum	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x Maximum Registers (Register 0x10 to Register 0x13)

These 16-bit registers store the maximum ADC conversion results for the relevant input channel. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Temperature Sensor (T_{SENSE}x) Maximum Registers (Register 0x20 to Register 0x22)

These 16-bit registers store the maximum ADC conversion results for the relevant temperature sensor channel. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Table 77. Temperature Sensor Maximum Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D15	B11	0: −256°C 1: 0°C
D14	B10	0: 0°C 1: 128°C
D13	B9	0: 0°C 1: 64°C
D12	B8	0: 0°C 1: 32°C
D11	B7	0: 0°C 1: 16°C
D10	B6	0: 0°C 1: 8°C
D9	B5	0: 0°C 1: 4°C
D8	B4	0: 0°C 1: 2°C
D7	B3	0: 0°C 1: 1°C
D6	B2	0: 0°C 1: 0.5°C
D5	B1	0: 0°C 1: 0.25°C
D4	B0	0: 0°C 1: 0.125°C
[D3:D0]	Reserved	Reserved

Current Sensor (I_{SENSE}x) Maximum Registers (Register 0x28 to Register 0x2B)

These 16-bit registers store the maximum ADC conversion results for the relevant current sensor channel. These registers can be set back to their default value by writing to them (the 12-bit write value is not written to these registers).

Table 78. V_{IN}x and Current Sensor Maximum Registers (Register 0x10 to Register 0x13, and Register 0x28 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

MAXIMUM 1 (PAGE 0x0D)

Table 79. Maximum 1 (Page 0x0D)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} maximum	2	R/W	0x0000
0x11	$DACV_{DD-UNI}$ maximum	2	R/W	0x0000
0x12	$DACV_{DD-BI}$ maximum	2	R/W	0x0000
0x13	AV_{SS} maximum	2	R/W	0x0000
0x14	$BI\text{-}V_{OUT}0_{MON}$ maximum	2	R/W	0x0000
0x15	$BI\text{-}V_{OUT}1_{MON}$ maximum	2	R/W	0x0000
0x16	$BI\text{-}V_{OUT}2_{MON}$ maximum	2	R/W	0x0000
0x17	$BI\text{-}V_{OUT}3_{MON}$ maximum	2	R/W	0x0000
0x28	$RS0+_{MON}$ maximum	2	R/W	0x0000
0x29	$RS1+_{MON}$ maximum	2	R/W	0x0000
0x2A	$RS2+_{MON}$ maximum	2	R/W	0x0000
0x2B	$RS3+_{MON}$ maximum	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$), and AV_{SS} Maximum Registers (Register 0x10 to Register 0x13)

These 16-bit registers store the maximum ADC conversion results for the relevant channels.

$BI\text{-}V_{OUT}0_{MON}$ to $BI\text{-}V_{OUT}3_{MON}$ Maximum Registers (Register 0x14 to Register 0x17)

These 16-bit registers store the maximum ADC conversion results for the relevant DAC monitoring channels. These registers can be set back to their default value by writing to them.

$RSx+_{MON}$ Maximum Registers (Register 0x28 to Register 0x2B)

These 16-bit registers store the maximum ADC conversion results for the relevant channels. These registers can be set back to their default value by writing to them.

Table 80. AV_{DD}, DAC Supply, AV_{SS}, $BI\text{-}V_{OUT}x_{MON}$,and $RSx+_{MON}$ Maximum Registers (Register 0x10 to Register 0x2B)

MSB												LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	[D3:D0]
B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Reserved

OFFSET 0 (PAGE 0x0E)

Table 81. Offset 0 (Page 0x0E)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	V_{IN}0 offset	2	R/W	0x0000
0x11	V_{IN}1 offset	2	R/W	0x0000
0x12	V_{IN}2 offset	2	R/W	0x0000
0x13	V_{IN}3 offset	2	R/W	0x0000
0x20	T_{SENSE}INT offset	2	R/W	0x0000
0x21	T_{SENSE}D0 offset	2	R/W	0x0000
0x22	T_{SENSE}D1 offset	2	R/W	0x0000
0x28	I_{SENSE}0 offset	2	R/W	0x0000
0x29	I_{SENSE}1 offset	2	R/W	0x0000
0x2A	I_{SENSE}2 offset	2	R/W	0x0000
0x2B	I_{SENSE}3 offset	2	R/W	0x0000
0x30	UNI-V_{OUT}0 offset	2	R/W	0x0000
0x31	UNI-V_{OUT}1 offset	2	R/W	0x0000
0x32	UNI-V_{OUT}2 offset	2	R/W	0x0000
0x33	UNI-V_{OUT}3 offset	2	R/W	0x0000
0x34	BI-V_{OUT}0 offset	2	R/W	0x0000
0x35	BI-V_{OUT}1 offset	2	R/W	0x0000
0x36	BI-V_{OUT}2 offset	2	R/W	0x0000
0x37	BI-V_{OUT}3 offset	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x Offset Registers (Register 0x10 to Register 0x13)

These read/write 8-bit registers store the offset values for the relevant input channel.

Temperature Sensor (T_{SENSE}x) Offset Registers (Register 0x20 to Register 0x22)

These read/write 8-bit registers store the offset values for the relevant temperature sensor channel.

Current Sensor (I_{SENSE}x) Offset Registers (Register 0x28 to Register 0x2B)

These read/write 8-bit registers store the offset values for the relevant current sensor channel.

Unipolar DAC (UNI-V_{OUT}x) Offset Registers (Register 0x30 to Register 0x33)

These read/write registers store the offset values for the corresponding DAC output. If the copy bit is set to 1, writing to any of the DAC offset registers sets all the other unipolar DAC offset registers to the same value.

Bipolar DAC (BI-V_{OUT}x) Offset Registers (Register 0x34 to Register 0x37)

These read/write registers store the offset values for the corresponding DAC output. If the copy bit is set to 1, writing to any of the DAC offset registers sets all the other bipolar DAC offset registers to the same value. Any write to these registers affects the DAC range in open-loop mode and the integrator limit in closed-loop mode.

Table 82. V_{IN}x and Current Sensor Offset Registers (Register 0x10 to Register 0x13, and Register 0x28 to Register 0x2B)

Bit Number(s)	Bit Name	Description
D7	B7	0: 0 LSB (default) 1: −128 LSB
D6	B6	0: 0 LSB (default) 1: 64 LSB
D5	B5	0: 0 LSB (default) 1: 32 LSB
D4	B4	0: 0 LSB (default) 1: 16 LSB
D3	B3	0: 0 LSB (default) 1: 8 LSB
D2	B2	0: 0 LSB (default) 1: 4 LSB
D1	B1	0: 0 LSB (default) 1: 2 LSB
D0	B0	0: 0 LSB (default) 1: 1 LSB

Table 83. Temperature Sensor Offset Registers (Register 0x20 to Register 0x22)

Bit Number(s)	Bit Name	Description
D7	B7	0: 0°C (default) 1: −16°C
D6	B6	0: 0°C (default) 1: 8°C
D5	B5	0: 0°C (default) 1: 4°C
D4	B4	0: 0°C (default) 1: 2°C
D3	B3	0: 0°C (default) 1: 1°C
D2	B2	0: 0°C (default) 1: 0.5°C
D1	B1	0: 0°C (default) 1: 0.25°C
D0	B0	0: 0°C (default) 1: 0.125°C

Table 84. Unipolar DAC Offset Registers (Register 0x30 to Register 0x33)

Bit Number(s)	Bit Name	Description
[D7:D6]	Reserved	Reserved
[D5:D4]	Offset	00: 0 V to 5 V (default) 01: 2.5 V to 7.5 V 10: 5 V to 10 V 11: 5 V to 10 V
[D3:D2]	Reserved	Reserved
D1	Copy	0: do not copy (default) 1: sets all unipolar DACs to same value
D0	Reserved	Reserved

Table 85. Bipolar DAC Offset Registers (Register 0x34 to Register 0x37)

Bit Number(s)	Bit Name	Description
[D7:D6]	Reserved	Reserved
[D5:D4]	Offset	00: 0 V to +5 V (default) 01: −4 V to +1 V 10: −5 V to 0 V 11: 0 V to +5 V in open loop, disables upper voltage limit in closed loop
[D3:D2]	Reserved	Reserved
D1	Copy	0: do not copy (default) 1: sets all bipolar DACs to same value
D0	Reserved	Reserved

OFFSET 1 (PAGE 0x0F)

Table 86. Offset 1 (Page 0x0F)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	AV_{DD} offset	1	R/W	0x0000
0x11	$DACV_{DD-UNI}$ offset	1	R/W	0x0000
0x12	$DACV_{DD-BI}$ offset	1	R/W	0x0000
0x13	AV_{SS} offset	1	R/W	0x0000
0x14	BI-$V_{OUT}0_{MON}$ offset	1	R/W	0x0000
0x15	BI-$V_{OUT}1_{MON}$ offset	1	R/W	0x0000
0x16	BI-$V_{OUT}2_{MON}$ offset	1	R/W	0x0000
0x17	BI-$V_{OUT}3_{MON}$ offset	1	R/W	0x0000
0x28	$RS0+_{MON}$ offset	1	R/W	0x0000
0x29	$RS1+_{MON}$ offset	1	R/W	0x0000
0x2A	$RS2+_{MON}$ offset	1	R/W	0x0000
0x2B	$RS3+_{MON}$ offset	1	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

AV_{DD}, DAC Supply ($DACV_{DD-UNI}$/$DACV_{DD-BI}$), and AV_{SS} Offset Registers (Register 0x10 to Register 0x13)

These read/write 8-bit registers store the offset values for the relevant supply voltage monitoring channels.

BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$ Offset Registers (Register 0x14 to Register 0x17)

These read/write 8-bit registers store the offset values for the relevant DAC monitoring channels.

$RSx+_{MON}$ Offset Registers (Register 0x28 to Register 0x2B)

These read/write 8-bit registers store the offset values for the relevant DAC monitoring channels. Note that, prior to conversion, the $RSx+_{MON}$ voltages are divided by 50.

Table 87. AV_{DD}, DAC Supply, AV_{SS}, BI-$V_{OUT}x_{MON}$, and $RSx+_{MON}$ Offset Registers (Register 0x10 to Register 0x2B)

Bit Number(s)	Bit Name	Description
D7	B7	0: 0 LSB (default) 1: −128 LSB
D6	B6	0: 0 LSB (default) 1: 64 LSB
D5	B5	0: 0 LSB (default) 1: 32 LSB
D4	B4	0: 0 LSB (default) 1: 16 LSB
D3	B3	0: 0 LSB (default) 1: 8 LSB
D2	B2	0: 0 LSB (default) 1: 4 LSB
D1	B1	0: 0 LSB (default) 1: 2 LSB
D0	B0	0: 0 LSB (default) 1: 1 LSB

ALERT (PAGE 0x10)

Table 88. Alert (Page 0x10)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x10	ALERTSUM	2	R/W	0x0000
0x12	V_{IN}x alert	2	R/W	0x0000
0x14	T_{SENSE}x alert	2	R/W	0x0000
0x15	I_{SENSE}x alert	2	R/W	0x0000
0x18	Supply and BI-V_{OUT}x$_{MON}$ alert	2	R/W	0x0000
0x19	RSx+$_{MON}$ alert	2	R/W	0x0000
0x1A	INT_{LIMIT}x and AV_{SS}/AV_{DD} alert	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

Alert Summary (ALERTSUM) Register (Register 0x10)

This 16-bit register stores the summary from the channel dedicated alert registers. If any of the bits from the corresponding alert register are set, the register bit is set to 1 (OR function of individual alert register bits). When 1 is written to any of the register bits, this bit is cleared, that is, removing alerts and the alert bits from the corresponding alert register. This write is a quick way to clear any alerts in the device. The upper byte contains the high alerts, whereas the lower byte contains the low alerts. This format is applicable to the individual alert registers as well. The default value of this register is 0x0000.

V_{IN}x Alert Register (Register 0x12)

This 16-bit register stores the V_{IN} channel related high and low alerts. When 1 is written to any of the register bits, this bit clears, removing the corresponding alert.

Temperature Sensor (T_{SENSE}x) Alert Register (Register 0x14)

This 16-bit register stores the temperature sensor related high and low alerts. When 1 is written to any of the register bits, this bit clears, removing the corresponding alert.

Current Sensor (I_{SENSE}x) Alert Register (Register 0x15)

This 16-bit register stores the current sensor related high and low alerts. When 1 is written to any of the register bits, this bit clears, removing the corresponding alert.

Table 89. Alert Summary (ALERTSUM) Register (Register 0x10), Bit D15 to Bit D8

D15	D14	D13	D12	D11	D10	D9	D8
RSx+ high	AV_{DD}/BI-V_{OUT}x high	INT_{LIMIT}x active	AV_{SS}/AV_{SS} alarm	I_{SENSE}x high	T_{SENSE}x high	Reserved	V_{IN}x high

Table 90. Alert Summary (ALERTSUM) Register (Register 0x10), Bit D7 to Bit D0

D7	D6	D5	D4	D3	D2	D1	D0
RSx+ low	AV_{DD}/BI-V_{OUT}x low	Reserved		I_{SENSE}x low	T_{SENSE}x low	Reserved	V_{IN}x low

Table 91. V_{IN}x Alert Register (Register 0x12)

MSB									LSB
[D15:D12]	D11	D10	D9	D8	[D7:D4]	D3	D2	D1	D0
Reserved	V_{IN}3 high	V_{IN}2 high	V_{IN}1 v	V_{IN}0 high	Reserved	V_{IN}3 low	V_{IN}2 low	V_{IN}1 low	V_{IN}0 low

Table 92. Temperature Sensor Alert Register (Register 0x14)

MSB							LSB
[D15:D11]	D10	D9	D8	[D7:D3]	D2	D1	D0
Reserved	T_{SENSE}D1 high	T_{SENSE}D0 high	T_{SENSE}INT high	Reserved	T_{SENSE}D1 low	T_{SENSE}D0 low	T_{SENSE}INT low

Table 93. Current Sensor Alert Register (Register 0x15)

MSB									LSB
[D15:D12]	D11	D10	D9	D8	[D7:D4]	D3	D2	D1	D0
Reserved	I_{SENSE}3 high	I_{SENSE}2 high	I_{SENSE}1 high	I_{SENSE}0 high	Reserved	I_{SENSE}3 low	I_{SENSE}2 low	I_{SENSE}1 low	I_{SENSE}0 low

Supply and BI-$V_{OUT}x_{MON}$ Alert Register (Register 0x18)

This 16-bit register stores the AV_{DD}, $DACV_{DD-UNI}$, DAC_{VDD-BI}, AV_{SS}, BI-$V_{OUT}x_{MON}$ high and low alerts. When 1 is written to any of the register bits, this bit clears, removing the corresponding alert.

RSx+$_{MON}$ Alert Register (Register 0x19)

This 16-bit register stores the RSx+ high and low alerts. When 1 is written to any of the register bits, this bit clears, removing the corresponding alert.

$INT_{LIMIT}x$ and AV_{SS}/AV_{DD} Alert Register (Register 0x1A)

This 16-bit register stores the closed-loop integrator limit active status and AV_{SS}/AV_{DD} alarm status.

Table 94. Supply and BI-$V_{OUT}x_{MON}$ Alert Register (Register 0x18), Bit D15 to Bit D8

D15	D14	D13	D12	D11	D10	D9	D8
BI-$V_{OUT}3_{MON}$ high	BI-$V_{OUT}2_{MON}$ high	BI-$V_{OUT}1_{MON}$ high	BI-$V_{OUT}0_{MON}$ high	AV_{SS} high	$DACV_{DD-BI}$ high	$DACV_{DD-UNI}$ high	AV_{DD} high

Table 95. Supply and BI-$V_{OUT}x_{MON}$ Alert Register (Register 0x18), Bit D7 to Bit D0

D7	D6	D5	D4	D3	D2	D1	D0
BI-$V_{OUT}3_{MON}$ low	BI-$V_{OUT}2_{MON}$ low	BI-$V_{OUT}1_{MON}$ low	BI-$V_{OUT}0_{MON}$ low	AV_{SS} low	$DACV_{DD-BI}$ low	$DACV_{DD-UNI}$ low	AV_{DD} low

Table 96. RSx+$_{MON}$ Alert Register (Register 0x19)

MSB									LSB
[D15:D12]	D11	D10	D9	D8	[D7:D4]	D3	D2	D1	D0
Reserved	RS3+$_{MON}$ high	RS2+$_{MON}$ high	RS1+$_{MON}$ high	RS0+$_{MON}$ high	Reserved	RS3+$_{MON}$ low	RS2+$_{MON}$ low	RS1+$_{MON}$ low	RS0+$_{MON}$ low

Table 97. $INT_{LIMIT}x$ and AV_{SS}/AV_{DD} Alert Register (Register 0x1A)

MSB						LSB
[D15:D12]	D11	D10	D9	D8	[D7:D1]	D0
Reserved	$INT_{LIMIT}3$ high	$INT_{LIMIT}2$ high	$INT_{LIMIT}1$ high	$INT_{LIMIT}0$ high	Reserved	AV_{SS}/AV_{DD} alarm

ALERT0 PIN ROUTING (PAGE 0x11)

All the registers from this page allow routing of the alert signals generated by the corresponding inputs/channels to the GPIO3/ALERT0 pin of the device. The upper byte controls the high alerts routing, whereas the lower byte controls the low alerts routing.

Table 98. ALERT0 Pin Routing (Page 0x11)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x12	V_{IN}x ALERT0	2	R/W	0x0000
0x14	T_{SENSE}x ALERT0	2	R/W	0x0000
0x15	I_{SENSE}x ALERT0	2	R/W	0x0000
0x18	Supply and BI-V_{OUT}x$_{MON}$ ALERT0	2	R/W	0x0000
0x19	RSx+$_{MON}$ ALERT0	2	R/W	0x0000
0x1A	INT_{LIMIT}x and AVss/AV_{DD} ALERT0	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x ALERT0 Register (Register 0x12)

This 16-bit register allows routing of the V_{IN}x generated alerts to the ALERT0 pin.

Temperature Sensor (T_{SENSE}x) ALERT0 Register (Register 0x14)

This 16-bit register allows routing of the temperature sensor generated alerts to the ALERT0 pin.

Current Sensor (I_{SENSE}x) ALERT0 Register (Register 0x15)

This 16-bit register allows routing of the current sensor generated alerts to the ALERT0 pin.

Supply and BI-V_{OUT}x$_{MON}$ ALERT0 Register (Register 0x18)

This 16-bit register allows routing of the supply channels and the bipolar DAC monitor channels generated alerts to the ALERT0 pin.

RSx+$_{MON}$ ALERT0 Register (Register 0x19)

This 16-bit register allows routing of the RSx+$_{MON}$ alerts to the ALERT0 pin.

INT_{LIMIT}x and AVss/AV_{DD} ALERT0 Register (Register 0x1A)

This 16-bit register allows routing of the closed-loop integrator limit and AV_{SS}/AV_{DD} alerts to the ALERT0 pin.

Table 99. V_{IN}x ALERT0 Register (Register 0x12)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	V_{IN}3 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D10	V_{IN}2 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D9	V_{IN}1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D8	V_{IN}0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
[D7:D4]	Reserved	Reserved
D3	V_{IN}3 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D2	V_{IN}2 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D1	V_{IN}1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D0	V_{IN}0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin

Table 100. Temperature Sensor ALERT0 Register (Register 0x14)

Bit Number(s)	Bit Name	Description
[D15:D11]	Reserved	Reserved
D10	T_{SENSE}D1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D9	T_{SENSE}D0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D8	T_{SENSE}INT high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
[D7:D3]	Reserved	Reserved
D2	T_{SENSE}D1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D1	T_{SENSE}D0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D0	T_{SENSE}INT low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin

Table 101. Current Sensor ALERT0 Register (Register 0x15)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	I_{SENSE}3 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D10	I_{SENSE}2 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D9	I_{SENSE}1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D8	I_{SENSE}0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
[D7:D4]	Reserved	Reserved
D3	I_{SENSE}3 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D2	I_{SENSE}2 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D1	I_{SENSE}1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D0	I_{SENSE}0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin

Table 102. Supply and BI-$V_{OUT}x_{MON}$ ALERT0 Register (Register 0x18)

Bit Number(s)	Bit Name	Description
D15	BI-$V_{OUT}3_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D14	BI-$V_{OUT}2_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D13	BI-$V_{OUT}1_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D12	BI-$V_{OUT}0_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D11	AV_{SS} high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D10	$DACV_{DD-BI}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D9	$DACV_{DD-UNI}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D8	AV_{DD} high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D7	BI-$V_{OUT}3_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D6	BI-$V_{OUT}2_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D5	BI-$V_{OUT}1_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D4	BI-$V_{OUT}0_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D3	AV_{SS} low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D2	$DACV_{DD-BI}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D1	$DACV_{DD-UNI}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D0	AV_{DD} low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin

Table 103. $RSx+_{MON}$ ALERT0 Register (Register 0x19)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	$RS3+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D10	$RS2+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D9	$RS1+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
D8	$RS0+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT0 pin
[D7:D4]	Reserved	Reserved
D3	$RS3+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D2	$RS2+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D1	$RS1+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin
D0	$RS0+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT0 pin

Table 104. $INT_{LIMIT}x$ and $AVss/AV_{DD}$ ALERT0 Register (Register 0x1A)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	$INT_{LIMIT}3$	0: no routing (default) 1: integrator limit active status routed to the ALERT0 pin
D10	$INT_{LIMIT}2$	0: no routing (default) 1: integrator limit active status routed to the ALERT0 pin
D9	$INT_{LIMIT}1$	0: no routing (default) 1: integrator limit active status routed to the ALERT0 pin
D8	$INT_{LIMIT}0$	0: no routing (default) 1: integrator limit active status routed to the ALERT0 pin
[D7:D1]	Reserved	Reserved
D0	AV_{SS}/AV_{DD}	0: no routing (default) 1: AV_{SS} or AV_{DD} alarm is routed to the ALERT0 pin

ALERT1 PIN ROUTING (PAGE 0x12)

All the registers from this page allow routing of the alert signals generated by the corresponding inputs/channels to the GPIO4/ALERT1 pin of the device. The upper byte controls the high alerts routing, whereas the lower byte controls the low alerts routing.

Table 105. ALERT1 Pin Routing (Page 0x12)

Address (Hex)	Name	Byte[1]	Access Type[1]	Default Value[1]
0x00	No op	N/A	N/A	0x00
0x01	Page select pointer	1	R/W	0x00
0x02	Conversion command[2]	1	W	N/A
0x03	Result	2	R	0x0000
0x04	DAC enable	1	R/W	0x00
0x05	GPIO	1	R/W	0x00
0x0C	Device ID	2	R	0x0018
0x0F	Software reset	2	R/W	0x0000
0x12	V_{IN}x ALERT1	2	R/W	0x0000
0x14	T_{SENSE}x ALERT1	2	R/W	0x0000
0x15	I_{SENSE}x ALERT1	2	R/W	0x0000
0x18	Supply and BI-$V_{OUT}x_{MON}$ ALERT1	2	R/W	0x0000
0x19	RSx+$_{MON}$ ALERT1	2	R/W	0x0000
0x1A	INT_{LIMIT}x and AVss/AV_{DD} ALERT1	2	R/W	0x0000

[1] N/A means not applicable.
[2] Not a physical register.

V_{IN}x ALERT1 Register (Register 0x12)

This 16-bit register allows routing of the V_{IN}x generated alerts to the ALERT1 pin.

Temperature Sensor (T_{SENSE}x) ALERT1 Register (Register 0x14)

This 16-bit register allows routing of the temperature sensor generated alerts to the ALERT1 pin.

Current Sensor (I_{SENSE}x) ALERT1 Register (Register 0x15)

This 16-bit register allows routing of the current sensor generated alerts to the ALERT1 pin.

Supply and BI-$V_{OUT}x_{MON}$ ALERT1 Register (Register 0x18)

This 16-bit register allows routing of the supply channels and the bipolar DAC monitor channels generated alerts to the ALERT1 pin.

RSx+$_{MON}$ ALERT1 Register (Register 0x19)

This 16-bit register allows routing of the RSx+$_{MON}$ alerts to the ALERT1 pin.

INT_{LIMIT}x and AV_{SS}/AV_{DD} ALERT1 Register (Register 0x1A)

This 16-bit register allows routing of the closed-loop integrator limit and AV_{SS}/AV_{DD} alerts to the ALERT1 pin.

Table 106. V_{IN}x ALERT1 Register (Register 0x12)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	V_{IN}3 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D10	V_{IN}2 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D9	V_{IN}1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D8	V_{IN}0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
[D7:D4]	Reserved	Reserved
D3	V_{IN}3 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D2	V_{IN}2 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D1	V_{IN}1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D0	V_{IN}0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin

Table 107. Temperature Sensor ALERT1 Register (Register 0x14)

Bit Number(s)	Bit Name	Description
[D15:D11]	Reserved	Reserved
D10	T_{SENSE}D1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D9	T_{SENSE}D0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin.
D8	T_{SENSE}INT high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin.
[D7:D3]	Reserved	Reserved
D2	T_{SENSE}D1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D1	T_{SENSE}D0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D0	T_{SENSE}INT low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin

Table 108. Current Sensor ALERT1 Register (Register 0x15)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	I_{SENSE}3 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D10	I_{SENSE}2 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D9	I_{SENSE}1 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D8	I_{SENSE}0 high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
[D7:D4]	Reserved	Reserved
D3	I_{SENSE}3 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D2	I_{SENSE}2 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D1	I_{SENSE}1 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D0	I_{SENSE}0 low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin

Table 109. Supply and BI-$V_{OUT}x_{MON}$ ALERT1 Register (Register 0x18)

Bit Number(s)	Bit Name	Description
D15	BI-$V_{OUT}3_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D14	BI-$V_{OUT}2_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D13	BI-$V_{OUT}1_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D12	BI-$V_{OUT}0_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D11	AV_{SS} high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin

Bit Number(s)	Bit Name	Description
D10	$DACV_{DD-BI}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D9	$DACV_{DD-UNI}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D8	AV_{DD} high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pi.
D7	BI-$V_{OUT}3_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D6	BI-$V_{OUT}2_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D5	BI-$V_{OUT}1_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D4	BI-$V_{OUT}0_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D3	AV_{SS} low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D2	$DACV_{DD-BI}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D1	$DACV_{DD-UNI}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D0	AV_{DD} low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin

Table 110. $RSx+_{MON}$ ALERT1 Register (Register 0x19)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	$RS3+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D10	$RS2+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D9	$RS1+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
D8	$RS0+_{MON}$ high	0: no routing (default) 1: high alert on the corresponding channel routes to the ALERT1 pin
[D7:D4]	Reserved	Reserved (default)
D3	$RS3+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D2	$RS2+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D1	$RS1+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin
D0	$RS0+_{MON}$ low	0: no routing (default) 1: low alert on the corresponding channel routes to the ALERT1 pin

Table 111. $INT_{LIMIT}x$ and $AVss/AV_{DD}$ ALERT1 Register (Register 0x1A)

Bit Number(s)	Bit Name	Description
[D15:D12]	Reserved	Reserved
D11	$INT_{LIMIT}3$	0: no routing (default) 1: integrator limit active status routed to the ALERT1 pin
D10	$INT_{LIMIT}2$	0: no routing (default) 1: integrator limit active status routed to the ALERT1 pin
D9	$INT_{LIMIT}1$	0: no routing (default) 1: integrator limit active status routed to the ALERT1 pin
D8	$INT_{LIMIT}0$	0: no routing (default) 1: integrator limit active status routed to the ALERT1 pin
[D7:D1]	Reserved	Reserved
D0	AV_{SS}/AV_{DD}	0: no routing (default) 1: AV_{SS} or AV_{DD} alarm is routed to the ALERT1 pin

SERIAL PORT INTERFACE

The AD7293 SPI allows the user to configure the device for specific functions and operations through an internal structured register space. The interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The device is capable of interfacing within a range of 1.7 V to 5.5 V, which is set by the V_{DRIVE} pin. SCLK is the serial clock input for the device. All data transfers on DIN or DOUT take place with respect to SCLK. The chip select input pin ($\overline{CS}$) is an active low control. For the interface to be active, the chip select must be low. Data is clocked into the AD7293 on the SCLK rising edge and is loaded into the device MSB first. The length of each SPI frame can vary according to the command being sent. A no op command is available for interface flexibility. Data is clocked out of the AD7293 on DOUT in the same frame as the read command, on the falling edge of SCLK, while $\overline{CS}$ is low. The SCLK and DIN signals are ignored when $\overline{CS}$ is high, and the DOUT line becomes high impedance.

INTERFACE PROTOCOL

When reading from or writing to the AD7293, the first byte contains the address pointer. Bit D7 of the address pointer is the read (high) and write (low) bit.

Table 112. Address Pointer

D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	X[1]	Register/page select					

[1] X means don't care.

Bit D5 to Bit D0 of the address pointer specify the register address for the read or write operation.

After the address pointer, the data to be written to the device is supplied in bytes. The register structure of the AD7293 is page based and divided according to their specific functions. Some registers are common to all pages, whereas the rest of the registers are contained within a particular page. To select a page, write to the 8-bit page select register. When a particular page is selected, the user does not have to rewrite to the page select register every time prior to writing to a register from the same page. Figure 52 to Figure 54 show the read and write data formats for the AD7293.

For a register write, the read/write bit is zero, and the DOUT line remains high impedance. Upon completion of a read or write, the AD7293 is ready to accept a new register address; alternatively, to terminate the operation, take the $\overline{CS}$ pin high.

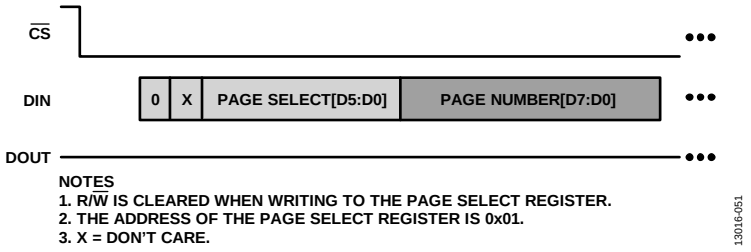

Figure 52. Accessing a Page

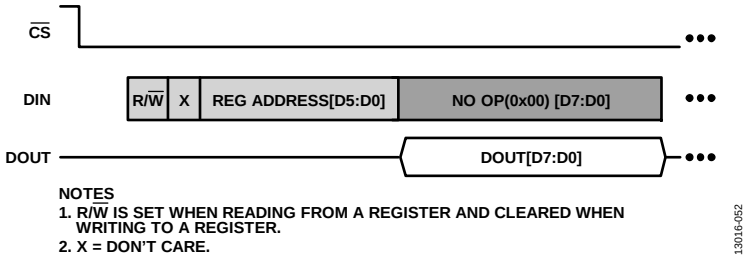

Figure 53. Accessing an 8-Bit Register

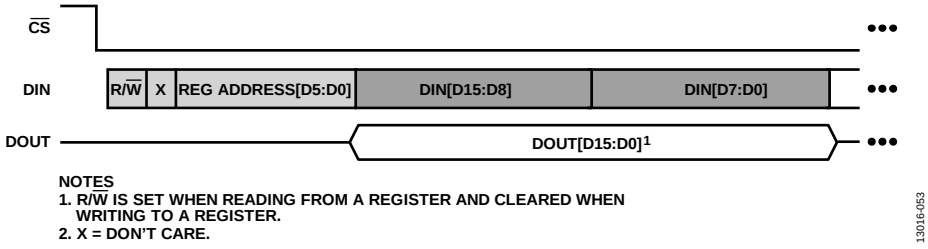

Figure 54. Accessing a 16-Bit Register

MODES OF OPERTION

There are two methods of initiating a conversion on the AD7293: background mode and command mode.

Background Mode (BG)

The AD7293 can be configured to continuously convert on a programmable cycle of channels, making it the ideal mode of operation for system monitoring. These conversions take place in the background and are transparent to the master. Typically, this mode is used to automatically monitor a selection of channels with either the limit registers programmed to signal an out of range condition via the alert function or with the minimum/maximum recorders tracking the variation over time of a particular channel. Reads and writes can be performed at any time during this mode (the result registers contains the most recent conversion results).

On power-up, this mode is disabled. This mode can be enabled by writing to the background enable bits (V_{IN}x background enable register; temperature sensor background enable register; current sensor background enable register; and the $RS+_{MON}$, supply monitor, and BI-V_{OUT}x background enable register) from the configuration page. The background conversions are active only when $\overline{CS}$ is pulled high, that is, the interface is not active. When $\overline{CS}$ is pulled low, the conversions pauses and resumes from the last channel in the cycle when $\overline{CS}$ is pulled high again. The user can read back the conversion results via the channel specific result registers.

If a command mode conversion is requested while the background mode is active, the scheduled background mode conversion from the cycle pauses while $\overline{CS}$ is low and tags onto the command mode conversion. Conversion is reflected in the ADC busy signal, which stays true for the combined duration of the command mode conversion and the background mode.

If the background conversions are enabled during the closed-loop mode operation, they run continuously irrespective of $\overline{CS}$ status. However, the results of the ADC conversions are only stored if $\overline{CS}$ is pulled high.

The ADC background cycle prioritizes in the following order: $V_{IN}0$ to $V_{IN}3$, T_{SENSE}INT, T_{SENSE}D0, T_{SENSE}D1, $I_{SENSE}0$ to $I_{SENSE}3$, voltage supply monitoring, BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$, and $RS0+_{MON}$ to $RS3+_{MON}$.

Command Mode

Command mode is useful for controlling the sampling instant on the V_{IN}x channels if an ac waveform is being converted. To enter this mode and initiate a conversion on a channel, the special command byte, 0x82, must be written to the device.

When the conversion command is received, the AD7293 uses the current values in the registers on the sequence page to determine which channel to convert on and subsequently read back from. The common result register is updated with the result of the current conversion channel, which allows the user to continuously read back the conversion results in command mode. The ADC command mode sequencer prioritizes in this order: $V_{IN}0$ to $V_{IN}3$, T_{SENSE}INT, T_{SENSE}D0, T_{SENSE}D1, $I_{SENSE}0$ to $I_{SENSE}3$, voltage supply monitoring, BI-$V_{OUT}0_{MON}$ to BI-$V_{OUT}3_{MON}$, and $RS0+_{MON}$ to $RS3+_{MON}$. The sequencer can be reset by writing to any of the sequence registers.

In the example in Figure 55, to initiate the continuous conversion command mode, point to the sequence page and write to the relevant sequence registers. The ADC sequence register is programmed to convert on analog input channels, $V_{IN}0$ to $V_{IN}2$, in this example. The first conversion takes place when the AD7293 enters command mode after the special command byte. Every subsequent conversion is initiated after the result readback frame, as shown in Figure 55.

Figure 56 shows another example for a command mode conversion with a fixed 24-bit SPI frame length. The first conversion is initiated when the device enters the command mode after the special command byte, which is followed by a 24-bit readback of the conversion result. The device exits command mode when $\overline{CS}$ is pulled high, although the sequencer is not reset. Every subsequent conversion is initiated by reentering the command mode via the special command byte after which the user must wait long enough to allow the device to finish any conversions before reading back the next result.

Current Sensor and Temperature Sensor Conversions

Conversions on the temperature and current sensor channels can be enabled only via one set of registers, T_{SENSE}x background enable and I_{SENSE}x background enable, respectively, unlike the other channels, because the current sense and temperature sense amplifiers work by integrating the input voltage for a fixed amount of time, depending on the gain required. At the end of this integration period, a request is sent to the ADC for a conversion to be performed. The ADC deals with these requests in the order in which they arrive. For the other channels, the ADC starts converting immediately. The corresponding sequence register for these channels is used only to put the temperature and current sensor results in the command mode readback sequence and not to enable conversions on these channels.

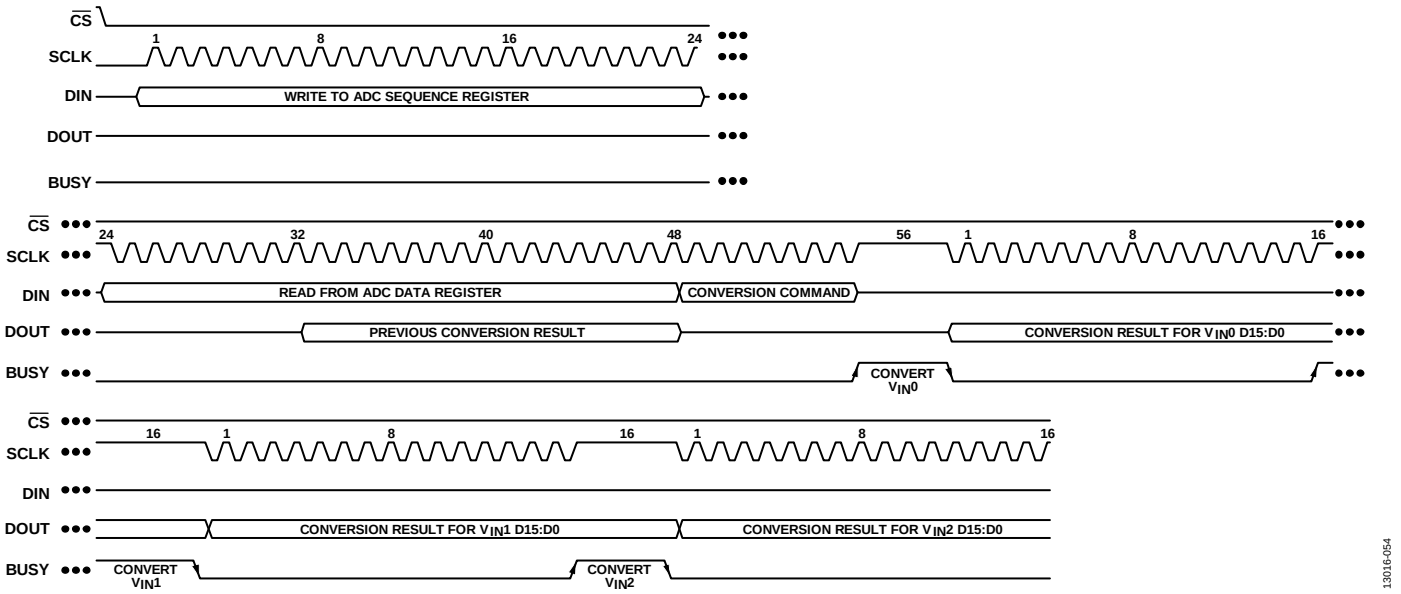

Figure 55. Continuous Conversion Command Mode Example

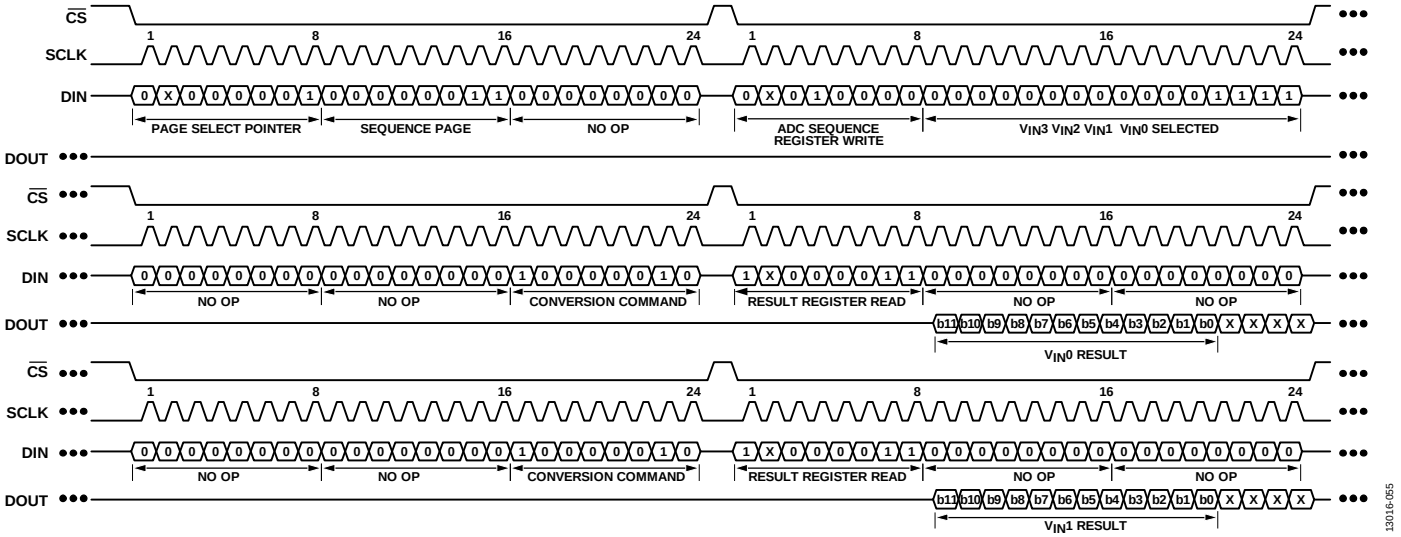

Figure 56. Command Mode Read Example (24-Bit Fixed Frame, $\overline{CS}$ Taken High After Each Conversion)

Conversion Timing

Table 113 shows the approximate conversion times for each type of channel under nominal conditions. Note that the temperature and current sensor channels, when enabled, are background conversions that are added on in command mode because the integration/sense times are greater than other ADC reads.

Table 113. Typical Conversion Time

Channel	Command Mode	Background Mode (µs)
$V_{IN}x$	0.7 µs	2.3
$I_{SENSE}x$	Not applicable	4.2
$T_{SENSE}x$	Not applicable	2.3
Monitor	4.0 µs	4.0

Current Sense and Temperature Sense Channel Integration Time

The internal current sense and temperature sense amplifiers function by integrating the input voltage for a fixed amount of time depending on the gain required. At the end of the integration period, a request is sent to the ADC for a conversion to be performed. The ADC deals with these requests in the order in which they arrive.

Table 114. Current Sensor Integration Time

Code	Gain	Clocks	Typical Integration Time (µs)
0000	6.25	440	17.6
0001	12.5	650	26.0
0010	18.75	860	34.4
0011	25	1070	42.8
0100	37.5	1490	59.6
0101	50	1910	76.4
0110	75	2750	110.0
0111	100	3590	143.6
1000	200	6950	278.0
1001	400	13670	546.8
1010	781.25	26480	1059.2

Table 115. Temperature Sensor Integration time

Channel	Clocks	Typical Integration Time (µs)
T_{SENSE}INT	30523	1220.92
T_{SENSE}D0	60987	2439.48
T_{SENSE}D1	60987	2439.48

Each current sense channel has its own integrator, whereas there is only one integrator for all three temperature channels. Therefore, temperature inputs that are enabled are measured sequentially. This means that, for example, if all are enabled, the update time is (1220.92 µs + 2 × 2439.48 µs) = 6099.88 µs

Conversion and Integration Timing Example 1

Enable three of the current sense channels with a gain of 6.25. All three integrations start as soon as the enable register is written to. After 17.6 µs, all three voltages are ready to be converted by the ADC. The $I_{SENSE}0$ channel is converted first, while the $I_{SENSE}1$ channel and the $I_{SENSE}2$ channel are held in the queue. After the $I_{SENSE}0$ conversion is complete, the $I_{SENSE}0$ amplifier is released to start a new integration, and the ADC moves on to convert the $I_{SENSE}1$ voltage.

The AD7293 settles into a routine, converting the three $I_{SENSE}x$ channels, each with an update time of (17.6 µs + 4.2 µs) = 21.8 µs.

See Figure 57 for more details.

Conversion and Integration Timing Example 2

In this example, in addition to the three current sense channels, three monitor channels are also enabled, as shown in Figure 58. The ADC is busy all the time; therefore, the time it takes to complete a cycle of conversions is the sum of all the conversion times: (4.2 µs × 3 + 4.0 µs × 3) = 24.6 µs.

If the temperature sensor is also enabled, when the output of the temperature sensor is ready (once every 1 ms to 2 ms depending on which channels are selected), the ADC sequencer waits for its turn in the sequence before initiating a conversion on the particular $T_{SENSE}x$ channel. The combination of conversions increases the duration of that particular cycle from 24.6 µs to (24.6 µs + 2.3 µs) = 26.9 µs in this example.

Digital Filtering

A digital filter is available on the ADC channels. The digital filter consists of a simple low-pass filter function to help reduce unwanted noise on dc signals. This low-pass filter has a −3 dB cutoff frequency of

$$f_{-3dB} = \frac{f_S}{2\pi \times 64} \approx \frac{f_S}{400}$$

where f_S is the sample frequency. The sample frequency depends on the type of channel, how many other channels are enabled, and whether it is in background mode or command mode (for example, if the internal temperature sensor channel is enabled alone, the update period is 1220.92 µs typically, which is close to $f_S \approx 819$ Hz). If $V_{IN}0$, $V_{IN}1$, $V_{IN}2$, and $V_{IN}3$ are also enabled in background mode, a conversion then takes place on $V_{IN}0$ every 9.2 µs (2.3 µs × 4), meaning $f_S \approx 1 \div 9.2$ µs ≈ 108.7 kHz. To avoid aliasing of high frequencies at the input, use an antialias filter to reject input frequencies above $f_S/2$.

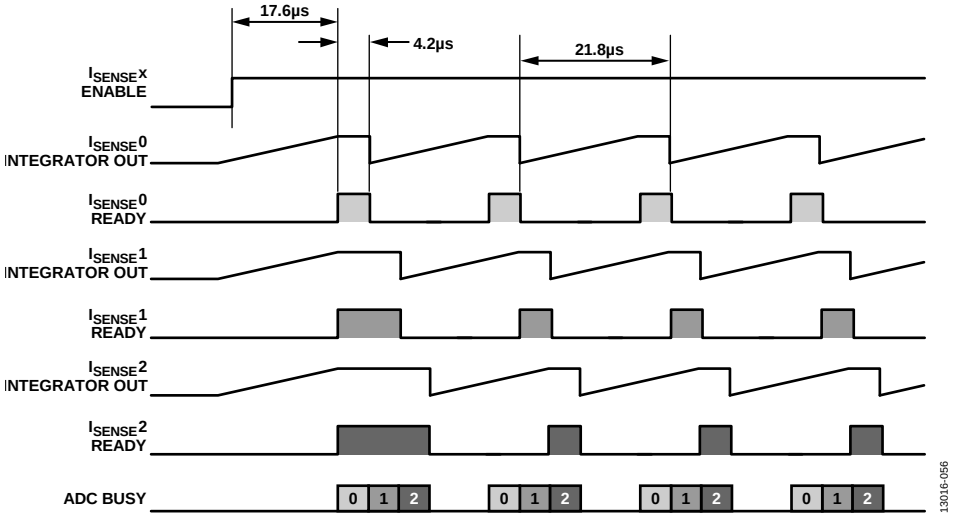

Figure 57. Conversation and Integration Internal Timing Example 1

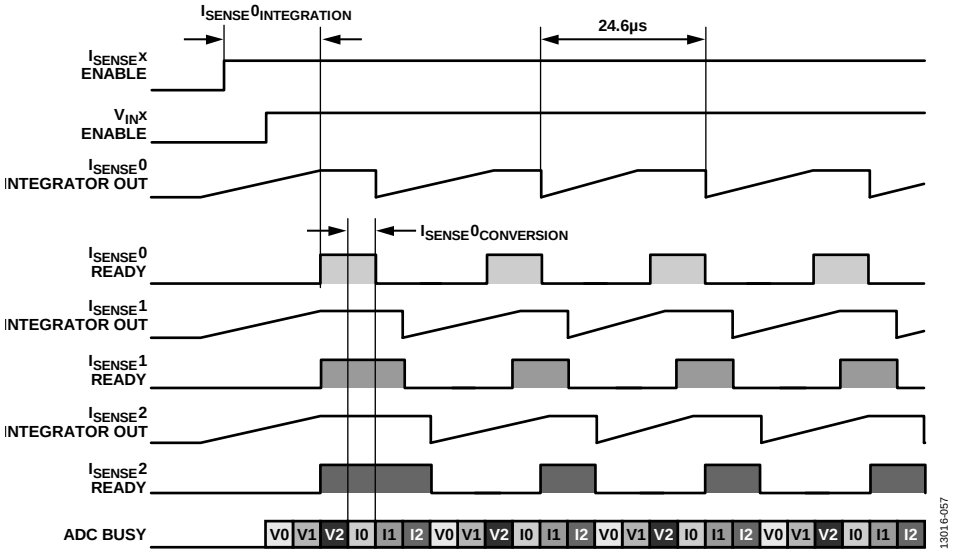

Figure 58. Conversion and Integration Internal Timing Example 2

APPLICATIONS INFORMATION

The AD7293 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature. With its 60 V maximum common-mode range, the device is useful in applications where current sensing in the presence of a high common-mode voltage is required. Closed-loop mode is designed for monitoring and controlling, for example, the power amplifier in a cellular base station.

BASE STATION POWER AMPLIFIER CONTROL

The AD7293 is used in a signal chain to achieve the optimal bias conditioning for enhancement mode or depletion mode power amplifiers. The main factors influencing the bias conditions are temperature, supply voltage, gate voltage drift, and general processing parameters. The overall performance of a power amplifier configuration is determined by the inherent trade-offs required in efficiency, gain, and linearity. The high level of integration as well as the intelligent features offered by the AD7293 allows the use of a single chip to dynamically control the drain bias current to maintain a constant value over temperature and time, thus significantly improving the overall performance of the power amplifier. The AD7293 incorporates the functionality of eight discrete components, providing considerable board area savings over discrete solutions.

The circuit shown in Figure 59 is the typical power amplifier control application diagram for the AD7293. The device monitors and controls the overall performance of four final stage amplifiers. The gain control and phase adjustment of the driver stage are incorporated in the application and are carried out by the four available uncommitted outputs of the AD7293. The high-side current sensor measures the amount of current on the respective final stage amplifiers while the closed-loop system maintains the programmed current across the sense resistor. Furthermore, the PA_ON provides optional control for a cutoff switch on the supply. The ALERTx pins can be configured to trigger when current readings are more than a specified limit and the RF input signal can be switched off by the ALERTx pin. The alert feature can also be routed internally to clamp the DAC outputs and turn off the power.

By measuring the transmitted (Tx) power and the received (Rx) power, the device can dynamically change the drivers and PA signal to optimize performance.

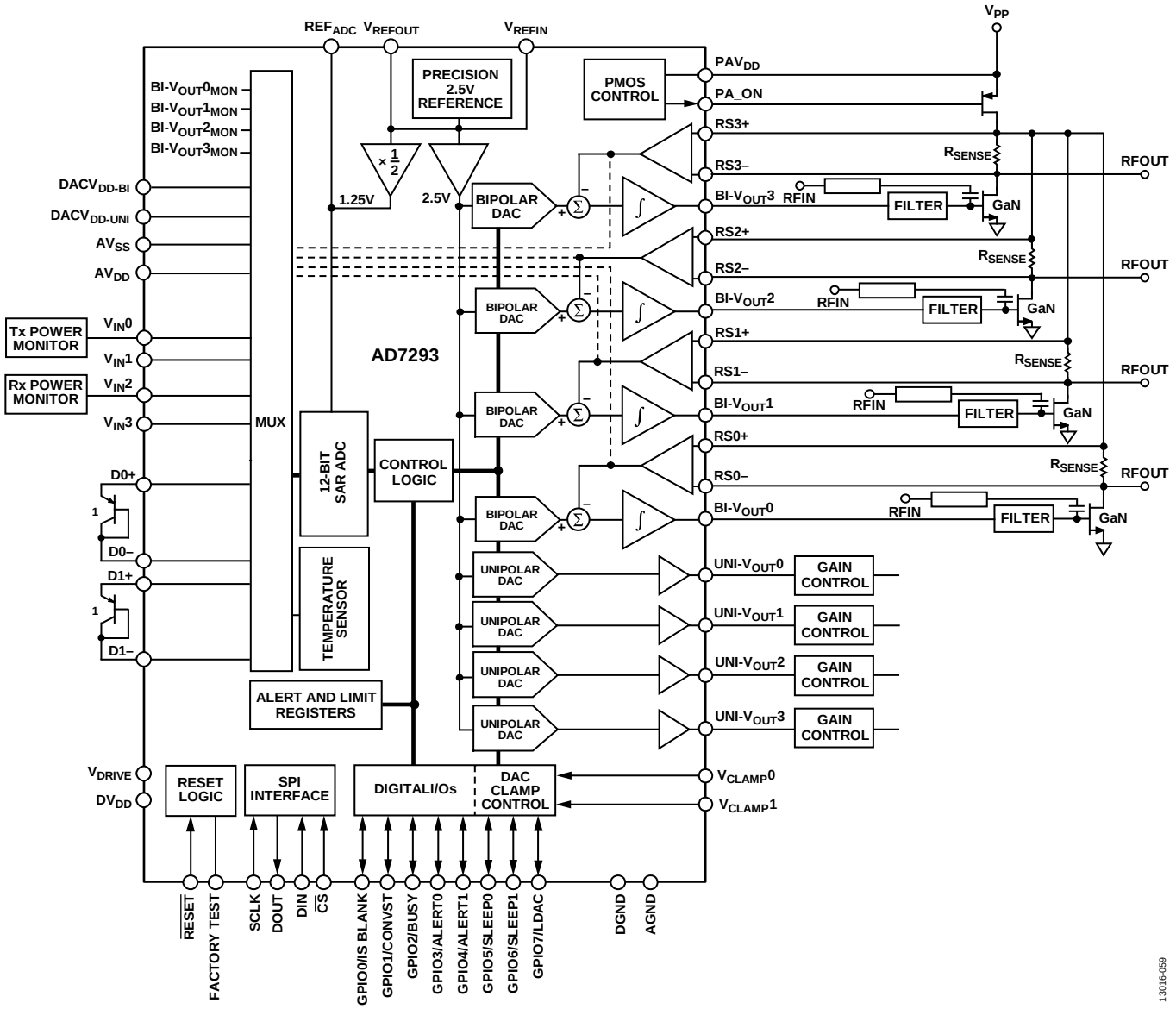

Figure 59. Typical Power Amplifier Control Application

DEPLETION MODE AMPLIFIER BIASING AND PROTECTION

Depletion mode devices (for example, gallium nitride (GaN) or gallium arsenide (GaAs)) require temperature compensated gate biasing voltages similar to enhancement mode devices (for example, laterally diffused metal oxide semiconductor (LDMOS)) to maintain constant quiescent drain current with temperature. The most important consideration for a depletion mode device is the biasing sequence. If the gate of a depletion mode device is at 0 V and the drain voltage is applied, the device may be damaged by drawing excessive current. It is also likely that a device may become potentially unstable at lower drain source voltages. Therefore, decreasing the gate voltage to less than the pinch off voltage while the drain voltage is being powered on and off is necessary.

The AD7293 was designed for depletion mode power amplifier biasing. Bipolar DAC outputs enable negative voltage biasing of the gate on the depletion mode device. A closed-loop mode combined with a low temperature drift reference ensures that the loop is steady over temperature.

The AD7293 works to ensure that instability or destruction of the depletion mode device is avoided. A PA_ON signal allows the user the option to control an external PMOS switch to turn on and off the drain current. This signal is set to the off state on power-up. Because depletion mode devices require a negative bias to remain at an acceptable level, and bipolar DACs transmit on the AV_{SS} supply for proper operation, PA_ON can be triggered when AV_{SS} exceeds an acceptable level.

In the event of an AV_{DD} voltage supply failure, the bipolar DACs clamp to the AV_{SS} supply (−5 V), which ensures that the PA

threshold voltage is not exceeded in the event of AV_{DD} voltage supply failure.

The on-chip bipolar DAC clamping circuitry ensures that the four bipolar outputs are set to their clamp value on power-up, and the DACs can be triggered to clamp by the external SLEEPx pins at any stage by the user.

The voltage monitoring of the supply voltages can help to quickly detect any system issues. The bipolar DAC output monitoring can be useful in closed-loop mode to sense the voltage output controlling the PA gate. Monitoring of the RSx+ pins voltages helps in detecting issues on the high side of the sense resistor.

To adhere to radio standards, it may be necessary to control the rate at which the PA gain changes. A ramp register is available that allows the user to control the slew rate of the DAC in closed-loop mode. Additionally, a closed-loop sequence is provided in the Closed-Loop Sequencing section to ensure the protection of the power amplifier from an overvoltage.

LOOP COMPONENT SELECTION

To select the loop component, use the following conditions:

$$R_S \leq 0.2/I_{DS(MAX)}$$

$$R_S \leq \tau_I/(52.5\ \mu s \times g_{m(MAX)})$$

$$\tau_G \leq \tau_I/(25 \times g_{m(MAX)} \times R_S)$$

$$\tau_S \leq (1/10) \times \tau_G$$

where:
R_S is the value of the current sense resistor in ohms.
$I_{DS(MAX)}$ is the PA drain current at the maximum required PA gain in amperes.
τ_I is the integrator time constant (default value = 840 µs) in seconds.
$g_{m(MAX)}$ is the PA transconductance at the maximum required PA gain in Siemens.
τ_G is the gate filter time constant in seconds.
τ_S is the current sense filter time constant in seconds.

To optimize the loop response from this point, the R_S, τ_I, τ_G, and τ_S values can be adjusted (see Table 116).

Table 116. R_S, τ_I, τ_G, and τ_S Adjustment Values

Parameter	Benefit of Increasing	Benefit of Decreasing
R_S	Setpoint resolution increased, improved dynamic range, and faster settling	Reduced overshoot, reduced power dissipation, and allows higher τ_G and τ_S
τ_I	Reduced overshoot, allows higher τ_G and τ_S	Faster settling
τ_G	Reduced noise from current control loop	Reduced overshoot, allows lower τ_I
τ_S	Improved filtering of disturbances at current sense input	Reduced overshoot, allows lower τ_I

When setting τ_G, do not exceed the maximum load capacitance specification (10 nF when R_G = 0 Ω, and 1 µF when R_G = 5 Ω). Include the PA gate capacitance in the calculation.

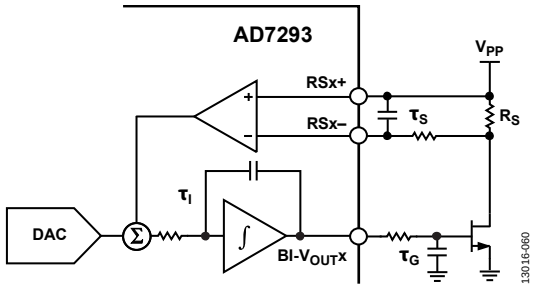

Figure 60. Loop Component Selection and Filtering

OUTLINE DIMENSIONS

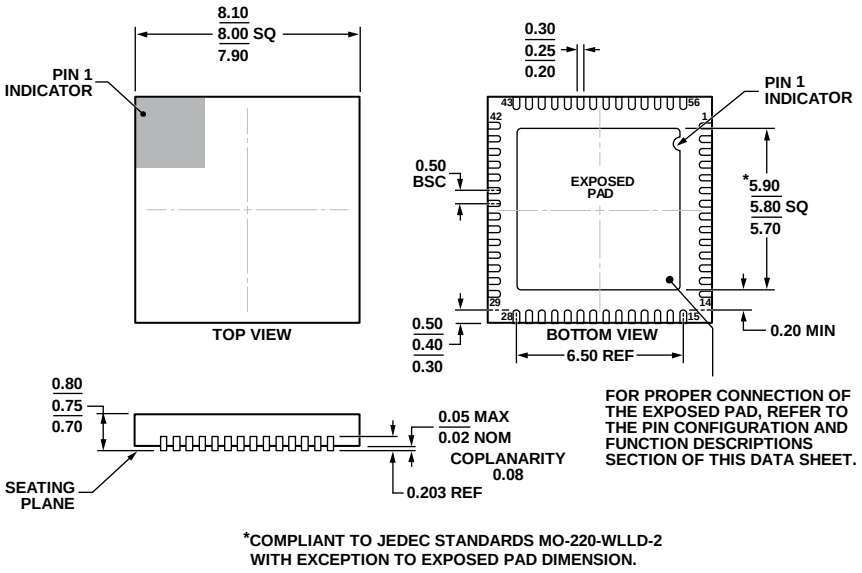

Figure 61. 56-Lead Lead Frame Chip Scale Package [LFCSP_WQ],
8 mm × 8 mm Body, Very Very Thin Quad
(CP-56-8)
Dimensions Shown in Millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7293BCPZ	−40°C to +125°C	56-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-56-8
AD7293BCPZ-RL	−40°C to +125°C	56-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-56-8
EVAL-AD7293SDZ		Evaluation Control Board	

[1] Z = RoHS Compliant Part.