

## N-Channel 200-V (D-S) 175 °C MOSFET

**PRODUCT SUMMARY**

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
200	0.030 at $V_{GS} = 10$ V	65 <sup>a</sup>

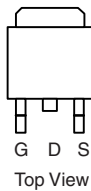
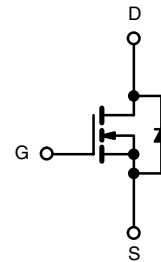
**FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 %  $R_g$  Tested


**RoHS**  
COMPLIANT

**APPLICATIONS**

- Isolated DC/DC Converters

**TO-263**

**Ordering Information:** SUM65N20-30-E3 (Lead (Pb)-free)


N-Channel MOSFET

**ABSOLUTE MAXIMUM RATINGS**  $T_C = 25$  °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	200	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	65 <sup>a</sup>	A
		$T_C = 125$ °C	37 <sup>a</sup>	
Pulsed Drain Current	$I_{DM}$	140		
Avalanche Current	$I_{AS}$	35		
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	61	mJ	
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	375 <sup>c</sup>	W
		$T_A = 25$ °C <sup>d</sup>	3.75	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C	

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

- Package limited.
- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).

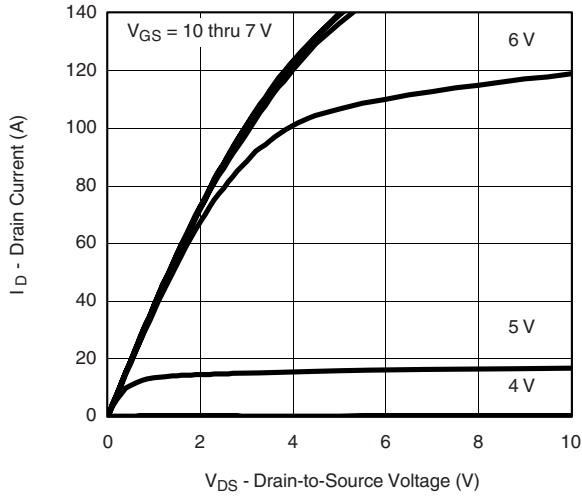
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.023	0.030	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.063	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.084	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		5100		$\text{pF}$
Output Capacitance	$C_{oss}$			480		
Reverse Transfer Capacitance	$C_{rss}$			210		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 85\text{ A}$		90	130	$\text{nC}$
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			23		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			34		
Gate Resistance	$R_g$		0.5	1.7	3.3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 65\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		24	35	$\text{ns}$
Rise Time <sup>c</sup>	$t_r$			220	330	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			45	70	
Fall Time <sup>c</sup>	$t_f$			200	300	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	$I_S$				65	A
Pulsed Current	$I_{SM}$				140	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 65\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	$Q_{rr}$			0.52	1.2	$\mu\text{C}$

**Notes:**

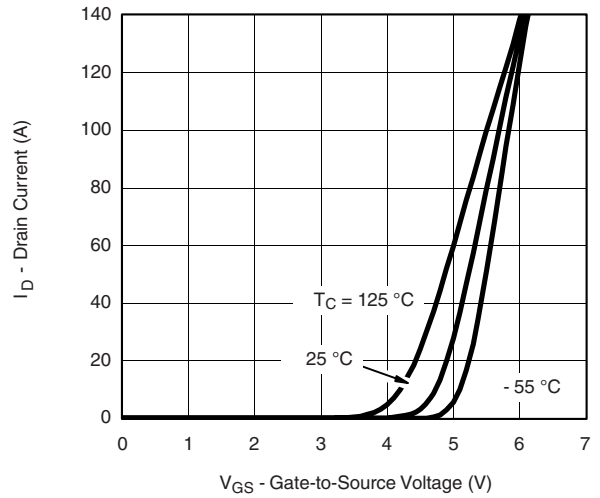
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

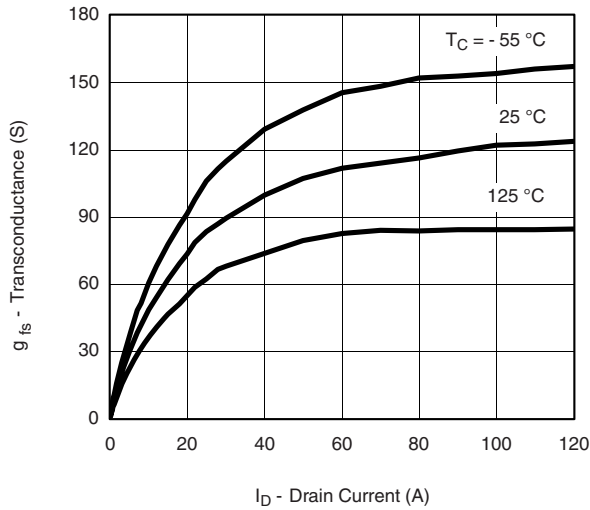
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



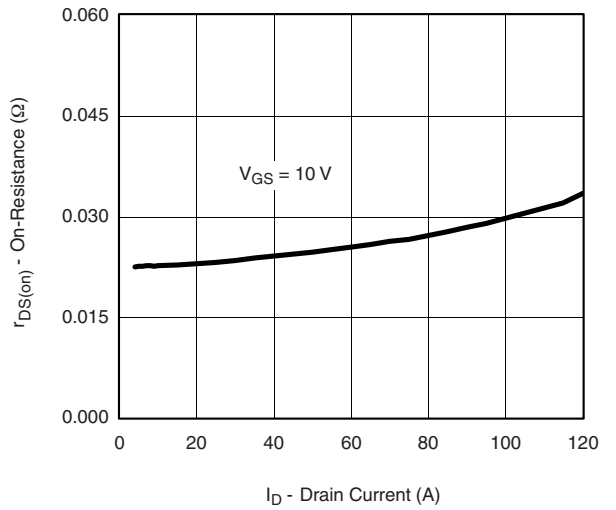
**Output Characteristics**



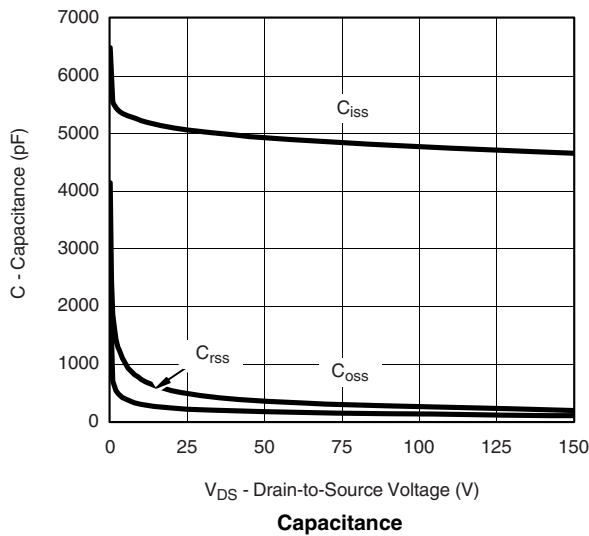
**Transfer Characteristics**



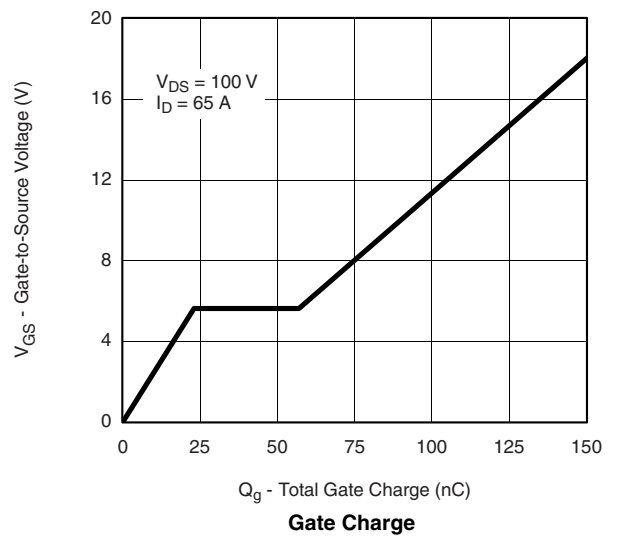
**Transconductance**



**On-Resistance vs. Drain Current**

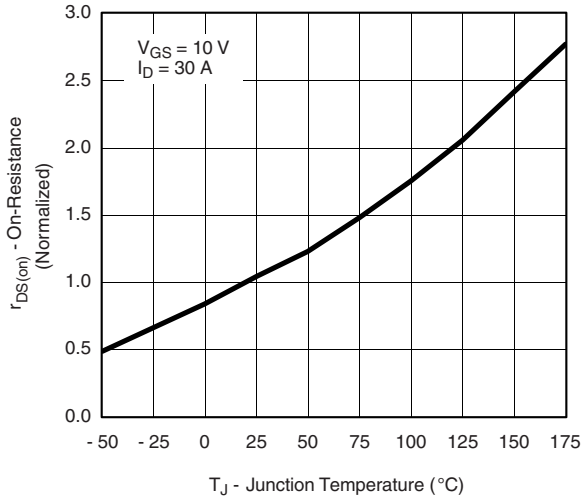


**Capacitance**

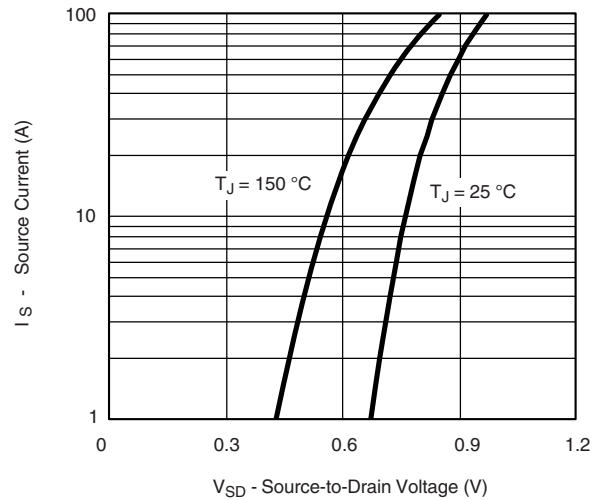


**Gate Charge**

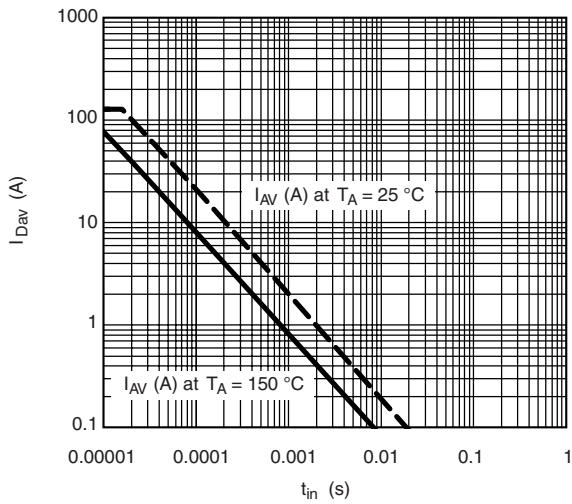
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



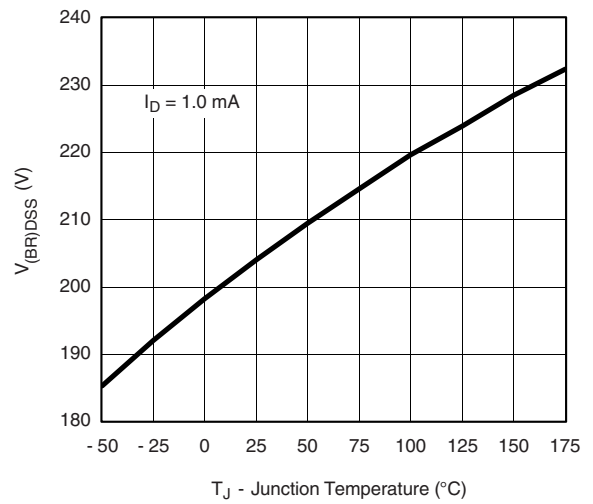
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



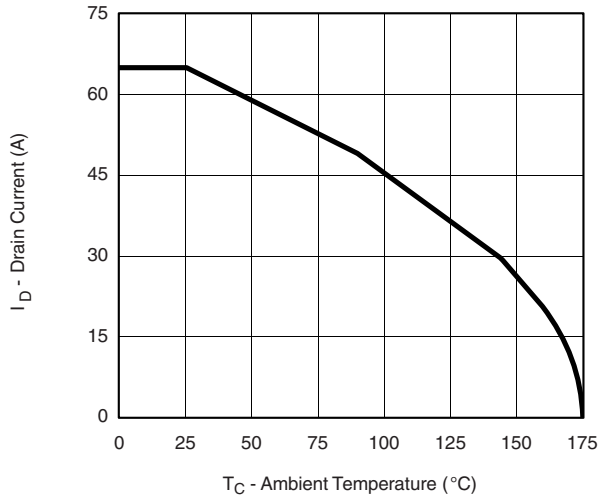
**Avalanche Current vs. Time**



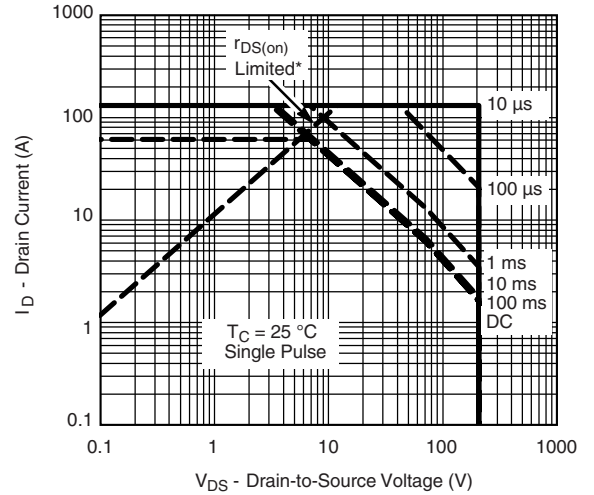
**Drain Source Breakdown vs. Junction Temperature**



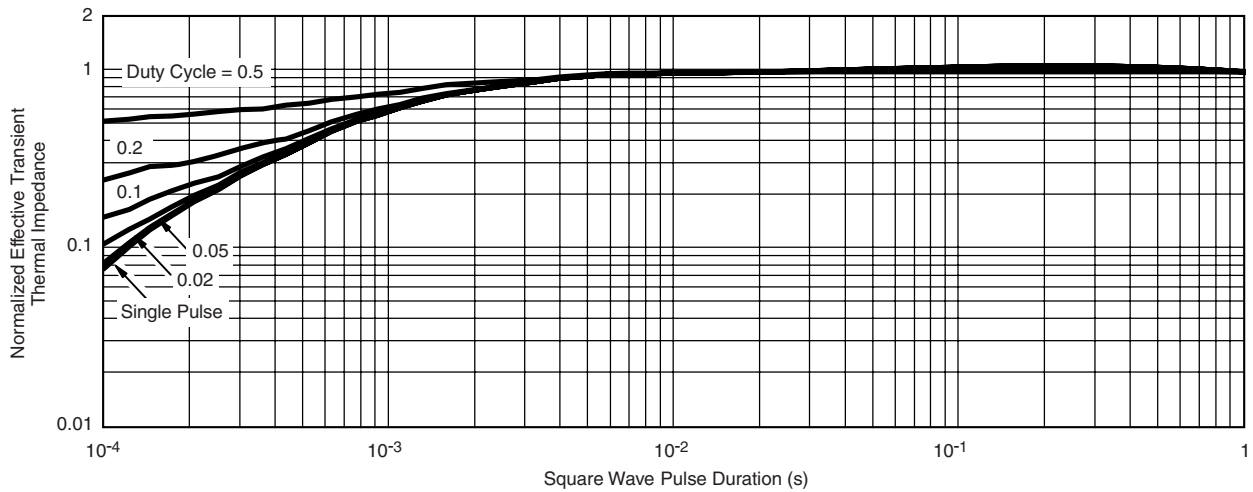
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**



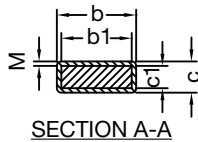
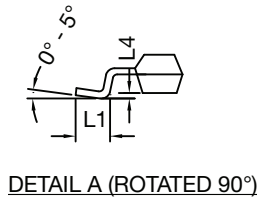
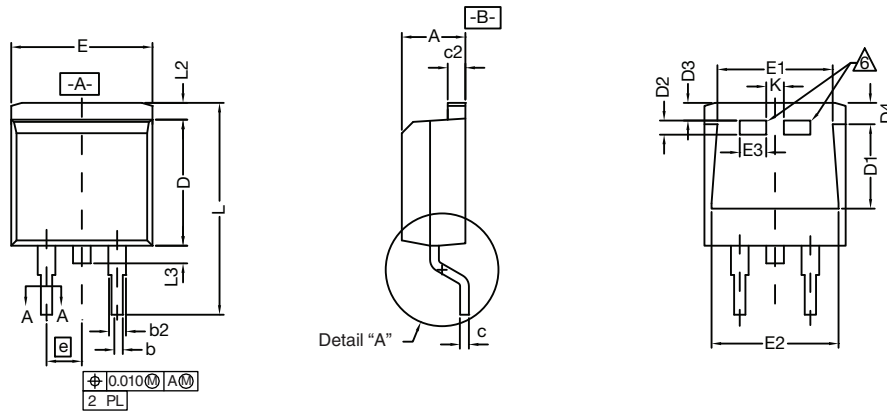
**Safe Operating Area**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified



**Normalized Thermal Transient Impedance, Junction-to-Case**

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD

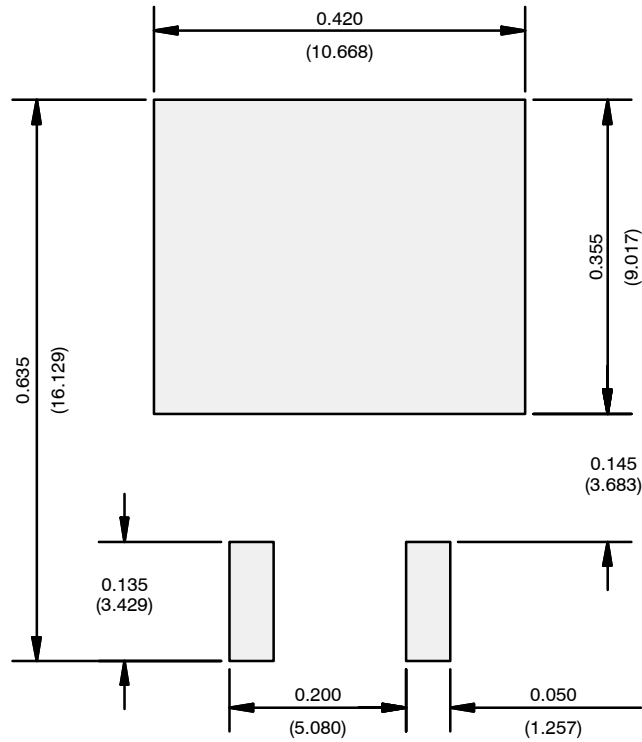


DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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