

N-channel 60 V, 0.021  $\Omega$  typ., 8 A STripFET™ F7  
Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - preliminary data

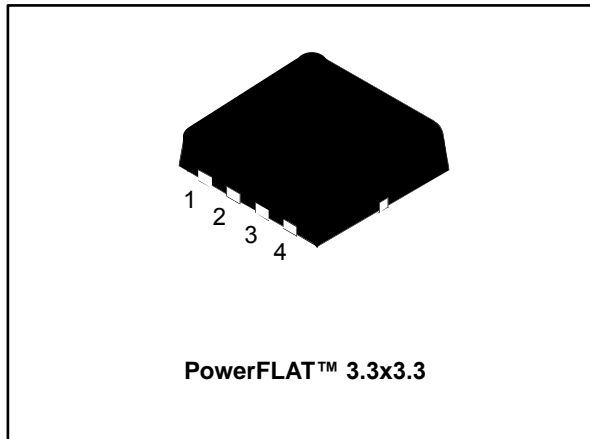
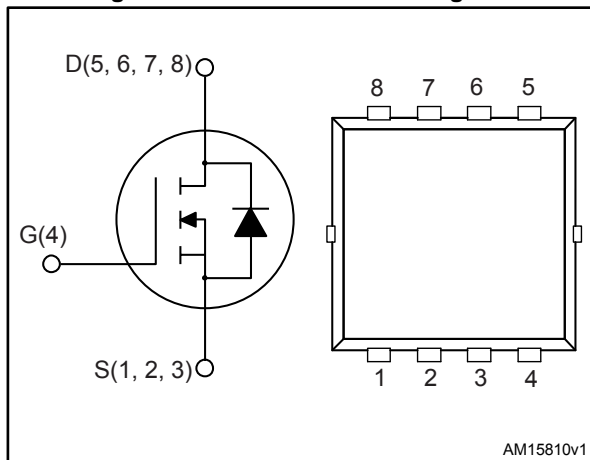


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL8N6F7	60 V	0.025 $\Omega$	8 A

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL8N6F7	8N6F7	PowerFLAT™ 3.3x3.3	Tape and reel

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	36	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	144	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	8	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	32	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	3	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature		

**Notes:**

<sup>(1)</sup>This value is rated according to  $R_{thj-c}$ .

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup>This value is rated according to  $R_{thj-pcb}$ .

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max.	2.1	$^\circ\text{C}/\text{W}$

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec.

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$		0.021	0.025	$\Omega$

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	450	-	pF
$C_{oss}$	Output capacitance		-	210	-	pF
$C_{rss}$	Reverse transfer capacitance		-	22	-	pF
$Q_g$	Total gate charge	$V_{DD} = 48\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 3: "Test circuit for gate charge behavior"</a> )	-	8	-	nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge		-	TBD	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 2: "Test circuit for resistive load switching times"</a> )	-	TBD	-	ns
$t_r$	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
$t_f$	Fall time		-	TBD	-	ns

Table 7: Source-drain diode

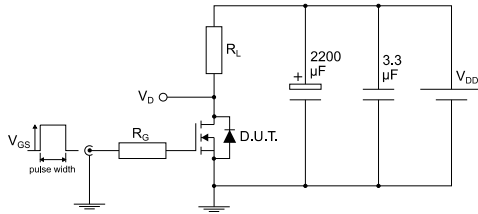
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 8 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_D = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	TBD		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 48 \text{ V}$ (see <a href="#">Figure 4: "Test circuit for inductive load switching and diode recovery times"</a> )	-	TBD		nC
$I_{RRM}$	Reverse recovery current		-	TBD		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

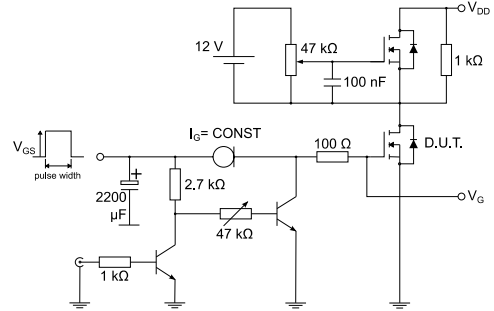
### 3 Test circuits

**Figure 2: Test circuit for resistive load switching times**



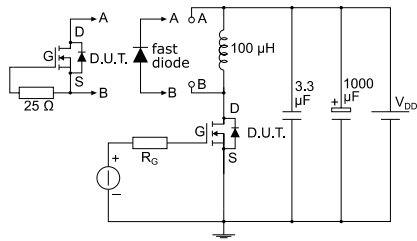
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**Figure 3: Test circuit for gate charge behavior**



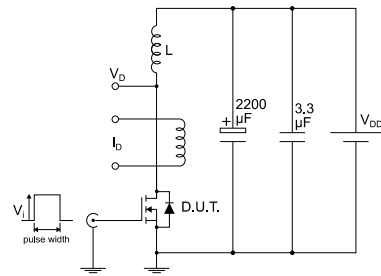
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**Figure 4: Test circuit for inductive load switching and diode recovery times**



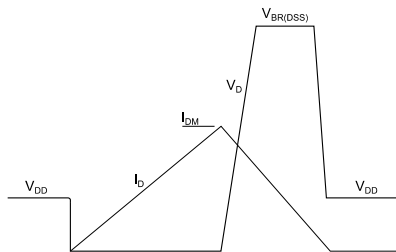
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**Figure 5: Unclamped inductive load test circuit**



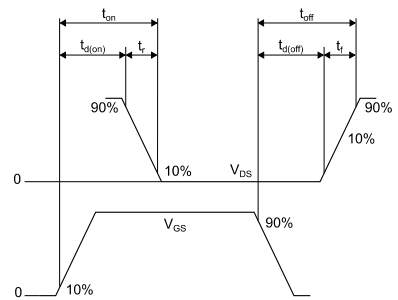
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**Figure 6: Unclamped inductive waveform**



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**Figure 7: Switching time waveform**



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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT 3.3x3.3 package information

Figure 8: PowerFLAT™ 3.3x3.3 package outline

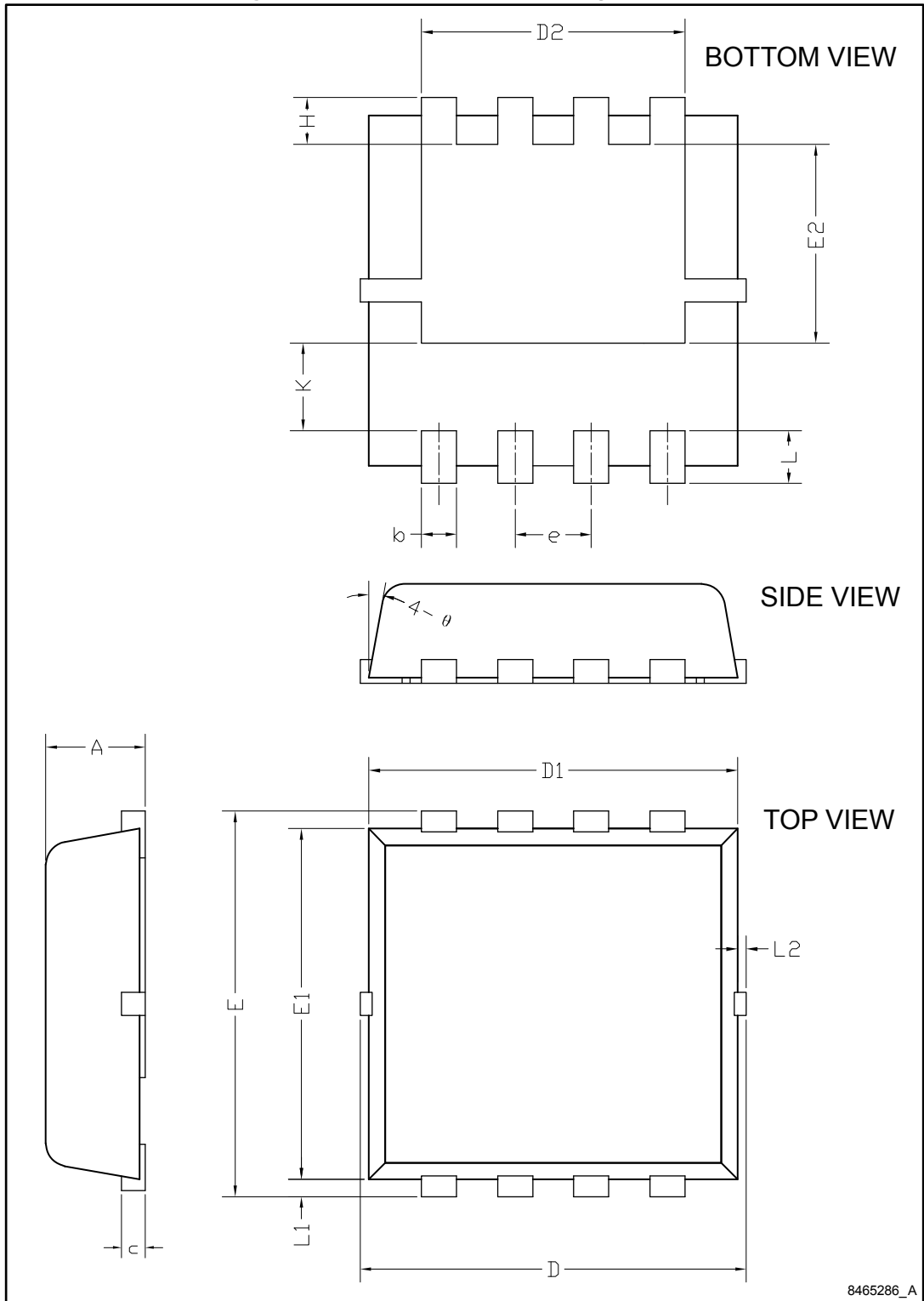
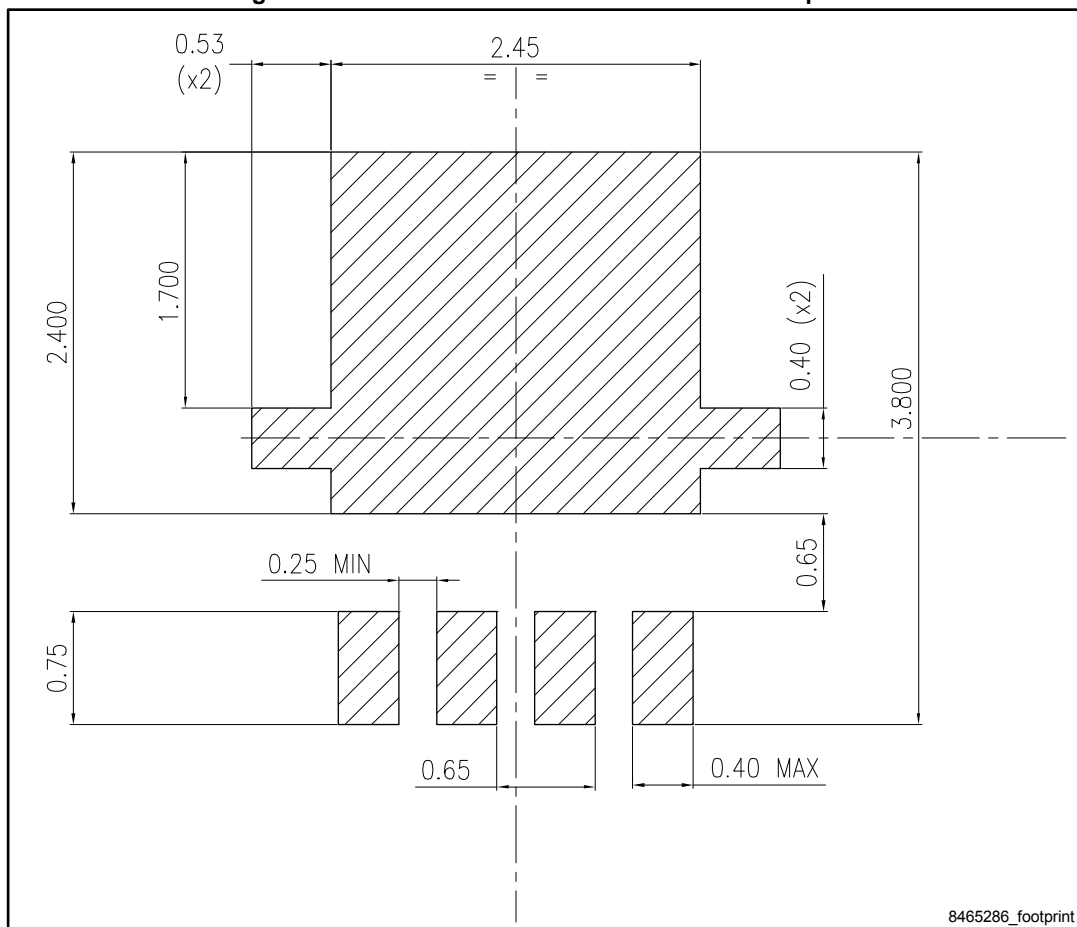




Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.5
∅	8°	10°	12°

Figure 9: PowerFLAT™ 3.3x3.3 recommended footprint



## 5 Revision history

Table 9: Document revision history

Date	Revision	Changes
27-Aug-2015	1	First release.

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