

Power over Ethernet Powered Device With 12V Isolated Supply

DESCRIPTION

Demonstration circuit 1145B, featuring the LTC[®]4267, provides a complete IEEE 802.3af Powered Device (PD) interface and isolated 12V at 0.9A power supply solution for use in Power over Ethernet (PoE) applications. An optional connection is included for a 12V auxiliary supply on the secondary side that disables PoE when present.

The LTC4267 integrates the 25k signature resistor, classification current source, thermal overload protection, signature disable and power good signal along with an undervoltage lockout optimized for use with the IEEE required diode bridge. The precision dual level input cur-

rent limit allows the LTC4267 to charge load capacitors and interface with legacy PoE systems.

The LTC4267 combines the above features with a current mode switching controller designed for driving a 6V rated N-channel MOSFET. It features programmable slope compensation, soft-start, and constant frequency operation, minimizing electrical noise even with light loads.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITIONS	VALUE
Minimum Turn-on Voltage	Input from PSE, I _{OUT} = 100mA	39V
Maximum Turn-off Voltage	Input from PSE	33V
Operating PoE Voltage	Input from PSE, I _{OUT} = 0 to Maximum Output Current	37V to 57V
Maximum Input Current	Input from PSE	350mA
Maximum Output Current	Input from PSE, V _{OUT} = 12V	0.9A
Output Voltage	Input from PSE, I _{OUT} = 0 to Maximum Output Current	12V ±2%
PD Power Class	R _{CLASS} = R7 = 45.3 Ohm	Class 3, 12.95W
Auxiliary input voltage	Input from auxiliary supply, dominant over PSE	10V to 16V
Invalid Signature	PD input, auxiliary supply present	9kΩ

OPERATING PRINCIPLES

Demonstration circuit 1145B interfaces with a customer's PoE test setup per Figure 1. A PSE connects to DC1145B through RJ45 connector J1. The front end of the demo circuit includes the required Ethernet input interface transformer and common mode termination integrated in J1. The LTC4267 after J1 performs IEEE 802.3af interface functions while data is passed to connector J3 to connect to an optional PHY. The switching regulator function is also carried out by the LTC4267 to output an isolated 12V.

Diode bridges D2 and D6 provide the required auto-polarity on the data pairs and spare pairs while C3 provides the PD's 0.1μF capacitance during detection. This demo circuit allows detection and power classification of the PD per the IEEE 802.3af specification. During the detection process of a PD, the LTC4267 displays the proper 25k signature resistor. Classification is programmed by the selection of a single external resistor R7 connected to the R_{CLASS} pin. DC1145B is set for Class 3, full power PD of 12.95W at the input.

OPERATING PRINCIPLES

After detection and classification, the PD is powered up when the input voltage exceeds the LTC4267 turn-on under-voltage lock out (UVLO) through a dual-level current-limited power switch. The 5 μ F capacitance minimum requirement after the in-rush circuit is met with C1 and C9. While the voltage between P_{OUT} and VPORTN is above the Power Good trip point, the amperage through the power switch is held below the low-level current limit. When the voltage between P_{OUT} and VPORTN is below the Power Good trip point, the Power Good signal goes active low and the amperage through the power switch is held below the high level current limit.

For the PD to remain powered on, it must present to the PSE both AC and DC components of the Maintain Power Signature (MPS). The PD must hold the DC MPS by drawing at least 10mA or the PSE may disconnect power. To meet the AC MPS, the PD must present 27k Ω of AC impedance or less. The LTC4267 will remain on with a PSE that uses the AC disconnect method since it will always meet the AC MPS.

The LTC4267 flyback converter operates at a typical switching frequency of 200kHz, controlled by the current mode controller portion of the LT4267. Galvanic isolation

is achieved through transformer T1, capacitor C14 and opto-isolators ISO1 and ISO2.

The primary side power path is comprised of C1, L1, C9, ½ of T1, Q2, and R6. These components should be as close to each other as possible when laying out the printed circuit board. In an actual implementation, a snubber circuit can be added across Q2 to reduce voltage spikes seen at the FET. The secondary side power path is made up of the other ½ of T1, D1, C4, C5 and C6. These parts should also be laid out as close to each other as possible, without overlapping any of the circuitry or traces of the primary side.

When a 12V auxiliary supply is connected at connect J2, which takes over as the supply for the output. ISO2 provides an isolated signal from the auxiliary supply to disable the LTC4267. All LTC4267 signature detection, classification and the internal power MOSFET switch are disabled. A PSE that uses DC disconnect will remove power. The LTC4267 can resume normal PoE operation when the auxiliary supply is removed. If power was removed, then the PSE will perform a new detection and then power the device.

QUICK START PROCEDURE

Demonstration circuit 1145B is easy to set up to evaluate the performance of the LTC4267. For proper equipment setup, refer to Figure 1 and follow the procedure below:

1. Apply an initial load of 100mA at V_{OUT} .
2. Connect a PoE compliant Power Sourcing Equipment (PSE) to RJ45 connector J1.
3. The PSE will detect and power up the PD. Verify output voltage measures 12V.
4. If the PSE has status readout, verify the proper PD power class 3 was detected.
5. In place of a PSE, the DC1145 board can be powered by an alternate input power supply. Connect 48V through the PoE+ and PoE- terminals.
6. Increase the load at V_{OUT} up to 0.9A. Observe the output regulation, ripple voltage, efficiency and other parameters
7. Measure \overline{PWRGD} and SIGDISA relative to POE-. Verify \overline{PWRGD} is logic low and SIGDISA is logic low.
8. Connect a 12V auxiliary supply and verify V_{OUT} equals the new supply.
9. Measure \overline{PWRGD} and SIGDISA relative to POE-. Verify \overline{PWRGD} is logic high and SIGDISA is logic high.
10. Remove the 12V auxiliary supply and verify the PSE power returns.

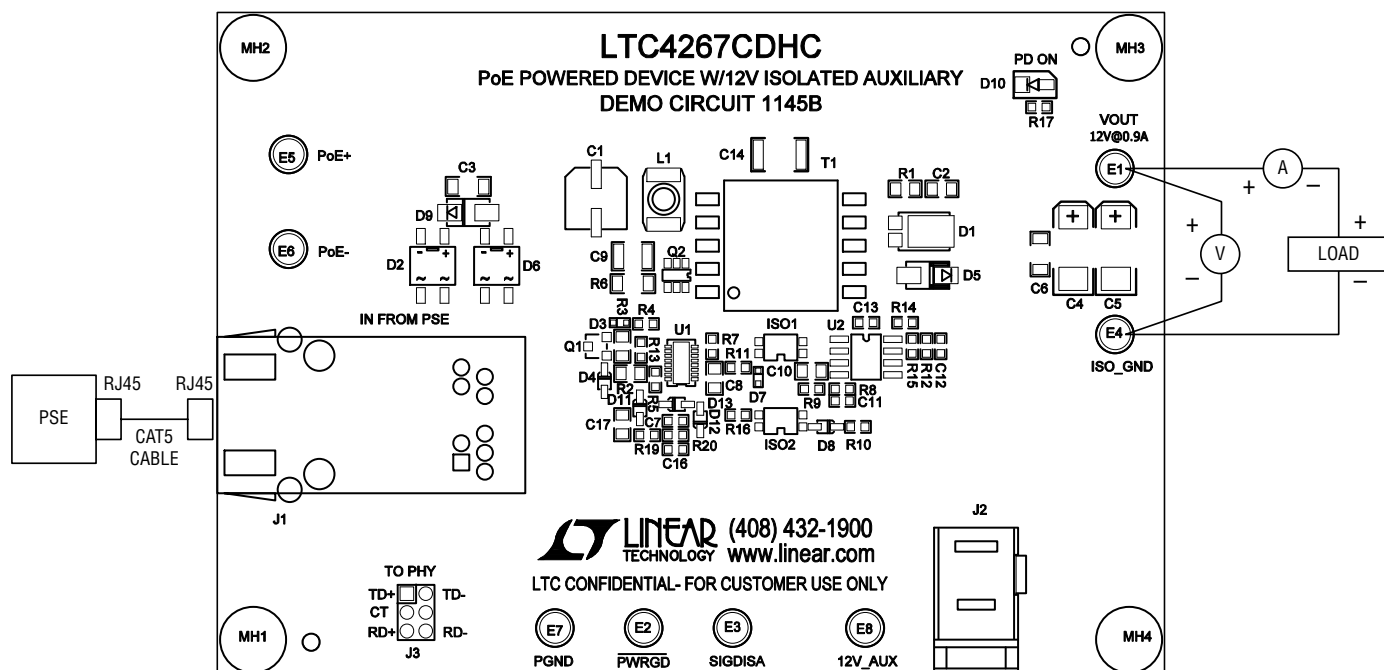


Figure 1. DC1145B Test Setup

MEASURED DATA

Figure 2 and 3 are measured data for a typical DC1145B.

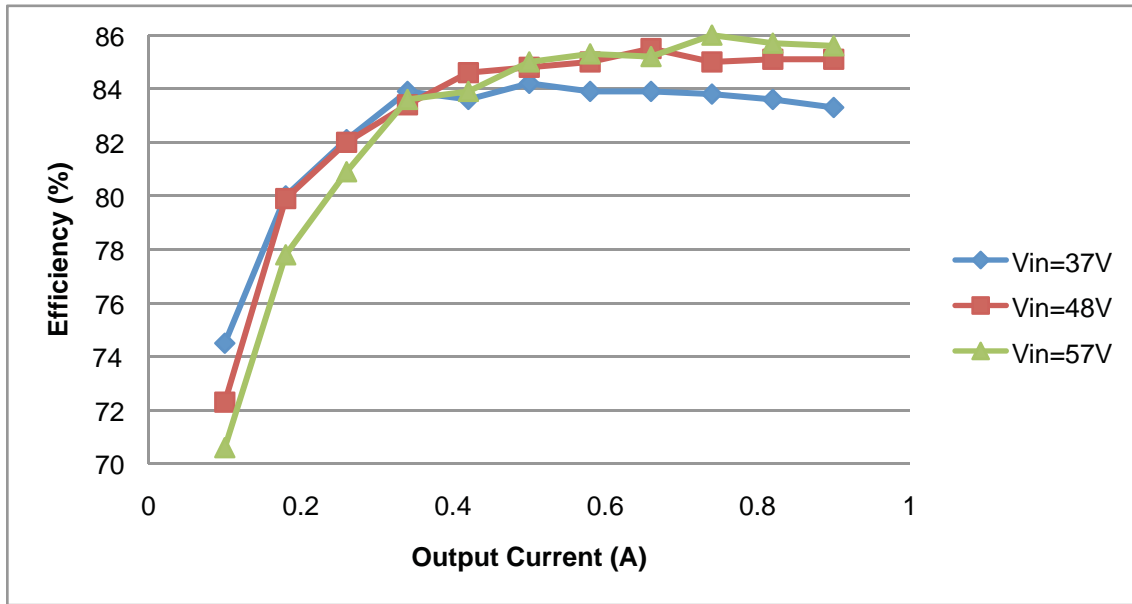


Figure 2: Efficiency (Input Voltage (V_{IN}) is measured at RJ45 Jack)

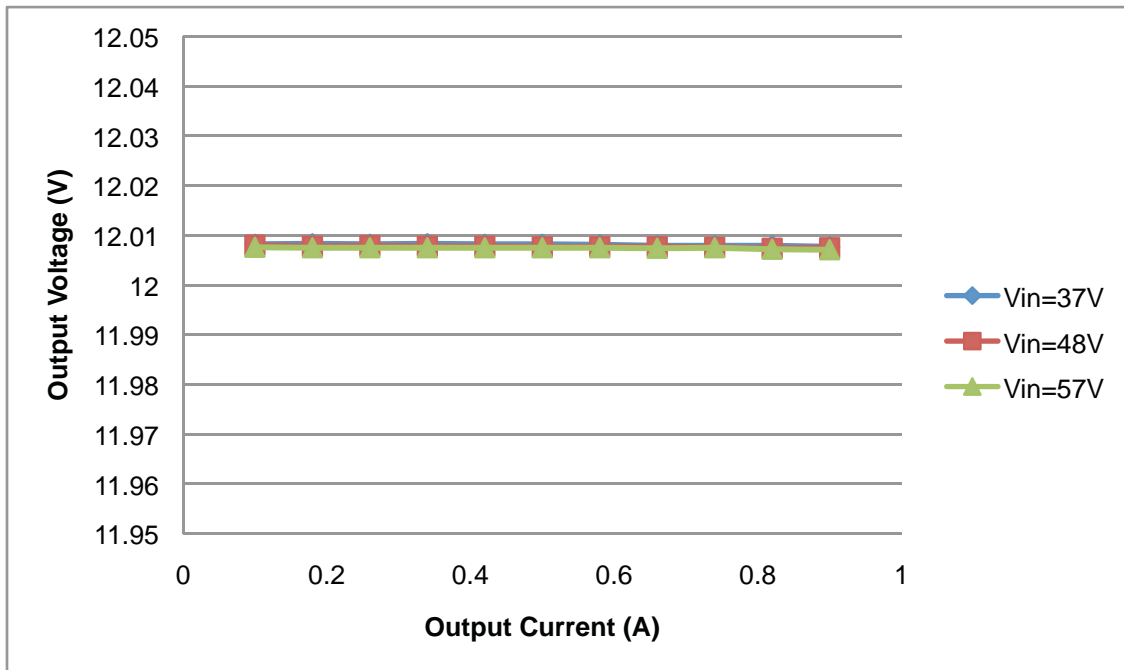


Figure 3: Output Voltage Regulation

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C1	Cap., Elec. 4.7µF 63V 20%	PANASONIC, EEEFK1J4R7R
2	1	C2	Cap., NPO 680pF 50V 10% 0805	AVX, 08055A681KAT2A
3	1	C3	Cap., X5R 0.1µF 100V 20% 1206	Taiyo Yuden, HMK316BJ104ML-T
4	2	C4, C5	Cap., Tant. 47µF 20V 20% 7343	Kemet, T495D476K020ATE100
5	1	C6	Cap., X5R 10µF 16V 20% 1206	Taiyo Yuden, EMK316BJ106ML
6	1	C8	Cap., X5R 4.7µF 16V 20% 0805	Taiyo Yuden, EMK212BJ475MG
7	1	C9	Cap., X7R 1µF 100V 20% 1210	TDK, C3225X7R2A105M
8	1	C10	Cap., X7R 0.01µF 25V 10% 0805	Kemet, C0805C103K3RACTU
9	2	C11, C16	Cap., X7R 0.01µF 25V 10% 0603	Kemet, C0603C103K3RACTU
10	1	C13	Cap., X7R 0.033µF 50V 20% 0603	AVX, 06035C333MAT2A
11	1	C14	Cap., X7R 2200pF 250V 10% 1812	Murata, GA343QR7GD222KW01L
12	1	C17	Cap., X7R 0.47µF 16V 20% 0805	AVX, 0805YC474KAT2A
13	1	D1	Diode, Schottky 3A 60V PowerDi5	Diodes Inc., PDS360-13
14	2	D2, D6	Rect Bridge GP 100V/0.8A PbF	Diodes Inc., HD01-T
15	2	D3, D7	Diode, High Speed	Philips Semi., BAS516
16	2	D4, D8	Diode, Zener 8.2V 200MW SOD-323	Diodes Inc., MMSZ5237BS-7-F
17	1	D5	Diode, Schottky 2A 20V SMA	Diodes Inc., B220A-13-F
18	1	D9	Voltage Suppressor, 58V	Diodes Inc., SMAJ58A-13-F
19	3	D11, D12, D13	Diode, SWITCH 75V 200MW SOD323	Diodes Inc., 1N4148WS-7-F
20	1	ISO1	Opto Iso., NEC High Ctr. PbF	NEC, PS2911-1-K-A
21	1	ISO2	Opto Iso., 4PIN MFLAT SINGLE DC HIGH V COUPLER	NEC, PS2913-1-K-A
22	1	L1	Inductor, 8.2µH DO1608C	COILCRAFT, DO1608C-822ML
23	1	Q1	XSTR, High Voltage PbF SOT23	ON Semi., MMBTA42LT1G
24	1	Q2	MOSFET, N-Chan., 200V SUPERSOT(6LEADS)	Fairchild Semi., FDC2612
25	1	R1	Res., Chip 13 0.1W 5% 0805	Vishay CRCW080513R0JNEA
26	2	R2, R3	Res., Chip 220k 0.1W 5% 0805	Vishay, CRCW0805220KJNEA
27	1	R4	Res., Chip 150 0.1W 5% 0603	Vishay, CRCW0603150RJNEA
28	1	R5	Res., Chip 10k 0.1W 5% 0603	Vishay, CRCW060310K0JNEA
29	1	R6	Res 0.05 OHM 1/4W 1% 1206 SMD	Vishay, WSL1206R0500FEA
30	1	R7	Res, Chip 45.3 0.06W 1% 0603	Vishay, CRCW060345R3FKEA
31	1	R8	Res., Chip 1k 0.06W 5% 0603	Vishay, CRCW06031K00JNEA
32	1	R9	Res., Chip 7.5k 0.1W 5% 0603	Vishay, CRCW06037K50JNEA
33	1	R10	Res., Chip 402 0.1W 1% 0603	Vishay, CRCW0603402RFKEA
34	1	R11	Res., Chip 6.8K 0.1W 5% 0603	Vishay, CRCW06036K80JNEA
35	1	R12	Res., Chip 107k 0.1W 1% 0603	Vishay, CRCW0603107KFKEA
36	1	R13	Res., Chip 200k 0.1W 5% 0603	Vishay, CRCW0603200KJNEA
37	1	R14	Res., Chip 61.9k 0.06W 1% 0603	Vishay CRCW060361K9FKEA
38	1	R15	Res., Chip 28.0k 0.1W 1% 0603	Vishay, CRCW060328K0FKEA
39	1	R16	Res., Chip 100k 0.1W 5% 0603	Vishay, CRCW0603100KJNEA
40	1	R19	Res., Chip 300k 0.1W 5% 0603	Vishay, CRCW0603300KJNEA

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PARTS LIST

41	1	R20	Res., Chip 100 0.1W 5% 0603	Vishay, CRCW0603100RJNEA
42	1	T1	Transformer, PoE	Pulse, PA1138NL
43	1	U1	I.C., PoE Switching Reg. DFN(16)(DHC)5mm × 3mm	Linear Tech.Corp.LTC4267CDHC#PBF
44	1	U2	I.C., Prog. Reference S08NB	Linear Tech. Corp., LT1431CS8#PBF

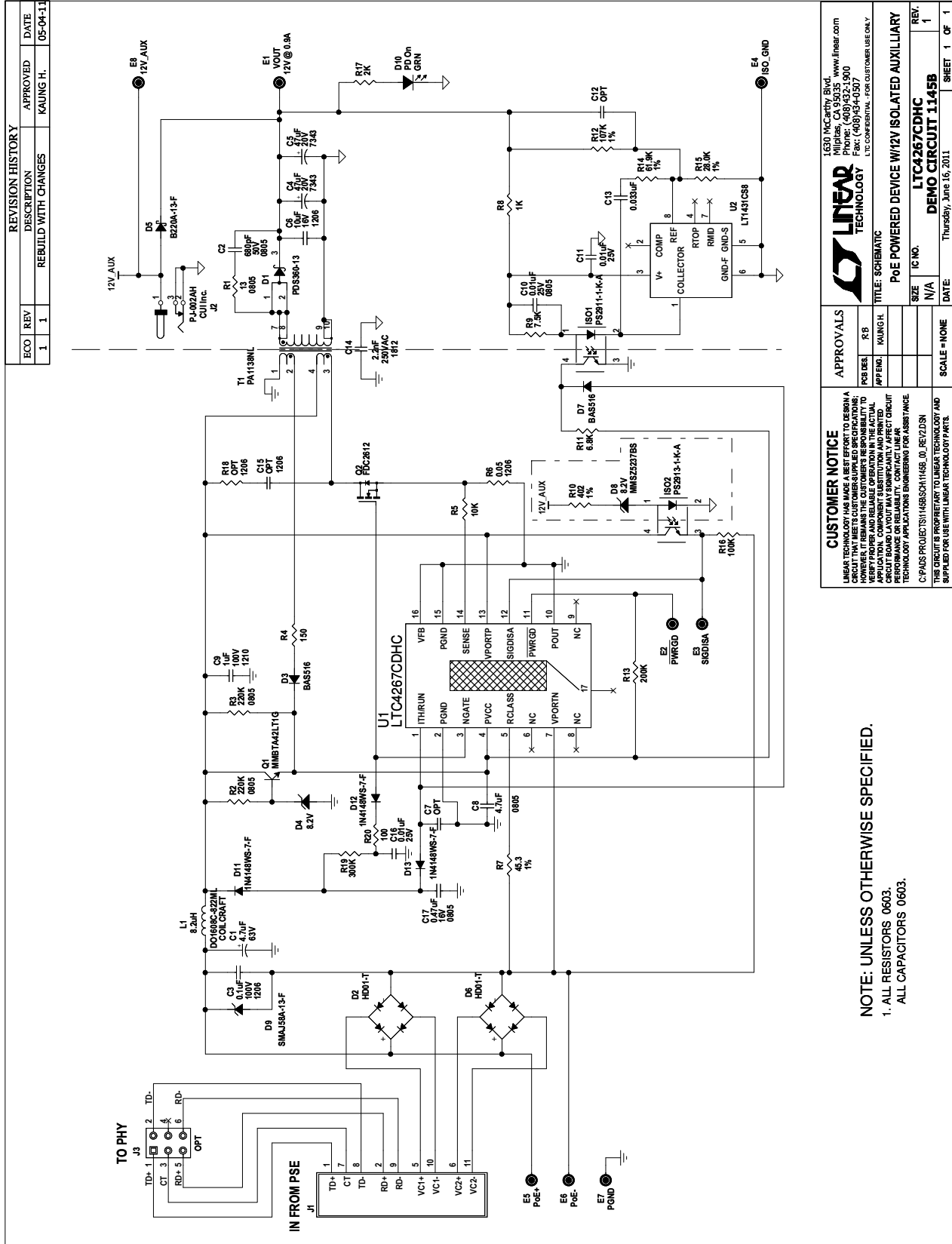
Additional Demo Board Circuit Components

1	0	C7, C12 (Opt)	Cap., 0603	
2	0	C15 (Opt)	Cap., 1206	
3	0	J3 (Opt)	Headers, Dbl. Row 2mm Ctrs.	CommConn Con Inc., 2202S-06G2
4	0	R18 (OPT)	Res., 1206	

Hardware for Demo Board Only

1	1	D10	LED, GRN	Panasonic, LN1351CTR
2	8	E1, E2, E3, E4, E5, E6, E7, E8	Turret, Testpoint	Mill Max, 2501-2-00-80-00-00-07-0
3	1	J1	Pulse Jack, PowerJack T12	Pulse Engrng., JK0-0044NL
4	1	J2	Connector, Wall Adapter	Cui Inc., PJ-002AH
5	4	MH1, MH2, MH3, MH4	STAND-OFF, NYLON 0.25" tall	KEYSTONE, 8831(SNAP ON)
6	1	R17	Res., Chip 2k 0.06W 5% 0603	Vishay CRCW06032K00JNEA
7	1		FAB, 1145B_Rev1	DEMO CIRCUIT 1145B

SCHEMATIC DIAGRAM



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DEMO MANUAL DC1145B

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